FAST ORBIT FEEDBACK WITH LINUX PREEMPT_RT

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Abstract

The fast orbit feedback (FOFB) system in development at the Australian Synchrotron (AS) [1] aims to improve the stability of the electron beam by reducing the impact of insertion devices and targeting orbit perturbations at the line frequency (50 Hz, 100 Hz and 300 Hz). The system is designed to have a unity gain at a frequency greater than 300 Hz with a simple PI controller with harmonic suppressors in parallel (as was done at Elettra). With most of the system in place (position aggregation, power supplies and corrector coils) we decided to implement a PC based feedback system to test what has been installed as well as the effectiveness of the proposed control algorithms while the firmware for the FPGA based feedback processor is being developed. This paper will report on effectiveness of a feedback system built with CentOS and the PREEMPT patch running on an Intel CPU.

INTRODUCTION

The ultimate goal of the feedback system is to ensure that the transverse RMS beam motion up to 100 Hz is kept to less than 9.0 µm horizontally and 1.6 µm vertically.

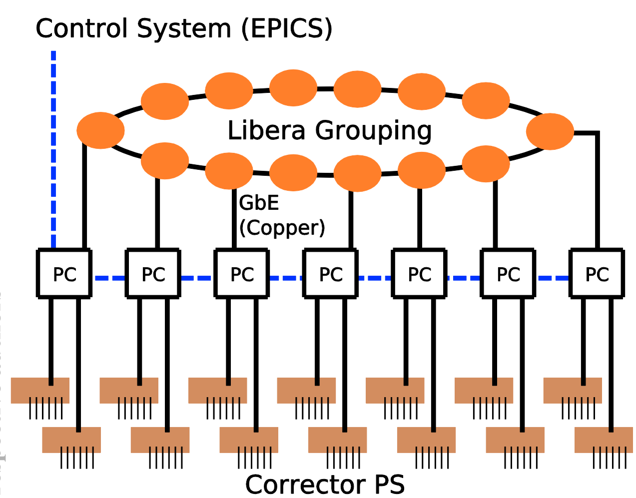

Figure 1: Distributed PCs processing the Fast Acquisition Data from the EBPMs and calculating the correction for the power supplies. No direct synchronisation between PCs. Control of the feedback system is through EPICS process variables running on a virtual server.

Figure 1 shows the distributed configuration of the seven PCs used to control the 14 power supplies around the storage ring. Each of the seven PCs receive real-time Fast Acquisition (FA) position data from the Libera Electron beam position processors (EBPMs), calculate and transmit the correction to the magnet power supplies through a 10 MBaud serial link. The synchronisation of the corrections between the PCs depends on the ability of the application to process the data in a repeatable time period and the synchronicity of the FA data transmitted by the EBPMs.

LINUX PREEMPT_RT PATCH

To achieve a repeatable processing period, with a tolerance of 10s of µs, a "realtime" operating system is required. There are many potential candidates, such as RTEMS and VxWorks, however in the interest of minimising the development time, a decision was made to attempt it with our nominal production operating system at the AS (CentOS) with a PREEMPT_RT patched kernel.

The PCs use a PCI-x serial card by Axxon to communicate with the power supplies (the Linux serial driver had to be patched to get the card to operate at the maximum rate). The test the "realtime" nature of the operating system and applications, a test program was written to transmit data packets at a rate of 5 kHz (using *clock_nanosleep* to set the period) and the period of the transmitted serial data measured on an oscilloscope. The program was tested with CentOS 5 (kernel 2.6.29.6-rt24; Intel Core2 Q8400 2.66 GHz) and CentOS 7 (kernel 3.10.75-rt80; Intel Celeron G1840 2.80 GHz).

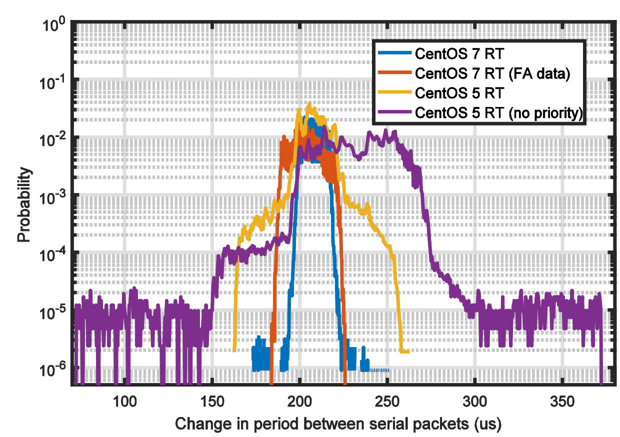

Figure 2: The newer kernel performs better and by setting a high scheduling priority the peak to peak jitter can be reduced to <100us. In the best case the peak to peak jitter is < 80 us with greater than 99.995% occurring within a 30 us window. If the serial output is triggered by the incoming FA data the jitter is subsequently worse due to jitter on the processing of the incoming data. (The sample size varies from 350k to 1300k).

The results of the measurements shown in Figure 2 indicate that upgrading from CentOS 5 to CentOS 7 reduces the jitter by almost half. In the best case more than

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99.995% of the measured period was within a 30 µs window. Without the patch, such a tight timing control is not possible.

The periodicity of the incoming FA data packets was also tested by measuring the period between packets using *clock_gettime*. The purpose is to test the response of the network interface (it is known that the EPBMs transmit the packets with timing jitters less than µs). Using the on-board Realtek (RTL8111/8168/8411) gigabit network interface the measured periods were between 1 µs to 400 µs, which is unacceptable. Changing to an Intel (82574L) gigabit network interface, the measured periods were between 70 µs and 130 µs with an average of 99.4 us.

Figure 2 (second trace) also shows the jitter in the period when the incoming packets is used as a trigger to transmit the serial data with a width of ~50 µs. With a potential processing latency of 80 µs (discussed later in this report), the system is unable to run the feedback loop at 10 kHz and can only run at 5 kHz.

SYNCHRONICITY BETWEEN PCS

The synchronisation of the PCs is vital and depends on the EPBMs synchronously transmitting the FA data. The serial output from two PCs was monitored and the difference in the transmission time was measured. The results in Figure 3 show a static offset of 13 µs with a spread of 2 µs showing that the data packets are well synchronised with fixed offsets relative to each other. The static offsets are sufficiently small that it will not degrade the efficiency of the system however it is sufficiently small to not (at 1 kHz an offset of 30 µs corresponds to a phase shift of 11 degrees).

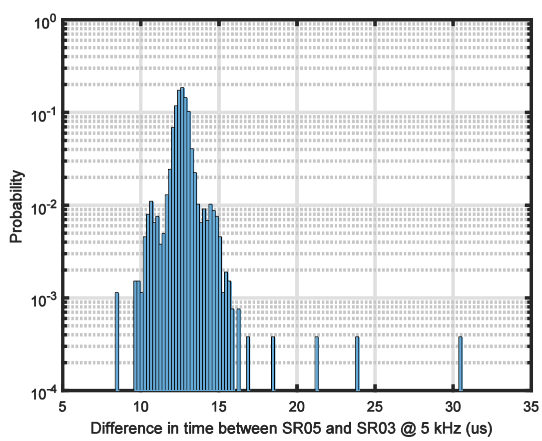

Figure 3: An offset of 13 us between two PCs is observed with a FWHM spread of 2 us (dataset of 2700).

CONTROL ALGORITHM

The feedback system uses a combination of a PI controller and harmonic suppressors at 50 Hz, 100 Hz and 300 Hz with a bandwidth of 0.2 Hz, 0.4 and 1.2 Hz, respectively. This method follows the system successfully implemented at Elettra [2]. The coefficients for the biquad peak filters were pre-calculated using Matlab for 50 Hz, 100 Hz and 300 Hz (for a sample rate of 5029 S/s). Phase delays were not tested, however with an estimated system latency of around 200 µs the phase error at 300 Hz should be less than 22 degrees.

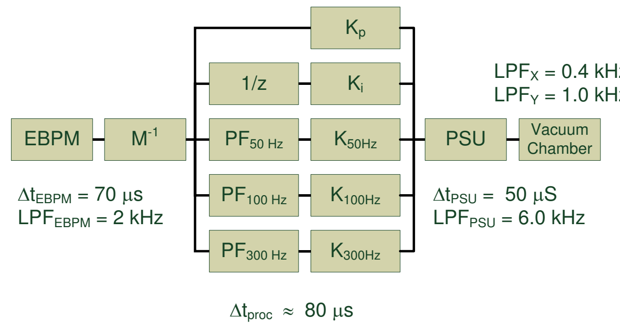

Figure 4: Block diagram showing the EBPMs, inverted BPM-corrector response matrix (M^{-1}), corrector magnet power supply (PSU) and the vacuum chamber. The feedback system uses a PI controller (K_p, K_i) as well as harmonic suppressors (using peak filters, PF) with the corresponding gain control (K_{freq}). The latencies (Δt) and frequency response (LPF) for the EBPM, PSU and vacuum chamber have been measured [1] while Δt_{proc}, is an estimate based on simulations shown later in this report.

RESULTS

After a few false starts we were soon running with the full system. The integrated horizontal and vertical RMS beam motion averaged across all insertion devices is show in Figure 5. The results with the feedback system are compared against to two operational modes related to the RF system. The AS Storage Ring is to operate with four warm RF cavities generating a total potential of 3 MV. For operational reasons a decision was made to run with three RF cavities and to drop the voltage to 2 MV. While rotating through the different triplet of cavities, the beam stability was observed to improve significantly when one particular cavity was not operational. This single cavity contributed significantly to the 50 Hz perturbations. Since then this cavity has been left on standby and work to isolate the cause of the perturbation to the beam has so far been unsuccessful.

Figure 6 shows the efficiency of the harmonic suppression on the line frequency perturbations, between -15 dB and -30 dB reduction in noise.

Matlab Models

The elements in the feedback system as shown in Figure 4 can be modelled in Matlab however a missing part is the processing latency of the PCs. In Figure 7 the measured results are compared against a model and the total system latency of the model changed to get the best fit at the higher frequencies. The best fit gave a total system latency of 200 µs. Removing all other known fixed delays in system (see Figure 4), the processing delay can be inferred to be around 80 µs.

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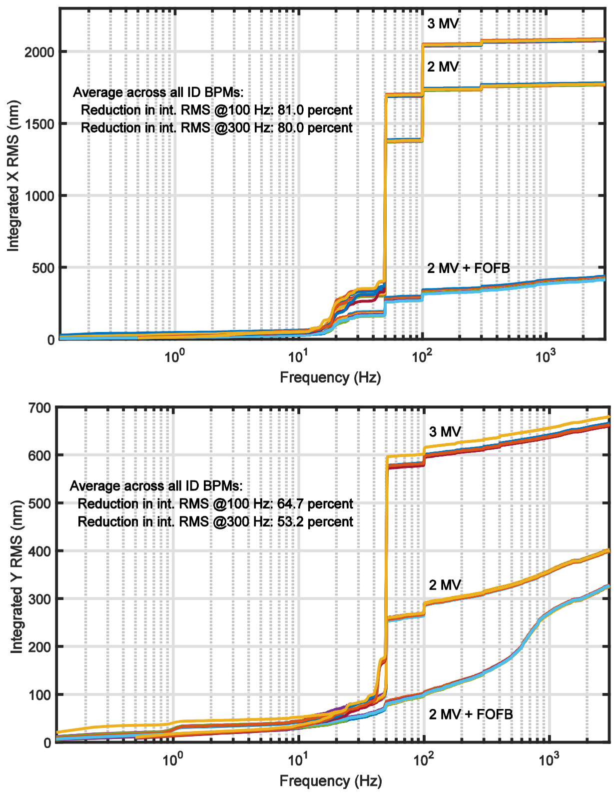

Figure 5: Integrated horizontal (top plot) and vertical (bottom plot) RMS averaged across all insertion device BPMs. There are 4 data sets shown here for three different conditions: 4 cavity operation (3 MV), 3 cavity operation (2 MV), with FOFB.

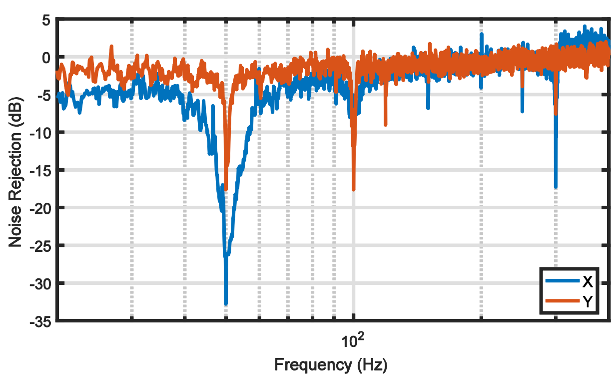

Figure 6: Efficiency of the harmonic suppressors showing between -15 dB and -30 dB reduction in noise. The harmonic suppression at 300 Hz for Y was disabled.

During the design phase, the initial estimates for the zero gain frequency crossing was 300 Hz (horizontally) and 370 Hz (vertically). With the PC based FOFB system the zero gain frequency crossing was measured to be as much as 325 Hz (horizontally) and 400 Hz (vertically) and with the FPGA implementation, this is expected to increase to above 400 Hz in both planes.

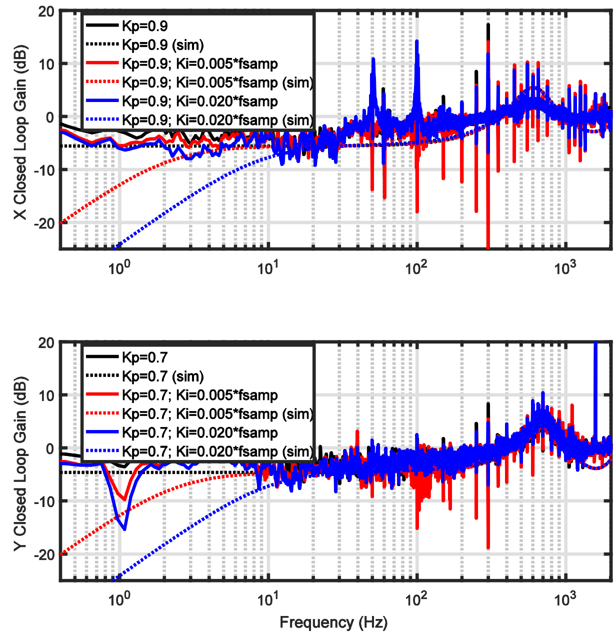

Figure 7: Ratio of the spectrum with and without feedback enabled with different integral coefficients, K_i. The measured results are compared to simulated bode plots calculated in Matlab assuming the properties shown in Figure 4 and a total system latency of 200 μs.

Insertion Device Perturbations

One of the goals of the fast feedback system is to ensure that perturbations from scanning insertion devices are minimised. In Figure 8 gap and phase scans on an APPLE II undulator are started under three conditions: with fast feedback (FOFB), with slow feedback (SOFB; 1 Hz) and no feedback.

The results with FOFB showed that it is possible to maintain orbit distortions to less than one μm even with large perturbations. The frequency analysis of the orbit perturbation during gap and phase scans showed that the perturbations had frequency components up to 10 Hz. Therefore with appropriate values for K_i it was possible to damp the perturbation by an order of magnitude (20 dB). The integral component also successfully damps a 1 Hz vertical perturbation as seen in Figure 7 and Figure 8 (as fuzziness to the vertical position with no FOFB).

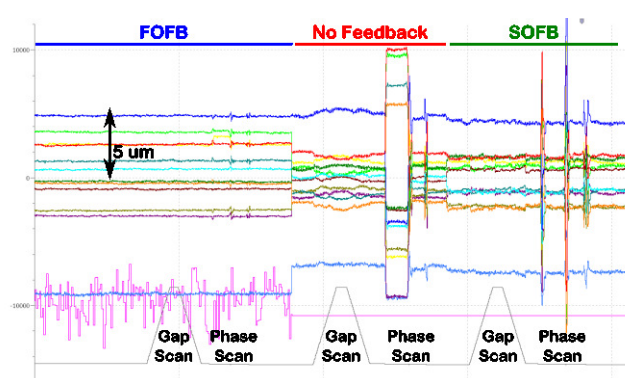

Figure 8: The APPLE II is the most disruptive of Insertion Devices (IDs). The gap and phase was scanned with

fast feedback (FOFB), slow feedback (SOFB; 1 Hz) and no feedback. Large vertical perturbation during the phase scan seen without feedback was caused by a fault in the feedforward table. FOFB can maintain vertical orbit perturbations below 1 µm.

Slow and Fast Correctors

The storage ring now has a set of slow Horizontal and Vertical Corrector Magnets (42 HCM and 56 VCM) and a set of Horizontal and Vertical Fast Corrector magnets (42 HFC and 42 VFC).

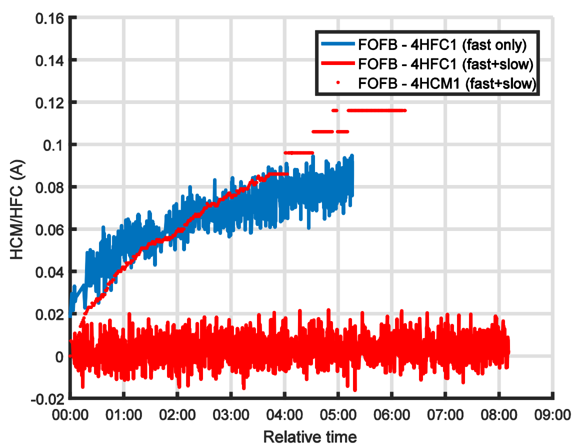

Figure 9: With only the fast correctors, the DC component starts to drift. By understanding the relationship between the slow and fast correctors, the "DC" component can be offloaded from the fast correctors to the slow correctors, thereby maintaining a "DC" value close to zero for the fast correctors.

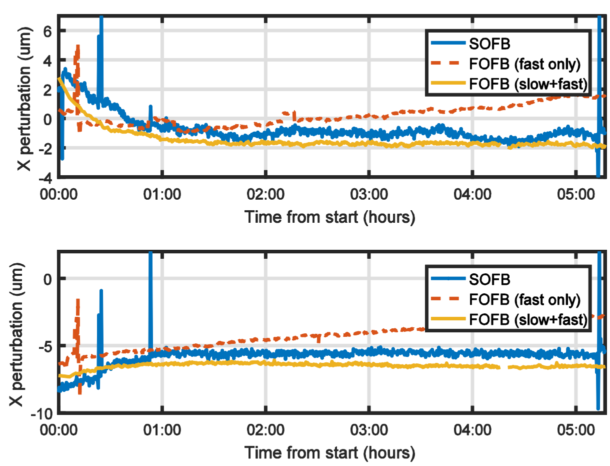

Figure 10: Example of two horizontal orbit positions when operating with feedback. With SOFB there is an initial period after injection where the storage ring is warming up, resulting in a drift of a few µm. With FOFB and just the fast correctors, there are additional drifts associated, to a more extensive shut down period and therefore longer warm up time and the feedback does not compensate for the slow drifts. With FOFB utilising both fast and slow magnets, the slow drift is eliminated and the position over the 5 hour period is more stable. The initial drift seen all three cases is likely caused by movements in the vacuum chamber as the ring warms up after a maintenance period.

The first 5 hour test of the FOFB system kept the slow magnets static. As expected the DC component of the fast corrector magnets drifted. This is a concern because the full range of the fast corrector power supplies is only ±1 A. It is therefore important to ensure that the DC component does not eventually saturate the power supply. In the second 8 hour test, the method for managing slow and fast correctors developed at Soleil was successfully implemented [3] to utilise both sets of magnets (RF corrections are excluded for now). Figure 9 shows that with this implementation, the DC drift is no longer present. Figure 10 shows that utilising the fast and slow correctors ensures better long term stability of the feedback system.

CONCLUSION

A PC based FOFB system has been developed over a short period of time with standard PC components to operate at a cycle rate of 5 kHz. The PI controller successfully damped frequencies below 30 Hz while the harmonic suppressors reduced the line frequency perturbations by as much as 30 dB. The zero gain cross over frequency was better than expected, measured at 325 Hz (horizontally) and 400 Hz (vertically).

Developing this system and running it has shown what the FOFB system is capable of doing (commissioning in Jan 2017), how it works and highlighting deficiencies in the original design. The refinements and diagnostics developed for this project has led to additions to the design of the system that would otherwise have not been discovered until commissioning. Implementing the FOFB in this manner is straight forward with minimal initial hardware costs. However there are open questions regarding the reliability and maintenance over its 10 year life span. Otherwise it is a very useful platform for prototyping control algorithms and diagnostics.

ACKNOWLEDGEMENT

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