ISBN: 978-3-95450-192-2 doi:10.18429/JACoW-IBIC2017-WE1AB1

THE SPS WIDEBAND FEEDBACK PROCESSOR: A FLEXIBLE FPGA-BASED DIGITAL SIGNAL PROCESSING DEMONSTRATION PLATFORM FOR INTRA-BUNCH BEAM STABILITY STUDIES

J. E. Dusatko#, J. D. Fox, C. H. Rivetta, O. Turgut (SLAC National Accelerator Laboratory, Menlo Park, California USA), E. Bjorsvik, W. Höfle (CERN, Geneva Switzerland)

Abstract

A flexible digital signal processing platform based on FPGA technology has been developed for vertical intra-bunch beam stability studies at the CERN SPS. This system is unique in that samples at a very high rate (4GSa/s) in order to measure and control motion within the 1.7ns proton beam bunch. The core of the system is an FPGA-based digital signal processor. Being programmable, it enables fast development of control algorithms. The processor, together with its supporting components forms a complete platform for demonstration studies of beam instability measurement and control. This system is capable of operation as either a stand-alone arbitrary waveform generator for driven mode instability studies, a closed-loop feedback control system for stability control and as a diagnostic instrument for measurement of beam motion. Recent measurements have shown the system is effective at damping single-bunch and bunch train intra-bunch instabilities with growth times of 200 turns. This paper summarizes the system design, provides some operational highlights, describes the upgrades performed to date and concludes with a description of the next generation processor now in development.

INTRODUCTION

The CERN Super Proton Synchrotron (SPS) accelerates protons for injection into the LHC. Control of performance-limiting transverse vertical bunch beam instabilities is normally handled a by dedicated transverse damper system [1]. For the planned High Luminosity LHC Upgrade (HL-LHC) [2], concerns have arisen that with the higher beam intensities, transverse intra-bunch motion driven by transverse mode coupling instability (TMCI) and the electron cloud instability (ECI), may become a limiting factor in the luminosity of the upgraded LHC [3,4]. Transverse beam instabilities within the SPS are being addressed in three ways: machine lattice configuration, vacuum chamber coating with amorphous carbon and active electronic feedback control, which is the role of the wideband feedback system (WBFB).

The hardware details of this system are described in another publication [5], presently we describe the design of the system with a focus on the signal processor.

SYSTEM DESCRIPTION

The comprehensive Wideband Transverse Feedback System (WBFB) consists of an ensemble of components. The system block diagram is shown in Figure 1.

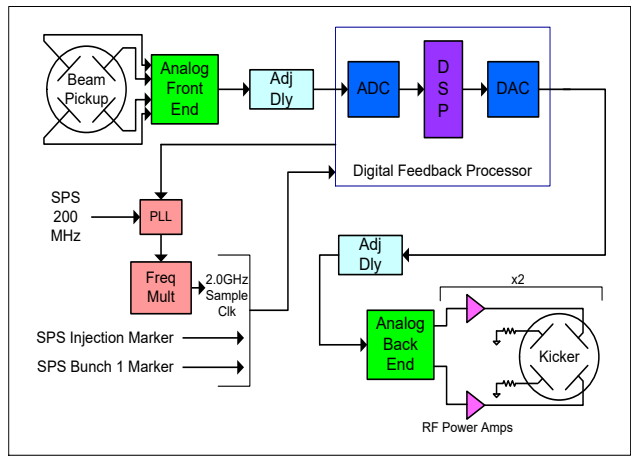

Figure 1: System Block Diagram.

DIGITAL FEEDBACK PROCESSOR

The Feedback Processor is designed as a general-purpose digital signal processing system with integrated data converters. A block diagram is shown in Figure 2. An FPGA implements all of the data formatting, system control and signal processing functions, as well as ancillary/support functions (e.g. control of the input trigger comparator threshold DACs). This is the most complex subsystem. Its functions and design will now be described.

Feedback Mode

In feedback mode, the processor can selectively compute corrections for [1…64] bunches or [1…32] scrubbing bunch doublets [6]. In non-doublet mode a 5ns sample window across the bunch takes 16 samples or slices (these parameters are 2x for doublets). The current control algorithm treats each slice as an independent signal and applies a non-recursive Finite Impulse Response (FIR) digital filtering function to that signal. Thus there are 16 FIR filters for each bunch, the filters have identical coefficients and are 16 taps long. The FIR filter is expressed as:

$$y(n) = \sum_{k=0}^{15} h(k)x(n-k)$$

*Work supported by the U.S. Department of Energy under contract DE-AC02-76SF00515, the US LHC Accelerator Research program (LARP), the CERN LHC Injector Upgrade Project (LIU) and the US-Japan Cooperative Program in High Energy Physics.
#jedu@slac.stanford.edu

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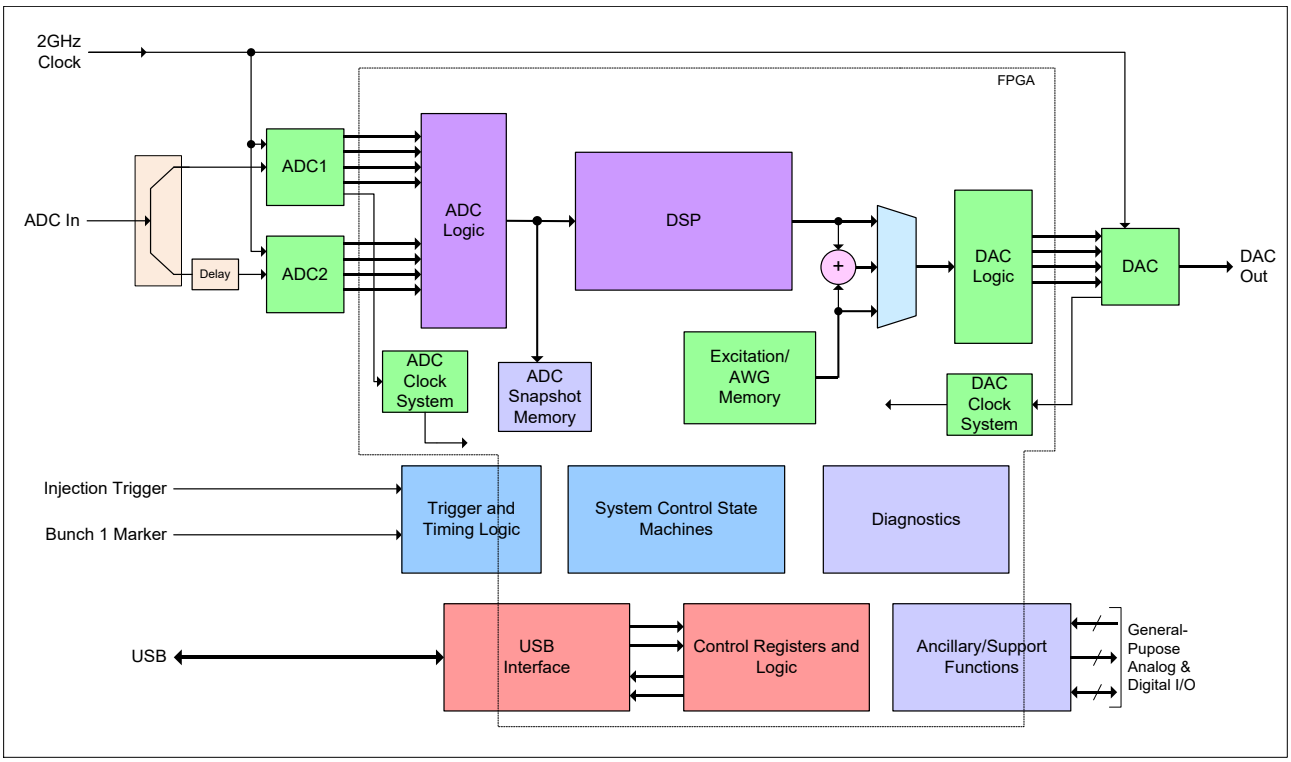

Figure 2: Feedback processor block diagram.

The coefficients are loadable from a configuration file. A useful feature is the ability to program the filter between two coefficient sets based on counting the number of ring fiducials. This allows us to "swap" the coefficients, selectively applying a different feedback mode (e.g. positive, then negative) for a programmable period of time

This is very useful for grow/damp studies where the beam can be dynamically driven into instability and then damped, simply by swapping coefficient sets.

Excitation Mode

For driven mode studies, the system can act as arbitrary waveform generator by loading its excitation memory with any desired sequence (e.g. chirps, spatial shaping, etc.) and playing it out based on programmed timing parameters. The waveform memory is loaded from an external file, and selectively drives a single bunch.

Special Modes

A variant of Feedback and Excitation mode, called Feedback Excitation Combined (FEC) is available that allows both modes to run in parallel for driven feedback studies. The feedback and excitation signals are numerically summed before being sent to the DAC. This eliminates the need for a separate excitation system.

Another special mode provides the ability to selectively control the gain of each individual slice over a range of [+1…-1] to allow unique gain (and sign) of feedback for each slice.

A selective mode has been added to compensate for the long tail present in the transient response of the RF power amplifiers, which can interfere with the next beam bunch. Compensation is accomplished by adding in a pre-amble, post-amble or split pre-/post-amble to the output DAC waveform. These added components act to upconvert the low frequency information onto a higher frequency carrier. The waveform is then sampled by the beam and mixed back down to the low frequency. This mode has been verified in operation.

Diagnostic Features

While driving and controlling the beam are the central functions for the feedback processor, it is also crucial to study the bunch motion directly as a diagnostic. The system includes a snapshot memory that can record all 16 samples from one selected bunch over many (up to 65536) turns. A future upgrade will use on-board DDR3 memory for recording of multiple bunches over many turns.

Hardware Design

The feedback processor is designed with combination of commercial and custom components. A commercial FPGA motherboard (Dini Group, Inc DNMEG_V6HXT, Figure 3.) was selected that offered high-density I/O connectors. The board contains a Xilinx XC6VHX565T FPGA device. Though optimized for high-speed serial I/O, it contains 566K logic cells, with a smaller complement (864) of DSP slices. The motherboard also contains provision for a DDR3 memory DIMM.

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The DAC device used is a Maxim Semi MAX19693 4GSa/s 12-bit device (used in 8-bit mode) it accepts four parallel LVDS data streams. It is designed onto a custom daughterboard, which also contains a USB2.0 interface used to communicate with the host computer, trigger input conditioning circuitry, diagnostic strobe output circuity, clock circuitry as well as general-purpose low speed digital and analog I/O. It interfaces to the FPGA motherboard, via a high-density connector.

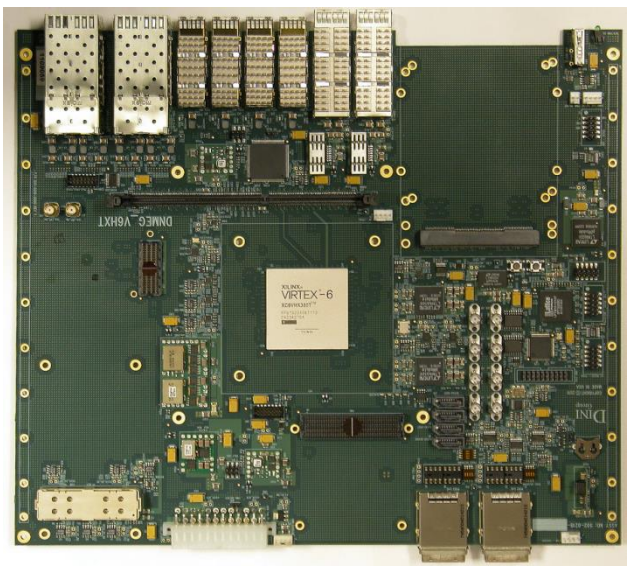

Figure 3: Commercial FPGA motherboard.

Analog to digital conversion at 4GSa/s was not common place when the feedback processor was originally designed. This was accomplished by time-interleaving two Maxim Semi MAX109 2GSa/s 8-bit ADCs, each with 2.2GHz of analog bandwidth. Time interleaving is accomplished by splitting and delaying the ADC analog signal on one leg by one half the sample clock period. Each ADC outputs four parallel LVDS streams. Time and budget constraints did not allow a custom board to be designed. Instead, two MAX-109EVB evaluation boards were used with a custom high speed coaxial parallel cable assembly developed in collaboration with the Samtec corporation.

Gateware Design

The FPGA implements a major portion of the system functionality. A convenient consequence of this is ease of reconfigurability. All development is done in VHDL. The design can be roughly broken down into three major sections: signal dataflow/processing, diagnostics and control & support.

The dataflow section is a pipeline structure that receives the ADC data, formats it, computes the correction and then reformats it for the DAC output. The pipeline, located inside the DSP block is buffered by two FIFO memories at the input and output with the processing algorithm in the middle. Clock domain crossing between the ADC and DAC is handled by the output FIFO. The design is structured so that the processing algorithm can be easily plugged/un-plugged in the system.

The current signal processing algorithm is a multichannel bank of 16, 64-channel, 16-tap FIR filters. All data is processed in 8-bit, two's complement format. Fitler coefficients are 8-bits as well, producing a 20-bit computational result. A shift gain/saturation block is used to programmably scale the filter result to the 8-bit DAC window and handle over- and under-flow properly by saturating full-scale in the appropriate direction.

The diagnostic section contains the snapshot and excitation memories as well as timing diagnostics (e.g. detect missing fiducial trigger). Both memories are implemented with on-chip SRAM. The FPGA motherboard has provision for up to 16GB of DDR3 memory, which we plan to use for deep snapshot recording of multiple bunches.

System control is handled by a hierarchy of three state machines. The master state machine receives the trigger markers, counts the fiducial pulses and directs and sequences the operation of the two other units which control the ADC/DSP and DAC, respectively. A set of memory mapped control and status registers are exposed through the USB2.0 interface. A limiting factor in the transfer of large datasets to and from system is the USB bottleneck, plans exist to implement an 1Gbps Ethernet interface to alleviate this.

Software Design

As in any modern electronic system, much functionality is implemented via software. The WBFB software design is broken into two categories: hardware interface & control and offline applications for configuration and analysis.

The interface to the system is implemented in Microsoft Visual Basic (VB), which connects to the hardware via USB driver calls. VB has proven to be a fast, simple way to implement complex functions in a GUI-based environment. System setup is simplified using a text-based configuration file loaded at system startup. The passing of setup information (filter coefficients, excitation data, etc.) and snapshot data is facilitated using text-based files. These files are auto-generated by the offline and VB applications, respectively.

The offline applications are developed using Matlab. Several applications exist to enable the design of excitation waveforms, digital filter functions, snapshot data viewing and in-depth signal analysis. These applications exist as both GUI-based and command line tools.

OPERATIONAL HIGHLIGHTS

The WBFB system has been used in multiple Machine Development (MD) studies at the SPS [7-9]. In these studies, beam dynamics were measured in different situations: driven-mode only with no feedback, driven-mode with feedback, positive and negative feedback and specical configurations of the SPS lattice where conditions were created to enhance bunch instabilities. Both single- and multi-bunch dynamics were studied. In driven-mode

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studies, we have been able to demonstrate excitation of low mode intra-bunch instabilities by either driven excitation or positive feedback, followed by damping of those instabilities.

Using ADC snapshot data taken during a June 2016 MD at the SPS, Figure 4 shows a multibunch case zooming in on bunch 71 of batch 4 of a typical LHC fill. The top graph shows the no feedback case: the bunch becomes

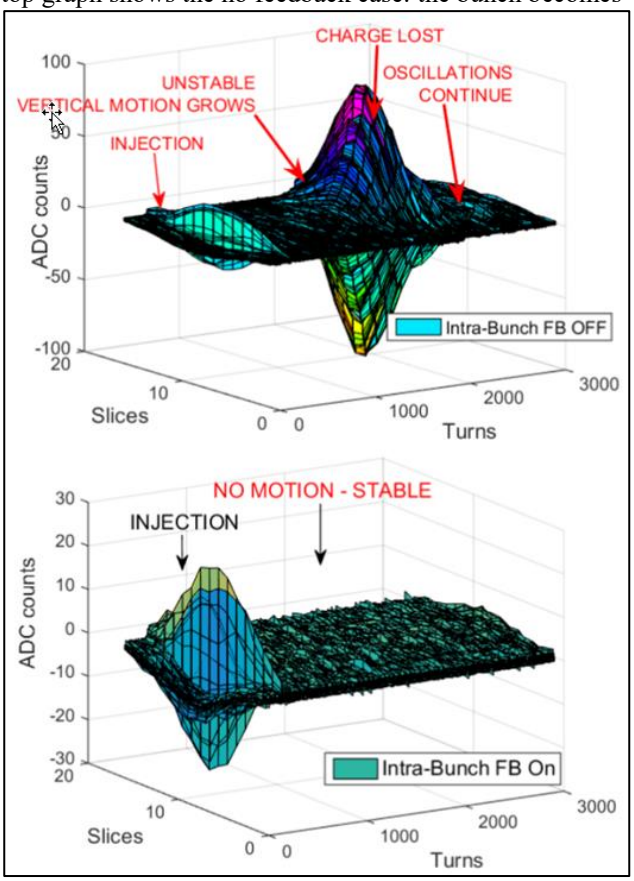

Figure 4: Feedback effect on bunch stability.

unstable after injection, oscillating in mode 0, growing in amplitude, eventually losing charge but still remaining unstable. The second graph shows the same scenario, but with feedback turned on: the bunch injection transient starts to oscillate just after injection, but is quickly damped after approximately 200 turns and the bunch remains stable. Additionally these measurements provide useful data for our simulation and modelling efforts [10].

UPGRADES AND NEXT GENERATION

With the successful demonstration of the WBFB, several upgrades are proposed to enhance performance and usefulness. In addition to the aforementioned DDR memory and Ethernet interface upgrades, we plan on adding an active bunch orbit offset rejection mechanism to extend the dynamic range of the ADC. We plan on upgrading the FPGA motherboard to allow control of the full SPS ring as well as explore different processing algorithms (IIR filter structures, observer based MIMO feedback controllers, etc.). The latter requires extensive matrix calculations which could be implemented using high-level signal processing design tools such as Xilinx System Generator which allows the designer to draw the algorithm in Simulink and compile that into an FPGA block.

Semiconductor technology has improved to the point where it is now possible to increase the system sampling rate to 8GSa/s. This opens up multiple possibilities such as more detailed diagnostics, dual sensor controller architectures, etc. To this end, a prototype 8GSa/s system has been designed similarly using a combination of commercial and custom components. The ADC uses two time-interleaved e2v Inc. EV10AQ190AD 12b, 5GSA/s devices and the DAC device used is a Euvis Inc. MD662H 8GSa/s 12b device. Each data converter device exists on evaluation boards which interface to a commercial Xilinx Virtex-7 FPGA (higher capacity) motherboard. The ADCs require a custom interface board, which has been designed. The PCB fabrication and FPGA development are

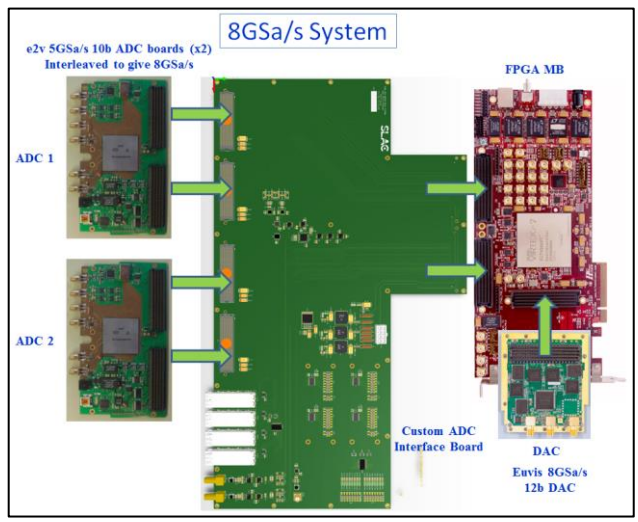

Figure 5: 8GSa/s Prototype System.

awaiting funding to proceed. Figure 5 shows a pictorial view of the 8GSa/s prototype system components.

ACKNOWLEGEMENTS

At CERN, we wish to thank Urs Wherle for his contributions and support in integrating the WBFS into SPS. We thank Hannes Bartosik, Gerd Kotzian, Tom Levens and Kevin Li for their assistance during the recent SPS MDs. At SLAC, we wish to thank Jeff Olsen for developing the VB GUI software and Chuck Yee for his diligence in PCB layout and WBFS chassis design.

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