PRELIMINARY DESIGN OF Mu2E SPILL REGULATION SYSTEM (SRS) *

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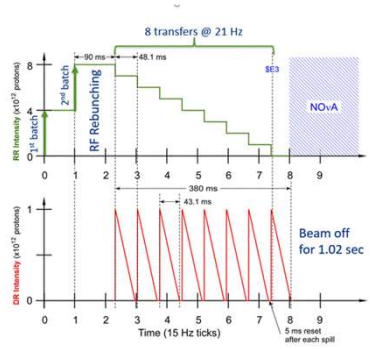
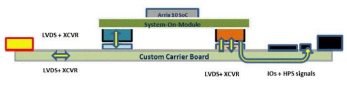
Mu2E Resonant Extraction from the Delivery Ring (DR)

Direct μ→e conversion requires resonant extraction of a stream of pulsed beam. Once the third integer resonant extraction condition is established in the Delivery Ring (DR), a family of 3 zero-harmonic quadrupoles (tune ramp quads) drives the machine tune to the exact resonance, gradually pushing the circulating beam into the resonance stop band. As unstable particles in the stop band drift towards the machine aperture, they get intercepted in the Electrostatic Septum (ESS) and are deflected towards the Mu2e target at the end of the extraction beam line.



Mu2e uses 8 kW of 8 GeV protons from the Booster. Two batches of ~4e12 protons are sent to the Recycler (RR). The batch is divided into 8 2.5 MHz bunches, extracted to the DR, and then slow extracted to the Muon proton target at 590.08 kHz over a 43.1 ms spill period. Dividing the total spill time by the length of the cycle, the spill duty factor is 27.1%



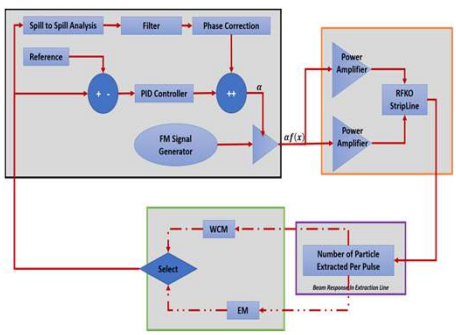
The SRS architecture will be controller board, consisting of the System-On-Module (SoM) and a carrier board. The SoM is a FPGA mezzanine card that hosts the Intel Arria10 SoC. The carrier board provides 16 16bit 650 MSPS ADC channels, 8 14bit 125MSPS DAC, and 4 16bit 200 kSPS DAC channels. The board also has 8 TTL level tolerant Schmidt trigger inputs as well as 16 TTL level, 50 Ω drive capable digital outputs.

Mu2E Spill Regulation System (SRS)

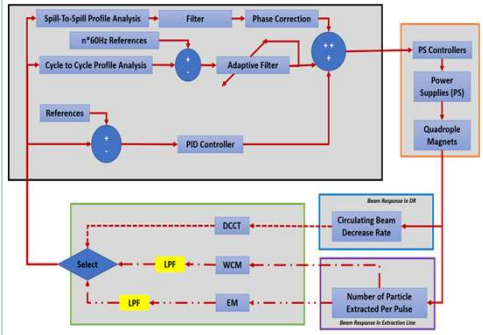
The objective of the Spill Regulation System (SRS) is to maintain the intensity uniformity of a stream of ~25k pulses as 1e12 protons are extracted at 590.08 kHz over a 43.1 ms spill period. The maximum spill variation is required to be <±50%, while maintaining the extraction efficiency at >98%.

The SRS will use two separate PID loops to control two regulation elements simultaneously: : tune ramp quads and a RF Knock-Out (RFKO) system. The SRS requires

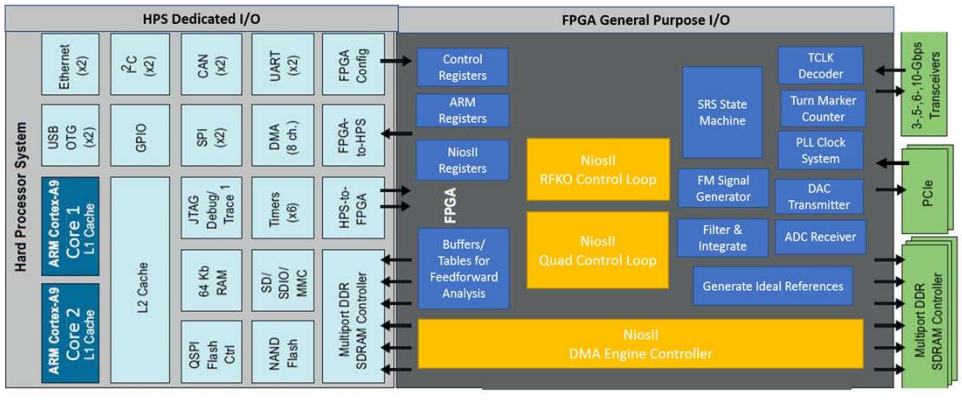
- At least one spill monitor that can resolve on average ~4e7 protons at 10 kHz
- An external clock clock from the Muon LLRF system
- Decoding of predefined machine TCLK and Beam Sync (BS) timeline events
- The Muon campus turn marker, which will be aligned with the bucket 0 of the DR.



The SRS will generate the RFKO's FM excitation signal, whose carrier frequency is tracking the current betatron sideband. Furthermore, the SRS's RFKO Control Loop will regulate the amplitude of this excitation signal.



The SRS will generate the reference ramp curve to the tune ramp quads. This reference determines the average shape of the beam intensity profile during the spill.



Arria10 SoC features a second-generation dual-core ARM Cortex-A9 MPCore processor-based hard processor system (HPS). One ARM Core will be designated for the front-end software application which provides an interface between the FPGA controller and the ACNET control system. The second ARM core of the HPS can be dedicated to calculating cycle-to-cycle feedforward corrections. The HPS and FPGA fabric will be interconnected thru the Platform Designer (formerly Qsys). Each module in the FPGA portion of the SoC can operate concurrently and synchronous to the phase-locked clocks. The data acquisition system (DAQ) is implemented in the FPGA fabric. In addition, the FPGA instantiates multiple NIOSII 32-bit embedded-processors. One configures and controls the modular scatter-gather DMA engines. The other 2 serve as floating-point processors for the regulation controller loops.

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