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APPLICATION OF SOC BASED APPLICATIONS IN THE TPS CONTROL SYSTEM

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Abstract

System on a chip (SoC) based system widely apply for accelerator control recently. These system with small footprint, low-cost with powerful CPU and rich interface solution to support many control applications. SoC based system running Linux operation system and EPICS IOC embedded to implement several applications. TPS (Taiwan Photon Source) adopts some SoC solutions in control system, includes alarm announcer, RadFET reader, frequency and divider control, power supply control, etc. The efforts for implementing are summarized in this paper.

INTRODUCTION

Using a circuit board to implement functions as a computer is called SBC (single-board computer) [1]. Its applications cover in telecommunications, industrial control, blade and high density servers, and lately laptops and mini-PCs, etc. Duo to the latest generation SoC technology, putting all major functionality into an integrated chip, educational used credit-card size SBC [2] likes the Raspberry Pi (RPi) and Banana Pi (BPi) are highly successful products. The BPi is the latest product of such category with powerful CPU, low power consumption SBC indeed, and the area of circuit board is only as credit card size.

The BPi which design idea is similar to the RPi-style SBC, and it is a fork of the RPi project using different components while maintain compatibility as much as possible. Moreover the BPi is added the functions of SATA interface, infrared transmission, microphone, USB-OTG ports, power button, reset button, etc. Then the BPi has 40-pin GPIO which is compatible with the RPi. The Cortex-A7 SoC as CPU/GPU, DDR3 memory and Gigabit Ethernet connection are applied on the BPi. The hardware specification of BPi is shown as Table 1 [3]. Linux-based operation system can be worked well on the BPi.

Table 1: Hardware Specification of the Banana Pi

	Banana Pi M2+/M2U/M3
CPU	Coretx-A7 H3 Quad-core 1.2GHz Coretx-A7 R40 Quad-core 1.5GHz Cortex-A7 A83T Octa-core 1.8GHz
Memory	1GB DDR3 RAM / 2GB DDR3 RAM
Network	1Gbps Ethernet RJ45, Wi-Fi
Storage	MicroSD card slot (up to 64GB), eMMC (8GB onboard) Extensible with SATA interface
I/O	GPIO, UART, I²C bus, SPI bus, PWM, +3.3V, +5V, GND
OS	Debian, Ubuntu, Android ...

The TPS control system of 3 GeV synchrotron light source is also based on the EPICS framework [4]. The EPICS toolkit provides standard tools for display interfaces creation, archiving, alarm handling, etc. Big success of EPICS is based on the definition of a standard IOC (Input Output Controller) structure together with an extensive library of driver software for a wide range of I/O cards. The EPICS framework which has various functionalities is employed to monitor and to control on embedded applications of accelerator system.

BANANA PI AS EPICS IOC

Stability and performance of Banana Pi (BPi) are enough as the EPICS IOCs for specific control applications. The EPICS framework can be built on the Linux-based BPi successfully [5]. Some control functions are implemented by use of the BPi platforms with EPICS support. The efforts of implementation are summarized as followings.

Software Architecture

To implement the BPi as the EPICS IOC for specific control applications, the EPICS base and modules are necessary to be set up on the BPi platform which operation system is the Debian or Ubuntu Linux. The device driver of SPI (Serial Peripheral Interface) bus is built for communicating with DAC/ADC modules, and the device support interface is also developed as the glue between the EPICS records and device drivers. The EPICS records support are created according to the specific functions. The EPICS archive server is set up to record various parameters variations for long time observation. The operation interfaces are created by used of the EDM, CS-Studio, etc. to control and monitor via PV (Process Variable) channel access, and the archived data can be retrieved with using a form of graphical representation of the CS-Studio based data browser. The schematic is shown as Fig. 1.

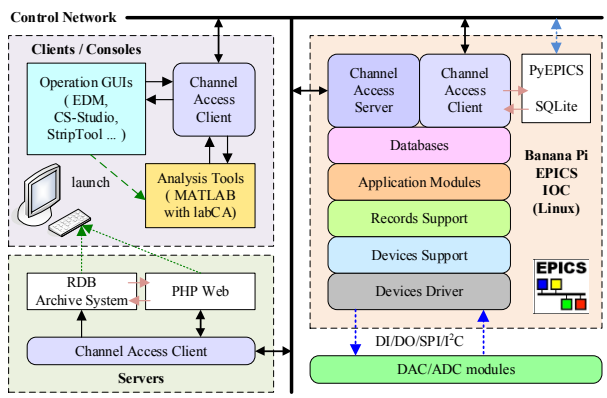

Figure 1: Software architecture of the BPi within EPICS support.

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Alarm Announcer

During the TPS commissioning and operation phases, the abnormal status may occur from one of sub-systems, and operators need to find out which sub-system problem happened from machine interlock interface. Due to many interlock signals need to be noticed, the sum signals of each interlock signals are necessary. According to the abnormal sum signals, the specific alarm message to be trigged and shown in the GUI. Then the BPi is used as the EPICS IOC to receive the request, and alarm announcement voice is sent to loud speaker for noticing. The system schematic is shown as Fig. 2.

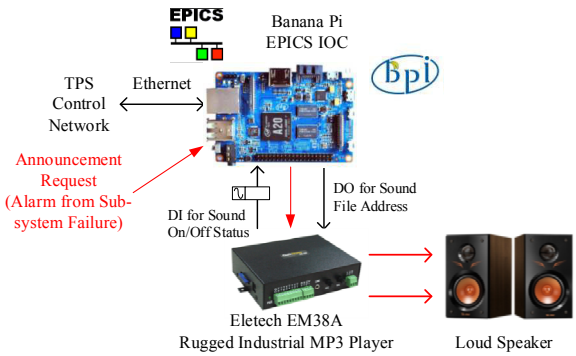

Figure 2: Block diagram of alarm announcer.

Direct Digital Synthesizer Control

To make possibility of different RF frequency without a similar multiplication factor work for linear accelerator (Linac) and booster synchrotron to optimize machine performance without adjust too many parameters in Linac system, a RF signal generator direct digital synthesizer (DDS) which can synchronize at injection instance have been implemented. Functional block diagram of the prototype is shown in Fig. 3. The BPi EPICS IOC is used to control the DDS to achieve goal. Synchronization is achieved to reset the phase of the DDS just before booster synchrotron injection to ensure constant phase relationship between RF system of Linac and booster synchrotron. Fig. 4 shows the prototype DDS signal generator. The RMS jitter of implemented DDS signal output is 0.3 picosecond approximately.

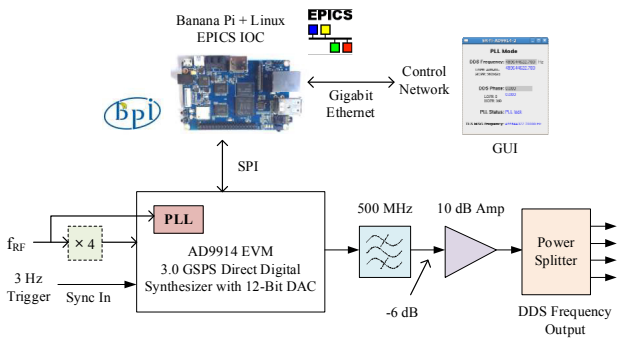

Figure 3: Block diagram of the DDS control.

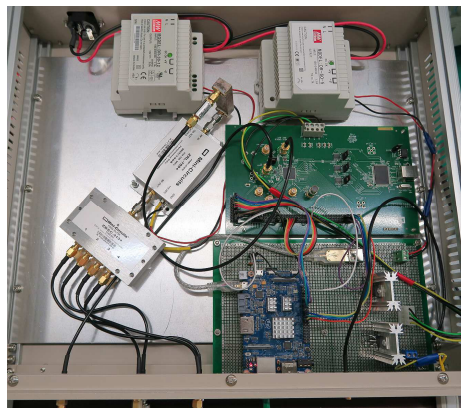

Figure 4: Photo of the DDS signal generator.

Programmable Frequency Divider

Machine clock of the accelerator system generated discrete fast logic chip (ECL/PECL) or combined of fast logic and field programmable logic array (FPGA) usually. Typical jitter is in a few picoseconds order. The programmable clock generator has been implemented by using the AD9508 clock and delay generator to generate clock with 100 femtosecond jitter for some applications (laser clock, filling pattern measurement timing, etc.). The system schematic is shown as shown in Fig. 5. The chip divider and delay parameters can be controlled by use of the BPi EPIC IOC via SPI interface. The implementation is shown as in Fig. 6.

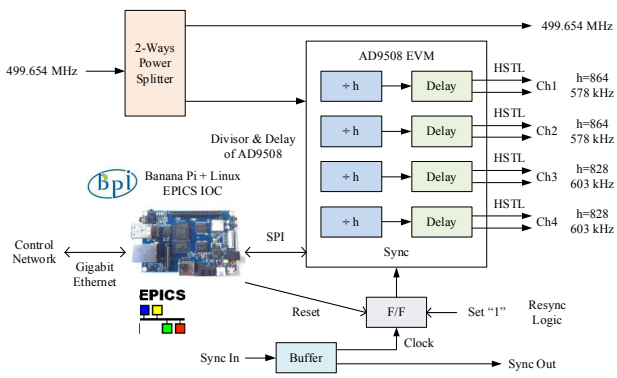

Figure 5: Block diagram of the programmable clock generator.

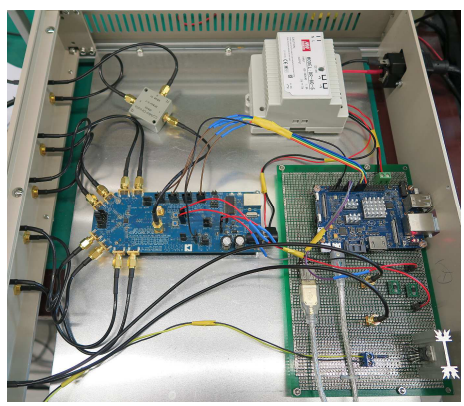

Figure 6: Photo of the frequency divider unit.

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RadFET Reader

To investigate the beam loss and its distribution during commissioning and operation phases of TPS and TLS (Taiwan Light Source), a sixteen-channel readout box was initially designed and implemented to read the threshold voltage of the RadFETs (radiation-sensing field-effect transistor) which were installed at accelerator tunnel [6]. The initial version design was that the reader plays a role of remote I/O for the EPICS IOC and the IOC collects voltage from readers distributed at the accelerator to deduce the integrated dose and dose rate.

The next version design is that the EPICS IOC will be embedded into the RadFET reader box. The BPi will be also adopted as the EPICS IOC for collecting the threshold voltage of the sixteen-channel RadFETs. The data transmission time between the IOC and SPI bus with ADC modules will be improved.

The EPICS IOC performs data acquisition, calculation, and publishes the specific EPICS PVs of dosage. Dosage rate is calculated by the EPICS record processing. All of the threshold voltage values based on EPICS PVs channel access can be recorded into the archive server for further off-line data processing. The MATLAB toolkit can be also used to analyze the RadFET threshold voltage archived data which retrieved from the RDB archive system directly. The control system also provides on-line display for virtualization usage. The system schematic of RadFET reader is shown as Fig. 7. The test prototype of RadFET reader with the BPi EPICS IOC is shown as Fig. 8.

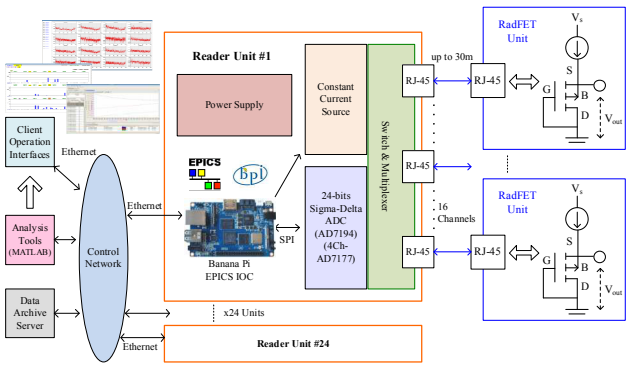

Figure 7: Block diagram of the RadFET readers system.

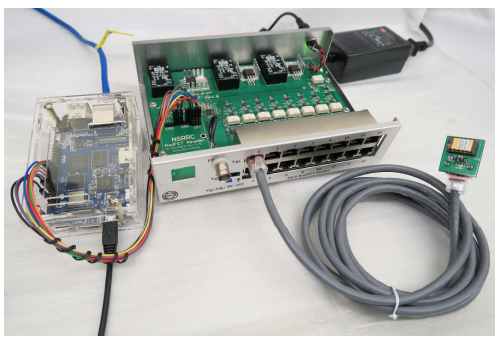

Figure 8: Prototype of the 16 channels RadFET reader with BPi EPICS IOC.

Corrector Power Supply Control

The small power supply for TPS corrector magnet is a sophisticated switching power supply with analogic regulator. Each power supply sub-rack accommodates up to eight power supply modules in one crate. The middle slot is allocated to install an interface card for controlling eight power supply modules. The CPSC (Corrector Power Supply Control) is therefore dedicatedly designed and also embedded the EPICS IOC. The existing CPSC provides general control, monitor and configuration, built-in waveform, synchronization mechanism, and orbit feedback which embedded by FPGA for handling fast update application [7].

New plan for another CPSC with basis control function has been developed. One 8-channel 18-bit ADC and four 2-channel 18-bit DAC modules is used, and interfaced with the BPi via SPI bus communication. The BPi EPICS IOC can reach to handle 100Hz data rate of 8-channel ADC. This system architecture and performance are under tuning. Functional block diagram of CPSC-lite is shown in Fig. 9. The functions of CPSC-lite are under testing, and the prototype is shown in Fig. 10.

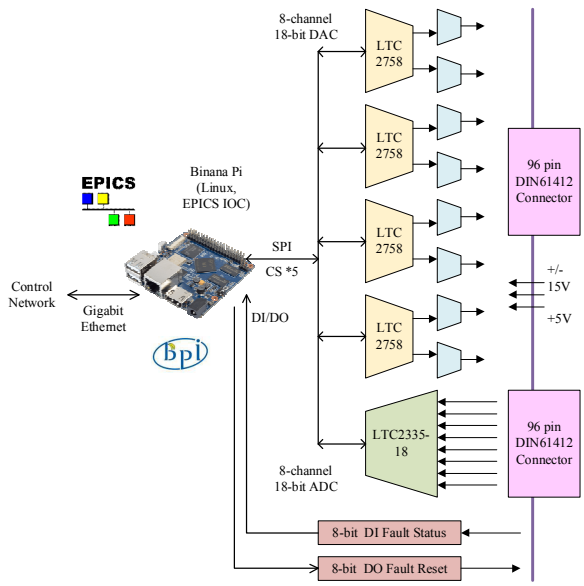

Figure 9: Block diagram of the CPSC-lite.

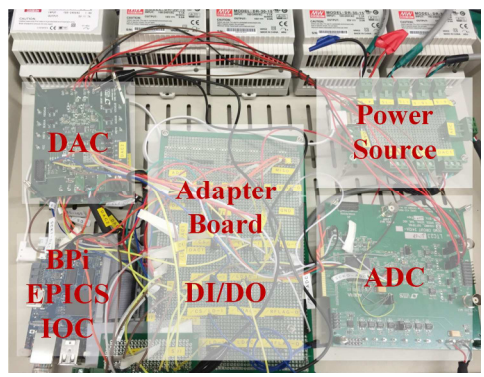

Figure 10: Prototype validation of the corrector power supply control.

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SUMMARY

SoC based system is widely adopted for educational purpose and also suitable for small scale embedded applications. The BPi is a kind of SoC based system. The BPi has been chosen for several applications at the TPS control environment as auxiliary supports which are not suitable to use standard platform in existed control system due to economics, simplicity, speciality viewpoints. More applications with SoC based system will be explored and implemented in near future.

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