

# **APPLICATION OF SOC BASED APPLICATIONS IN THE TPS CONTROL SYSTEM**

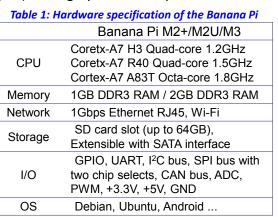
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## Abstract

System on a chip (SoC) based system widely apply for accelerator control recently. These system with small footprint, low-cost with powerful CPU and rich interface solution to support many control applications. SoC based system running Linux operation system and EPICS IOC embedded to implement several applications. TPS adopt some SoC solutions in control system includes, alarm announcer, RadFET reader, frequency and divider control, power supply control, etc. The efforts for implementing are summarized in this paper.

## Introduction

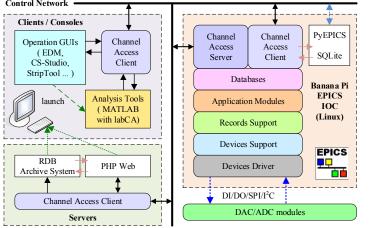
- Duo to the latest generation SoC technology, putting all major functionality into an integrated chip, educational used credit-card size SBC likes the Raspberry Pi (RPi) and Banana Pi (BPi) are highly successful products.
- BPi which design idea is similar to the RPi-style SBC, and it is a fork of the RPi project using different components while maintain compatibility as much as possible.
- Hardware specification of BPi is shown as Table 1. Linux-based OS can be worked well on the BPi.



# **Banana Pi as EPICS IOC**

## Software Architecture

- To implement the BPi as an IOC, the EPICS base and modules are necessary to be set up on the BPi platform with the Debian or Ubuntu Linux.
- Device driver of SPI (Serial Peripheral Interface) bus is built for communicating with DAC/ADC modules, and the device support interface is also developed as the glue between the EPICS records and device drivers.
- EPICS records support with databases are created according to the specific functions. Control Network

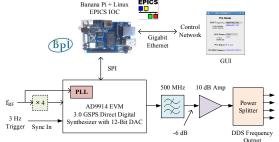


Software architecture of the Banana Pi with EPICS support.

# Embedded Applications with EPICS Support

#### **Direct Digital Synthesizer Control**

To make possibility of different RF frequency for linear accelerator (Linac) and booster synchrotron, a RF signal generator direct digital synthesizer (DDS) which can synchronize at injection instance have been implemented.



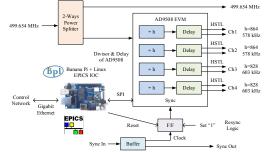


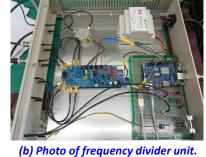


## Programmable Frequency Divider

(b) Photo of prototype DDS signal generator.

Programmable clock generator has been implemented by using the AD9508 clock and delay generator to generate clock with 100 femtosecond jitter for some applications (laser clock, filling pattern measurement timing, etc.).

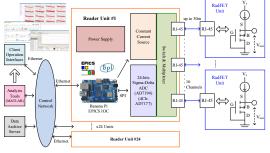




(a) Block diagram of programmable clock generator.

#### RadFET Reader

- To investigate the beam loss and its distribution, a sixteen-channel readout box was implemented to read the threshold voltage of the RadFETs (radiation-sensing fieldeffect transistor) which were installed at accelerator tunnel.
- Next version design is that the EPICS IOC will be embedded into the RadFET reader box for collecting the threshold voltage of each channel RadFET. The data transmission time between IOC and SPI bus with ADC modules will be improved.



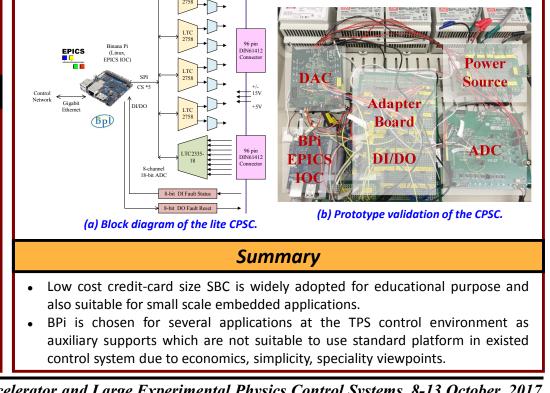


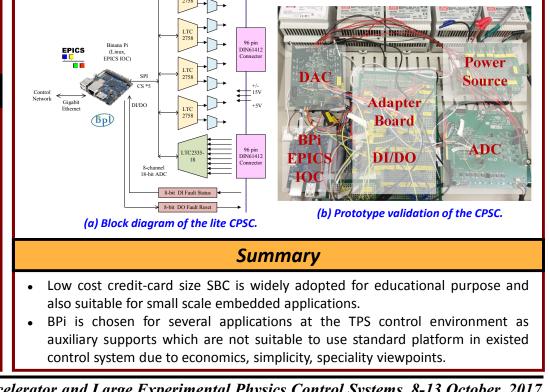
(b) Photo of the prototype 16 channels RadFET reader with BPi EPICS IOC.

(a) Block diagram of the RadFET readers system.

## **Corrector Power Supply Control**

New plan for another CPSC for basis corrector power supply control has been developed.





# **Embedded Applications with EPICS Support**

#### Alarm Announcer

Due to many interlock signals need to be noticed, the specific alarm message to be trigged and shown, and the BPi is used as the EPICS IOC to receive the request and send alarm announcement sound to loud speaker for noticing.





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