NEW CONTROLLER FOR HIGH VOLTAGE CONVERTER MODULATOR AT SPALLATION NEUTRON SOURCE

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Abstract

The Spallation Neutron Source (SNS) has developed a new control system for the High Voltage Converter Modulator (HVCM) at the SNS to replace the original control system which is approaching obsolescence. The original system was based on controllers for similar high voltage systems that were already in use [1]. The new controller, based on National Instruments' PXI/FlexRIO Field Programmable Gate Array (FPGA) platform, offers enhancements such as modular construction, flexibility and non-proprietary software. The new controller also provides new capabilities like various methods for modulator pulse flattening, waveform capture, and first fault detection. This paper will discuss the design of the system, including the human machine interface, based on lessons learned at the SNS and other projects. It will also discuss performance and other issues related to its operation in an accelerator facility which requires high availability. To date, 73% of the operational HVCMs have been upgraded with the new controller, and the remainder are scheduled for completion by mid-2017.

MOTIVATION

The original HVCM control system was comprised of several supporting commercial, off-the-shelf and custom components integrated in a custom rack to control the HVCM and provide equipment protection. Most of the equipment is from the original design, but modifications were incorporated based on operational experience to enhance protection, improve performance, and provide more user feedback. These upgrades were limited by the original, proprietary firmware and offered limited measurement and control capability. The lack of integrated data acquisition and access to all possible faults on the HVCM made troubleshooting difficult, forcing the use of asynchronous oscilloscopes to acquire relevant data.

Local interface to the PLC-based controller utilized the Allen Bradley PanelView system, offering limited functionality and a user interface that left much to be desired. A new, PXI/FlexRIO FPGA based controller was purposefully designed for the HVCMs at the SNS and built to simplify the entire system by combining the PanelView, original controller, PLC, Dynamic Fault Chassis, Remote SCR Control Head, and oscilloscope functions into one unit.

New Controller Requirements

In the design process, the new controller's role was expanded to not only replace the existing equipment's functionality, but to provide more features that helped protect and optimize the HVCM operation. To that end, a list of requirements emerged including 32 channel synchronized waveform monitoring and capture at a rate of 50 megasamples per second, first fault detection and logging, and the ability to individually set analog fault and warning thresholds overlaid on live data waveforms.

Dynamic timing settings were included in the requirements, as well, allowing such functions as Phase Shifted Pulse Width Modulation (PSM), Frequency Modulation (FM), Pulse Width Modulation (PWM), and Flux Compensation for individual Insulated Gate Bipolar Transistors (IGBTs) timing pulses. PSM, PWM and FM are all techniques that can be used to flatten the modulator's high voltage output pulse by controlling the amount of energy delivered to the load through the H-bridge IGBTs [2]. In PSM, one half of the H bridge drive signals are fixed while the other half's phase is changed on an individual pulse basis over the duration of the macro pulse. In PWM the entire H-bridge changes pulse width over the duration of the macro pulse (Fig. 1). When using FM, the individual IGBT gate drive frequency is varied over the macro pulse to achieve flattening. In addition, smarter logic controls IGBT start pulse gating to control pulse rise-time, shape, and to ensure transformers do not saturate during operation. The above listed attributes along with high-reliability, modular configuration, and pliability for expansion were considered essential components for any new controller design.

DESIGN

Many of the design cues were taken from operational experience with the HVCMs, the desire to eliminate the limitations of the original control system, and the engineer's previous experience in projects designed for military application. In particular, the use of warning and trip thresholds were incorporated to assist in identifying developing problem areas.

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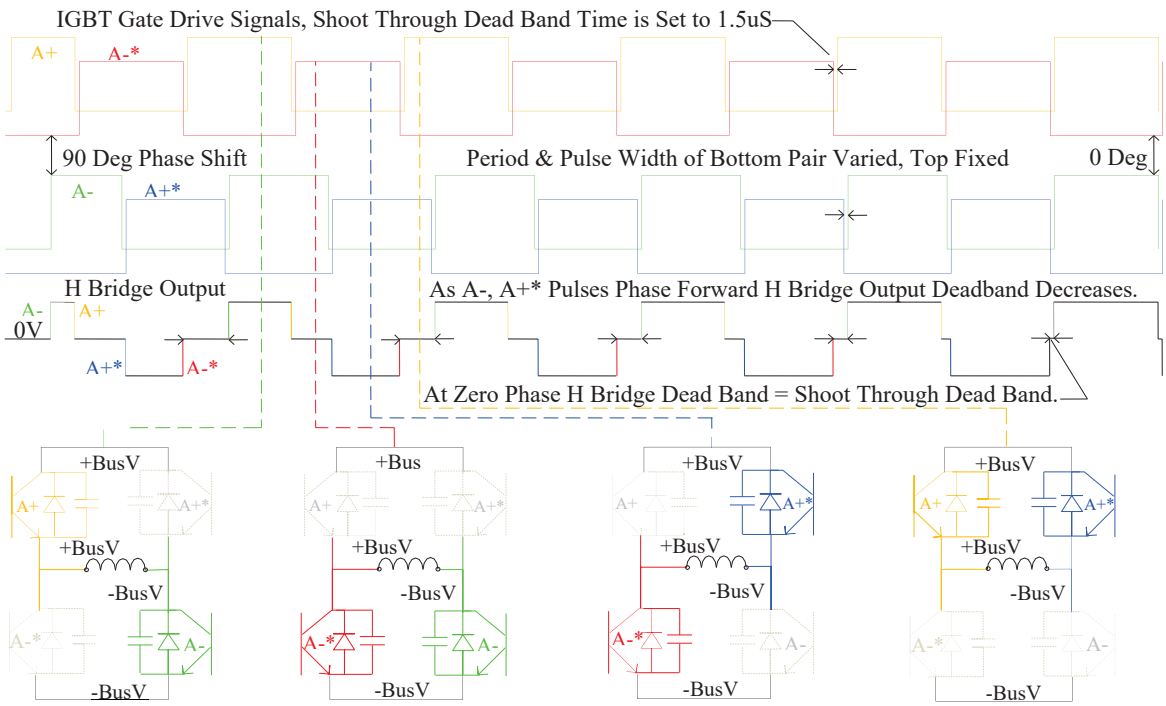

Figure 1: Timing system layout interaction in Phase Shifted Pulse Width Modulation Mode.

Hardware

The PXI platform from National Instruments was chosen as the basis of the design because it utilizes an industry standard chassis with modules that are available from multiple sources. As such, it is considered sustainable and expandable. The PXIe chassis, controller, and modules were selected to provide the highest available bandwidth at the time this project began. The hardware implemented is as follows:

- NI PXIe 1082 – 8 slot 3U PXI Express chassis with 7 GB/s system bandwidth.
- NI PXIe 8135 – 2.3 to 3.3 GHz i7 embedded controller with 8 GB/s bandwidth.
- 2 NI PXIe 7962R FlexRIO FPGAs with 512 MB onboard RAM.
- 2 NI 5751 50 MHz digitizers.
- 1 NI PXIe 6674T timing module.
- PXI 7842R multifunction FPGA

Custom analog and digital signal interface chassis were designed to buffer, protect, and provide adjustable gain to the I/O signals. A re-designed SCR interface chassis replaced the previous antiquated, unreliable hardware that included digital meters and a PLC. The new human-machine interface for the entire system is a rack mounted keyboard/mouse combo along with an LCD monitor.

The new HVCM controller uses pure LabVIEW implementation of EPICS Channel Access protocol developed at SNS [3,4]. This implementation doesn't use any native EPICS libraries and is expected to work on all LabVIEW platforms supporting network stack (tested on Windows and LabVIEW RT). Since it is not a standard IOC implementation, no record programming is available and all business logics is handled by LabVIEW application. The same interface is used in numerous beam instrumentation devices at the SNS accelerator.

System Features

The new HVCM interface Status Screen provides an overview of the system and gives status of crucial signals, fault indications, fault logs, and top level waveforms for quick diagnosis (Fig. 2). At this level, one can easily place the HVCM in its default operating mode, choose modulator voltage regulation, or change it to run in other regulation modes. The modulator can also operate in single phase mode, isolating a particular phase from the others to make diagnosing problems easier.

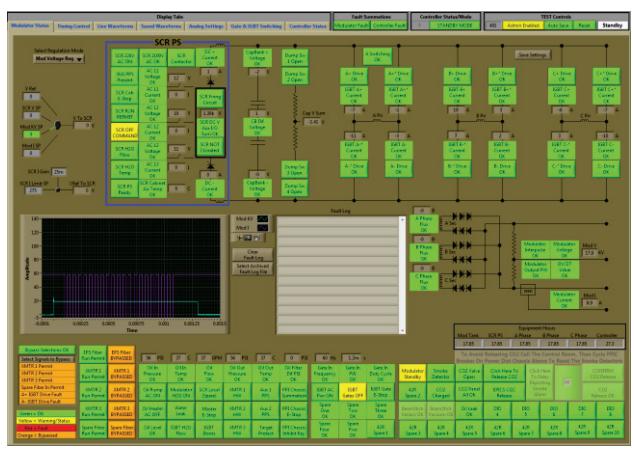

Figure 2: HVCM Status Screen.

Using the timing control screens, the user can control IGBT timing to implement phase-shifted pulse width modulation, frequency modulation, pulse width modulation, flux compensation, and change the start pulse settings for individual phases (Fig. 3). From the same screen, flux and voltage signals can be displayed to see the real-time effects of the different modes (Fig. 4).

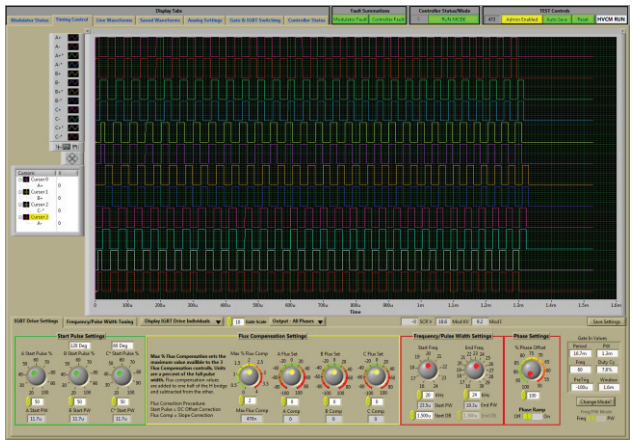

Figure 3: Timing control for PSM/FM/PWM and flux compensation.

Live waveforms can be displayed on yet another screen with threshold adjustments readily available to the user to set the appropriate level either before or during runtime. Snapshots of machine state can be taken during runtime and are saved for further analysis in a comma-separated value file. Similarly, if a fault occurs, two files are generated; one captures the last three pulses, and the other zooms into the problem area with higher resolution. In both cases, these files can be viewed directly in the LabView environment and the waveforms can be adjusted to allow the user easy interpretation of the data (Fig. 4). We also devised a method for the user to remotely view the generated files and analyze the faults in a timely fashion. The files are opened in a decimated executable form of the full LabView program to provide an environment consistent with the full program's experience.

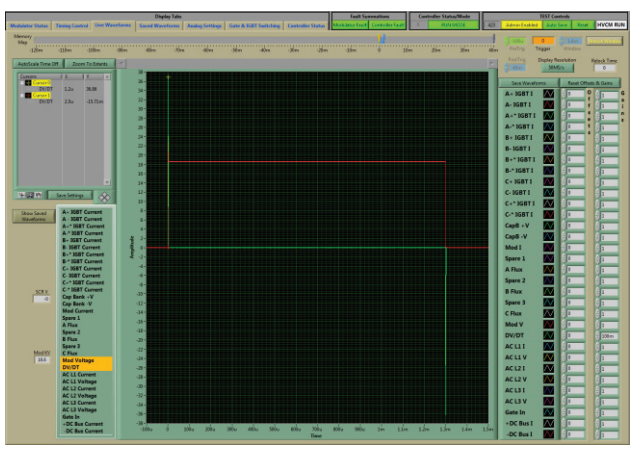

Figure 4: Live waveforms screen.

The Analog Settings screen is a real-time display of waveforms with the ability to set warning and fault thresholds, which are shown overlaid on the waveforms for clarity. These signals are separated into logical family groups for ease of access and to simplify the display.

Operational Experience

The first controller was installed on the HEBT development modulator around five years ago where pulse flattening using both Phase Modulation and Frequency Modulation had been successfully demonstrated over several 100+ hour full power runs. To date, the controller has been installed on eleven production HVCMs and is slated to be installed on four more by mid-2017. The two test HVCMs that are running the program provide a test stand for continued improvement to the code and testing in real world situations. A separate test stand for controllers is slated to be installed in 2017. This will provide for ready spares which are networked and updated along with operational units.

CONCLUSION

As of March 1st, 2017 we have logged 14,547 hours of uptime on the oldest installed production controller, and over 16,300 hours on the HEBT development modulator have been logged. The new capabilities offer unprecedented control of the HVCM systems and opportunities for future modifications are possible based on the software and firmware platforms.

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