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LOW-LEVEL RF SYSTEM FOR THE CHINESE ADS FRONT-END DEMO LINAC

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Abstract

The Chinese ADS Front-end Demo Linac (FDL) is constructed to demonstrate the technology of superconducting linac with high proton beam loading of CW 10mA. The low-level RF (LLRF) control system for the ADS FDL is developed by IMP, and the cooperation with TRIUMF. In the normal conducting (NC) section, the normal RF feedback control loop is used. In order to stable the superconducting (SC) cavity with loaded high RF power, the self excited loop with phase locked mode was used on the SC linac. This paper introduces the LLRF control system for buncher, SC linac, and the structures of hardware and the functions of software of these LLRF systems. The operating status of the LLRF systems is also reported.

INTRODUCTION

Figure 1 shows the ADS FDL facility installation diagram, it is designed to accelerate proton beam to 25MeV with beam current up to 10 mA, this accelerator system includes a proton ECR ion source, a low energy beam transport line, a 2.1MeV room-temperature RFQ, a MEBT, a superconducting radio frequency linac system, and this proton accelerator operated in continuous-wave mode. The amplitude and phase stability of all RF resonant cavities need to be controlled precisely by the LLRF control system.

THE LLRF CONTROL SYSTEM FOR BUNCHER

The LLRF control system which used to control buncher cavity is developed by IMPCAS. Figure 2 shows the system architecture of one LLRF system, this system consists of cavity amplitude and phase controller, and the cavity resonance frequency tuning controller. The operating frequency is 162.5 MHz. The system is an all-digital closed-loop feedback control system and based on the IQ quadrature sampling demodulation technique [1].

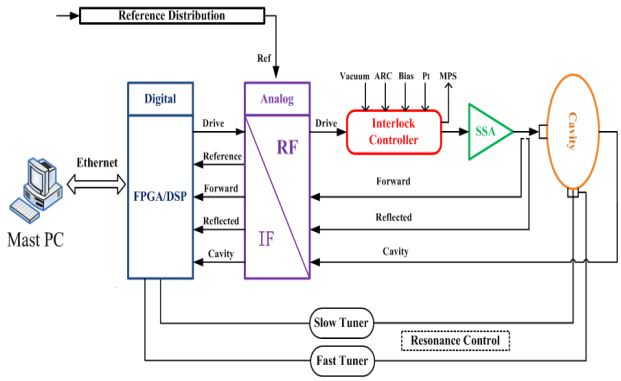

Figure 2: The LLRF control system for Buncher.

System Hardware

The LLRF system for buncher includes amplitude, phase, and frequency feedback loops. It uses digital control technology based on FPGA.

The LLRF system is composed of two layers of hardware. The bottom layer contains the power supply module, an AD9858 direct digital synthesizer board, an AD9510 clock distribution board, an ADC sample daughter board, and a digital signal processing FPGA board. The top layer is an RF modulated front end composed of commercial components.

The buncher LLRF system realized RF up-conversion and down-conversion by mixer on hardware, this system adopted AD9254 of 14-bit resolution, an analog-to-digital conversion chip, the maximum conversion speed of AD9254 can reach to 150 MSPS. It also adopted DAC56721 of 14-bit resolution, a digital-to-analog conversion chip, with 275 MSPS conversion speed of maximum. The AD9858 generates 30.72MHz as an intermediate frequency while the AD9510 generates 122.88 MHz as a clock[2].

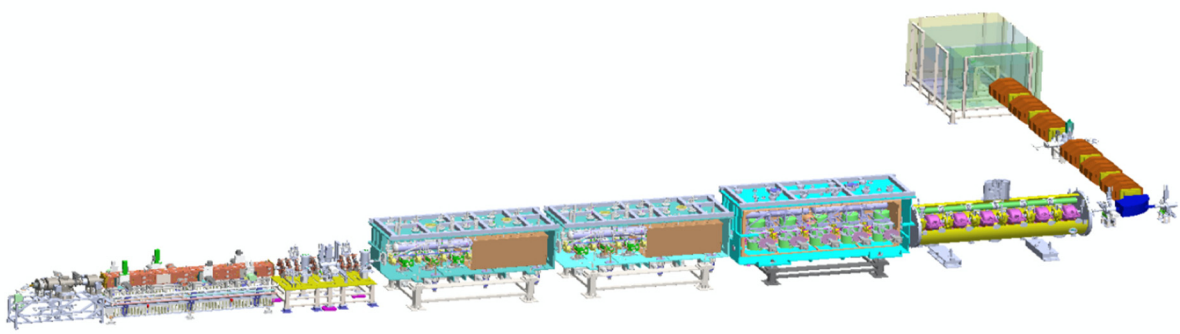

Figure 1: The layout of ADS FDL.

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These signals are assigned to the FPGA, AD, and DA blocks. Figure 3 shows 162.5 MHz buncher LLRF system block diagram.

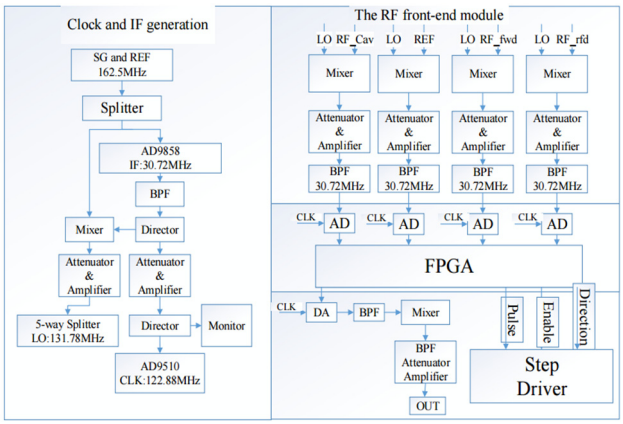

Figure 3: LLRF block diagram of buncher.

In the block diagram of Fig. 3, the local oscillator (LO) signal mixed with the RF signal to obtain an intermediate frequency (IF) signal of corresponding. The signals that need to be controlled and monitored including the cavity RF pick-up signal, the RF forward and reflected signal from directional coupler, and the RF reference signal. The four-channel ADC samples the corresponding IF signal and sends them to FPGA for processing. Then output RF signal and motor control signal.

Operation Result

This buncher LLRF system had been successfully applied on ADS FDL. The maximum error of amplitude and phase respectively are 2.7% and ±0.32 degree, which is shown in Fig. 4 and Fig. 5. It meets the design requirements.

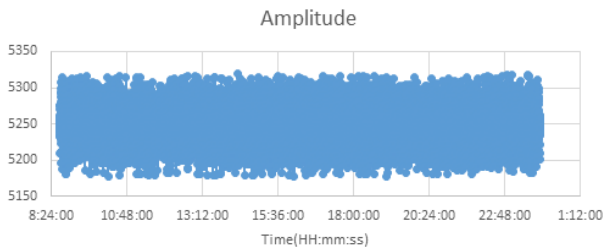

Figure 4: Amplitude error: 2.7%.

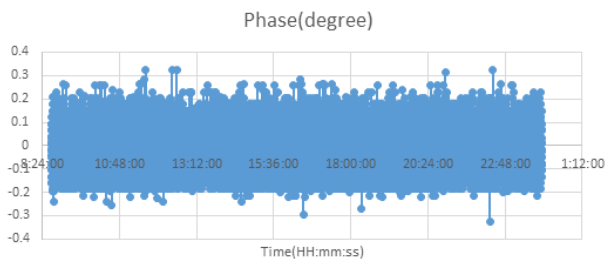

Figure 5: Phase error: ±0.32°.

THE LLRF CONTROL SYSTEM FOR SC LINAC

The LLRF control system for superconducting cavity is developed by cooperation with TRIUMF. A block diagram of the RF control system is presented in Fig. 6. The Superconducting cavity's LLRF system primary function is amplitude and phase locking. Instead of operating in driven mode, this system now operates in self-excited mode, where the self-excited frequency is determined solely by the loop phase. This frequency is locked to an external reference by regulating the phase shift within the self-excited loop, capable of operating in both CW and pulse mode [3].

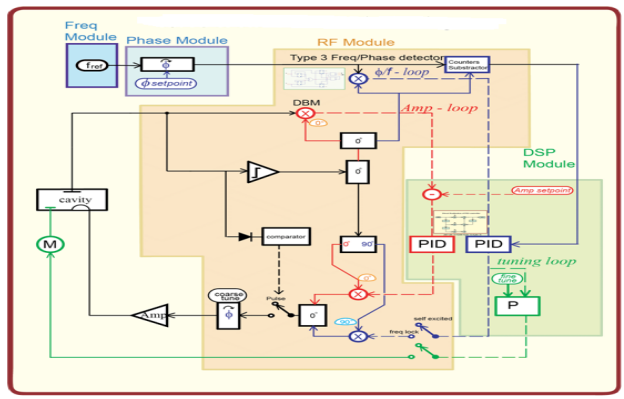

Figure 6: The block diagram of SC LLRF.

System Hardware

These LLRF systems are housed in a VXI mainframe, and used for RF control of HWR010 superconducting cavities. The system consists of two main parts: The first is RF Module, where the RF signal are processed and converted into baseband. The second is DSP Module, where the baseband signal is converted into digital form and processed by a pair of Digital Signal Processors, then re-converted back into an analogue form for modulation by the RF module.

The other RF control system hardware is a rack-mounted PC, which provides supervisory control and data acquisition. Communication between the PC and the VXI mainframe is done via a FireWire (IEEE 1394) interface. In the VXI mainframe, a VXI slot zero control module, the RF module, and the DSP module are housed. These function together to provide three main regulation loops: the amplitude loop, the quadrature phase/frequency loop, and the tuning loop. As seen in Fig. 6, the primary amplitude detector is a synchronous demodulator, in which an internal PLL supplies an amplitude-stabilized reference to be multiplied with the RF input. The product is filtered, sampled and digitized at 40k samples/sec and processed by a Motorola DSP56002DSP. The DSP is configured as a Proportional-Integral controller, providing amplitude regulation.

Other diagnostic instruments not shown in the figure include forward and reflected power meters, a frequency counter and oscilloscopes. These instruments are used to measure the accelerating field and Q of the cavity.

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Software and Operation

There are two main functions of the system software: control of the superconducting cavity, data acquisition and calculation [4]. In order to achieve the purpose of controlling the cavity, the low level feedback control was used to open and close loop regulation. The host computer interface can monitor the information of cavity, and then adjust cavity amplitude and phase according to the feedback information. For data acquisition, communication between the PC and the central control system is done via 100BaseT Ethernet, and computer can access the data server and request data from the control processor. Figure 7 is the local control interface which is written by C++.

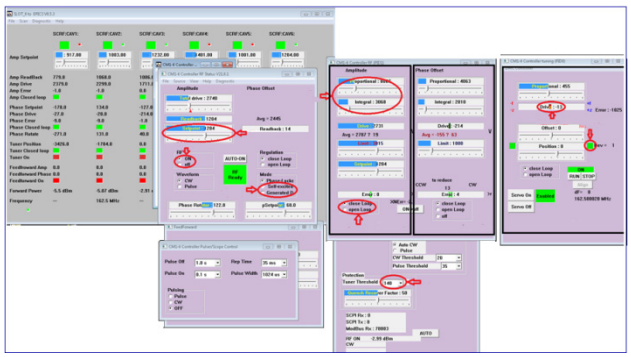

Figure 7: The local control interface.

The target of cavity RF control is to keep the amplitude, phase and frequency stable. The prerequisite of SC cavity control is that the protection system needs to work properly. The RF power loading of SC cavity has two modes: the Generator Driven (GD) mode and the Self Excited (SE) mode. The GD mode is suitable for cavity RF test. It needs manu-tuning for resonance tracking. The Self Excited mode is suitable for high power loading. The local control interface is useful for us to control RF cavity. Click "Generated D" button choose GD mode, and then adjust "Limit", "Drive" button to set the largest drive value to protect equipment. According to the vacuum, it's necessary to adjust the frequency of cavity and the duty cycle of pulse. The SE mode can auto-lock the cavity frequency during the power loading until the needed Epk value is reached. Then the SE loop will lock the phase with the reference signal.

In order to easy control for machine operator, the simplified operator interface shown in Fig. 8 is provided by using the Epics CSS (Control System Studio).

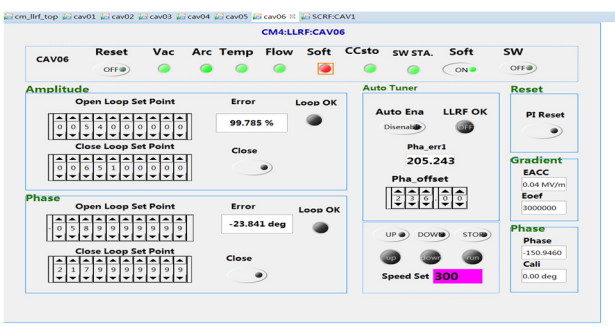

Figure 8: The simplified operator interface.

Operation Result

The SC LLRF system was successfully tested with HWR 010 cavities. The maximum error of amplitude and phase respectively are 5‰ and ±0.5 degree. The operation results were shown in Fig. 9.

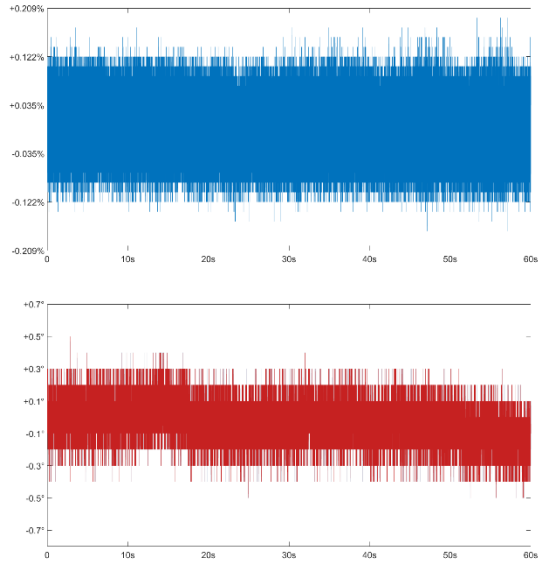

Figure 9: The amplitude (a) and phase error (b) of SC LLRF.

SUMMARY

The Chinese ADS FDL has successfully accelerated 12 mA (@ 26 MeV) pulse and 0.3 mA (@ 25 MeV) CW beam. The beam commissioning results also demonstrate that the LLRF control system can maintain stable operation.

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