FRIB FAST MACHINE PROTECTION SYSTEM: ENGINEERING FOR DISTRIBUTED FAULT MONITORING SYSTEM AND LIGHT SPEED RESPONSE *

Z.Y. Li †, B. Dalesio, L. Wang, M. Ikegami, S.M. Lidia, S. Zhao, Facility for Rare Isotope Beams, East Lansing, Michigan, USA

Abstract

The Facility for Rare Isotope Beams (FRIB), a high-power, heavy ion facility, can accelerate beam up to 400 kW power with kinetic energy ≥ 200 MeV/u. Its fast protection system is required to detect failure and remove beam within 35 µs to prevent damage to equipment. The fast protection system collects OK/NOK inputs from hundreds of devices, which are distributed over 200 m. The engineering challenge here is to design a distributed control system to collect status from these devices and send out the mitigation signals within 10 µs timing budget and also rearm for the next pulse for 100 Hz beam (10 ms). This paper describes an engineering solution with a master-slave structure adopted in FRIB. Details will be covered from system architecture to FPGA hardware platform design and from communication protocols to physical interface definition. The response time of ~8µs from OK/NOK inputs to mitigation outputs is reached when query method is used to poll the status. A new approach is outlined to use bi-direction loop structure for the slave chain and use streaming mode for data collection from slave to master, ~3µs response time are expected from this engineering optimization.

INTRODUCTION

The Facility for Rare Isotope Beams (FRIB), a high-power, heavy ion facility, can accelerate beam up to 400 kW power with kinetic energy ≥ 200 MeV/u [1][2][3]. A Machine Protection System (MPS) minimizes component damage and operational interruption caused by both acute (fast) and chronic (slow) beam losses [1]. The fast protection system collects OK/NOK inputs from hundreds of devices, such as low level RF controllers, beam loss monitors, and beam current monitors, which are distributed over 200 m. The engineering challenge here is to design a distributed control system to collect status from these devices and send out the mitigation signals within timing budget, also quickly rearm for the next pulse for 100 Hz beam. This paper describes an engineering solution with a master-slave structure adopted in FRIB. Details will be covered from system architecture to FPGA hardware platform design and from communication protocols to physical interface definition, from system prototype to its function verification test results.

SYSTEM ARCHITECTURE

FRIB MPS [3] displayed in Fig. 1 consists of the FPS network, MPS sensors, MPS mitigation devices, and MPS Input Output Controllers (IOCs) [4]. Run Permit System function is needed to start the beam but is separated from MPS system. Time-critical sensors and mitigation devices are connected directly to MPS network. Non-time-critical sensors are connected to MPS network via aggregation PLCs.

For 100% beam loss at full power, or faults other than beam loss, MPS must turn off the beam in a maximum of 35 µS in order to avoid any severe damage to the machine. Response time of 35 µs is based on Analysis of Beam Damage to FRIB Driver Linac. The allocation of response times for FPS will be determined during commissioning. Design goals are:

- 10 µs for device to detect a failure and to inform MPS network about it (including cable delay)
- 10 µs for MPS network to identify the right mitigation action(s) and to distribute the signal to appropriate output(s)
- 5 µs for mitigation device to receive signal and to execute mitigation action (including cable delay)
- 10 µs for beam mitigation time (residual beam in the accelerator)

FPS consists of FPS master, FPS slaves and fiber patch panels. FPS master is linked with each FPS slave chain with one string of fiber from fiber trunk routed between fiber patch panels. FPS shares the fiber trunks and patch panels with Global Timing System (GTS) and network system.

The FRIB machine offers the following mitigation actions which must be controllable from MPS:

A) Remove high voltage from both front end vertical electrostatic dipoles (E-bends). This mitigation action shall take less than 1 µs.

B) Trip Chopper control system to apply deflector voltage to the chopper in the Low Energy Beam Transport system (LEBT) to stop the beam. This mitigation action shall take less than 1 µs.

C) Disable the ECR ion source extraction high voltage via fiber link. This mitigation action shall take less than 50 ms.

FRIB MPS is designed with four operation states:

- Disabled: Status of MPS sensors is not monitored. Mitigations A and B are activated regardless of the sensor inputs.
- Monitor-only: Status of MPS sensors is monitored. Mitigations A and B are activated regardless of the sensor inputs.

* Work supported by Work supported by the U.S. Department of Energy Office of Science under Cooperative Agreement DE-SC0000661.

† liz@frib.msu.edu

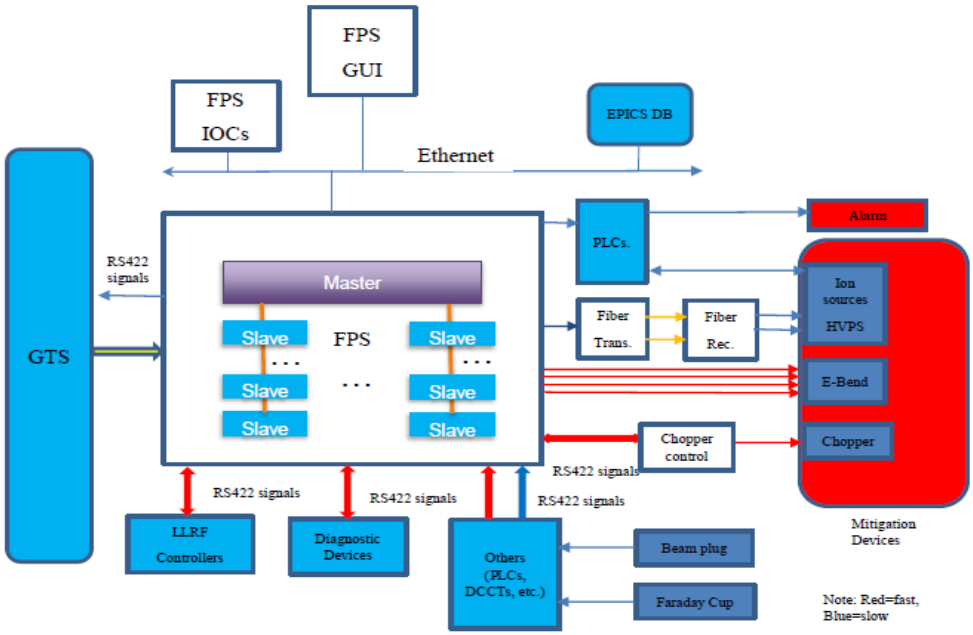

Figure 1: FRIB MPS architecture.

- Enabled: Status of MPS sensors is monitored. All mitigations are deactivated if no NOK signal is detected. Automatically transit to Fault mode upon detecting NOK signal.
- Fault: Status of one or more MPS sensors not masked is latched to NOK. Mitigations A, B, and C are activated.

Here, beam mitigation device is defined as "activated" when it mitigates beam, and "not activated" or "deactivated" while nominal beam operation.

KEY MPS HARDWARE DEVELOPMENT

Displayed in Fig. 2, FRIB General Purpose Digital Board is developed for MPS control board. The core part of the FGPDB is the Spartan-6 FPGA XC6SLX150T-2FGG900C. It's a microTCA.4 standard board with rich extended interfaces. There is 4 Gb DDR3 ram on the board. JTAG and RS232 is supported for debugging FPGA. MCU is the management module controller which is also defined by microTCA.4 standard. FGPDB need only single +12V power supply. It is can work either standalone or in microTCA chassis. For MPS application, FGPDB is placed in the "Pizza" box with an AC to DC power supply, a rear panel board which provides 28 RJ45 ports and GPIO ports, a front panel board which provides 16 RJ45 ports.

Our strategy of MPS master is to develop the master based on FGPDB board first to meet front end commissioning schedule, the master based on KCU105 board will be developed later for Linac commissioning to provide more daisy chains needed for Linac. Firmware of slave and master is developed. Both slave and master firmware have the Micro-blaze system to manage the UDP communication, Flash, DDR3 and the FPS logic to manage the I/O ports, daisy-chain communication, Event Receiver (EVR). The challenge of Firmware development for FPS is to fit the design into the Spartan-6 chip which has only 16 global clocks and solve the timing issues of Clock Domain Crossing (CDC) between GTS clock, Ethernet clock, Daisy chain clocks, I2C clock and system clocks.

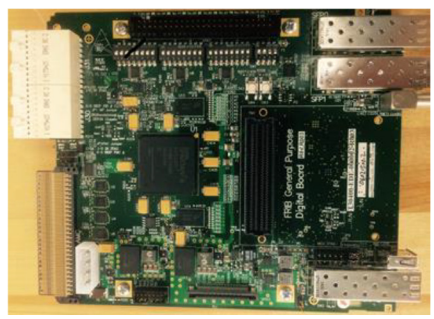

Figure 2: FRIB General Purpose Digital Board, Rev.3.

SYSTEM PROTOTYPE

A MPS system prototype is built for performance demonstration, which includes FPS, Ion source fiber control system, MPS slave and master IOCs and Operator Interface (OPI). The FPS includes one FGPDB based master and one daisy chain of 8 slave nodes. GTS event generator and EPICS network server are connected with FPS. Response time of MPS is measured as displayed in Fig. 3, the daisy chain fiber between master and the first slave is 210 meters, between slaves is 20 meters. Master collects the sensor status from each MPS slave by polling; it queries the daisy chain every 4 μS, slave responses the query with its own data package first, transmits the data from other slaves after which is stored in the FIFO. The data package starts with the sync code first, followed by the start of

frame, slave address, version, master request event code, time stamp, 96 I/O status, check sum and stop of frame. If error get latched in the slave, the time stamp labels the time when error is occurred. Master also sends the slaves the event code to inform the MPS status. The worst case scenario which gives the longest response time is when the last slave of the daisy chain gets the error input from sensor right after I/O status is sent to the master. The test signal is an 8 ns pulse train which starts the first pulse right after I/O status data is sent from the slave, followed by the pulse which is 8ns phase shifted from the previous one and is sent 4.096 ms (1024 query periods) after the query period when the previous pulse is sent. After repeating for 1024 times of above process and it will start from the first pulse again. When Slave 8 receives the test pulse, the error will be latched until one bit of 96 I/O bits is set to fault and transmitted over daisy chain. When master receives the data with fault bit from slave, it will react differently with operation states. If it is in "enabled" state, it will switch to "Fault" state. The fault and time stamp of slave will be latched along with master time stamp which labels when fault bit is received until operation state switches to "Monitor-only". At "Monitor-only" state, master will latch the error until the next slave data is received. The response time is measured with "Monitor-only" state, as displayed in Fig. 4, channel 1 is the accumulated test pulses while oscilloscope is triggered at error latched at master on channel 2, the response time of this pulse train is about from 4.1μS to 8.1 μS. When Master is at "Enabled" state and test pulse is turned on, it will trigger the MPS and time stamp of the source slave and time stamp of master will be latched on EPICS OPI. Hence response time can be derived from these two latched time stamps. The response time of first test pulse of pulse train is 8.074ns if measured with EPICS OPI, it is very close to 8.1μS of worst case response time measured with Oscilloscope.

FUTURE DEVELOPMENT

Polling method is used to collect the I/O status from slave in the current development, to improve the response speed, streaming method can be used to reduce the slave the wait time to transmit the data. Also, bi-direction loop structure for the daisy chain can be used to short the path from last slave to the master, ~3μS response time is expected from this engineering optimization. Real time post mortem data analysis [5] [6] implemented in MPS master FPGA is also considered for future development to locate the root cause of fault conditions quickly and easily. Reliability assessment [7] will be proceeded with MPS system prototype. Master with 9 daisy chains need to be developed.

CONCLUSION

The MPS system prototype is built and function is verified, its function meets for the project requirements. The worst case response time of ~8.1 μS from OK/NOK inputs to mitigation outputs is reached when query command is used to poll the status. A new approach is outlined to use bi-direction loop structure for the slave chain and streaming mode for data collection from slave to master, ~3μS response time are expected from this engineering optimization. Real time post mortem data analysis is proposed to be implemented in MPS master FPGA and reliability assessment will be proceeded with the current MPS system prototype.

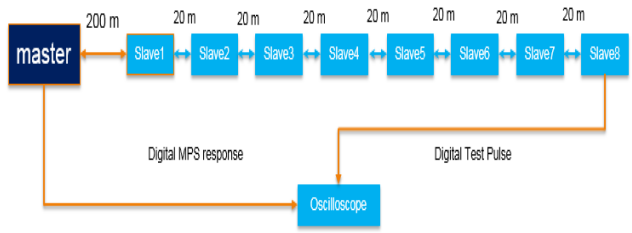

Figure 3: Response Test Diagram of MPS prototype.

Figure 4: Response time measured with oscilloscope.

REFERENCES

[1] J. Wei *et al.*, "The FRIB project – accelerator challenges and progress", in *Proceedings of HIAT 2012*, Chicago, IL USA.

[2] R.York *et al.*, "Technical challenges in design and construction of FRIB", in *Proceedings of 2011 Particle Accelerator Conference*, New York, NY, USA.

[3] G. Kiupel, S. Assadi *et al.*, "Fast and critical detection devices planned for the machine protection system at the facility for rare isotope beams", in *Proceedings of DIPAC2011*, Hamburg, Germany.

[4] Lin Wang *et al.*, "EPICS IOC Prototype of FRIB Machine Protection System", presented at *LINAC'16*, East Lansing, MI, USA, Sep. 2016, paper THPLR043, unpublished.

[5] M. Jonker *et al.*, "The CLIC machine protection", in *Proceedings of IPAC'10*, Kyoto, Japan.

[6] C. Sibley *et al.*, "Machine protection strategies for high power accelerators", in *Proceedings of the 2003 Particle Accelerator Conference*.

[7] B.Dehning *et al.*, "Reliability Assessment of the LHC Machine Protection System", in *PAC2005*, Knoxville, USA, May 16-20, 2005.

ISBN 978-3-95450-169-4