FRIB Fast Machine Protection System: Engineering For Distributed Fault Monitoring System And Light Speed Response

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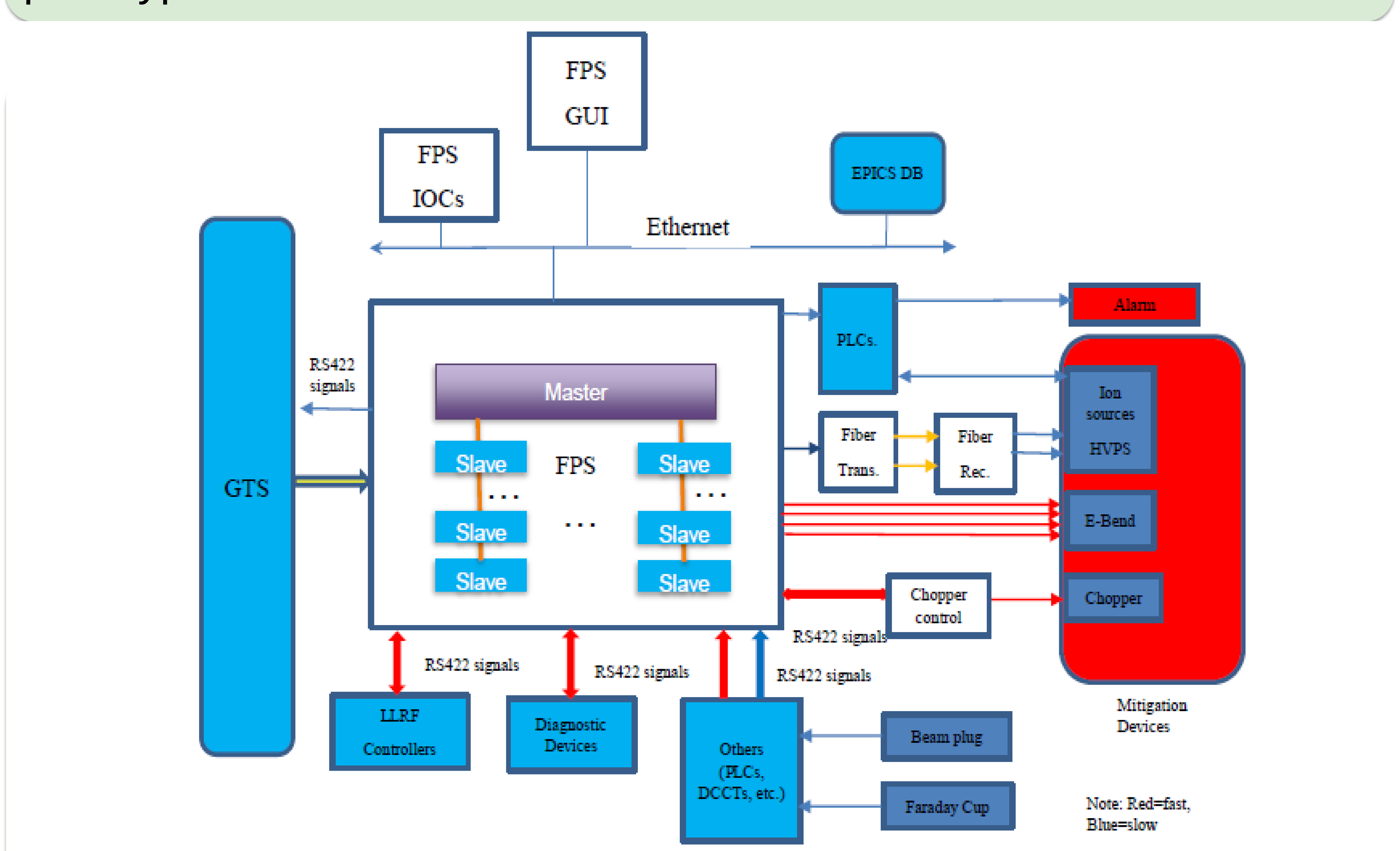
Introduction

The Facility for Rare Isotope Beams (FRIB) needs a Machine Protection System (MPS) to minimize component damage and operational interruption caused by both acute (fast) and chronic (slow) beam losses. The fast protection system collects OK/NOK inputs from hundreds of devices, such as low level RF controllers, beam loss monitors, and beam current monitors, which are distributed over 200 m. The engineering challenge here is to design a distributed control system to response within 35 μs from sensing the fault to dump the beam, also quickly rearm for the next pulse for 100 Hz beam. This poster describes an engineering solution with a master-slave structure adopted in FRIB which covered from system architecture to FPGA hardware platform design, from system prototype to its function verification test results.

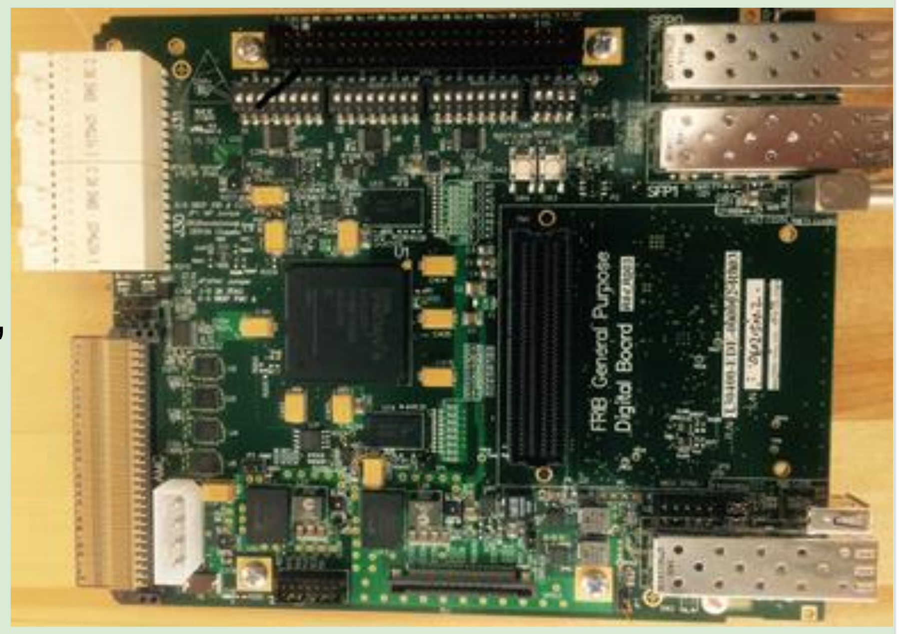


FRIB MPS consists of the FPS network, MPS sensors, MPS mitigation devices, and MPS Input Output Controllers (IOCs). Run Permit System function is needed to start the beam but is separated from MPS system. Time-critical sensors and mitigation devices are connected directly to MPS net-work. Non-time-critical sensors are connected to MPS network via aggregation PLCs. The allocation of response times will be determined during commissioning. Design goals are:

•10 µs for device to detect a failure and to inform MPS network
•10 µs for MPS network to identify the right mitigation action(s) and to distribute the signal to appropriate output(s)
•5 µs for mitigation device to receive signal and to execute.
•10 µs for beam mitigation time (residual beam in the accelerator)

Key MPS Hardware Development

FRIB General Purpose Digital Board is developed for MPS control board. The core part of the FGPDB is the Spartan-6 FPGA XC6SLX150T-2FGG900C. It's a microTCA.4 standard board with rich extended interfaces. Our strategy of MPS master is to develop the master based on FGPDB board first to meet front end commissioning schedule, the master based on KCU105 board will be developed. Both slave and master firmware have the Micro-blaze system to manage the UDP communication, Flash, DDR3 and the FPS logic to manage the I/O ports, daisy-chain communication, Event Receiver (EVR). The challenge of Firmware development for FPS is to fit the design into the Spartan-6 chip which has only 16 global clocks and solve the timing issues of Clock Domain Crossing (CDC) between GTS clock, Ethernet clock, Daisy chain clocks, I2C clock and system clocks.



Future Development

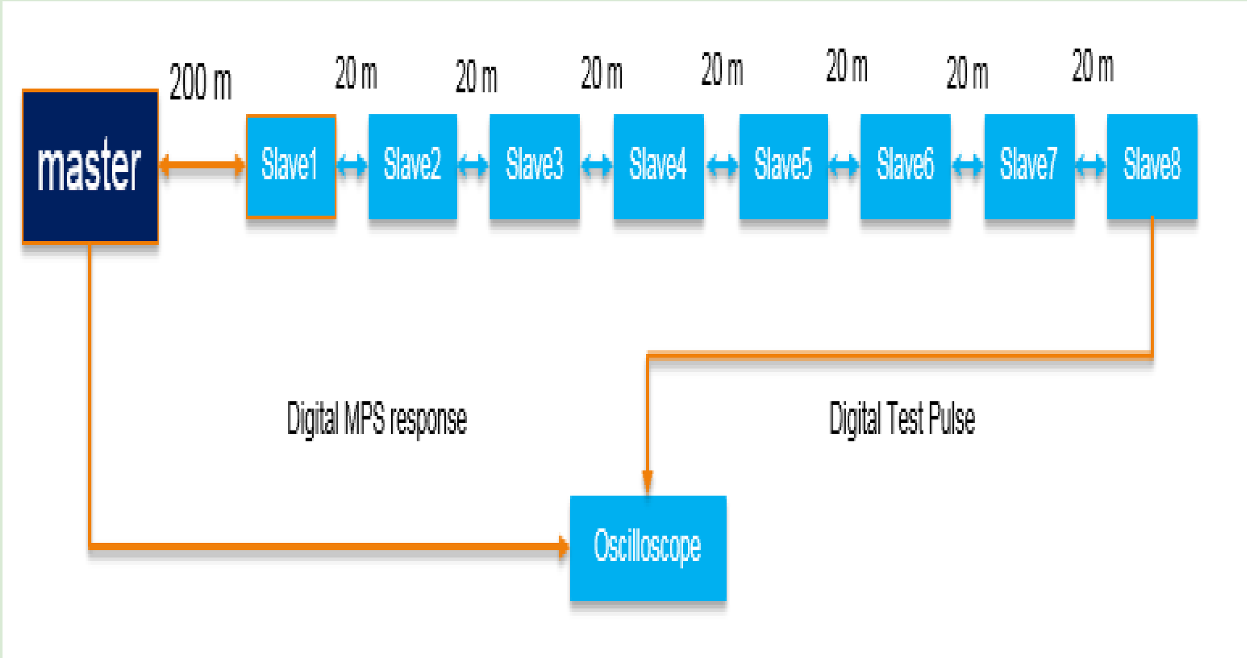
Polling method is used to collect the I/O status from slave in the current development, to improve the response speed, streaming method and bi-direction loop structure for the daisy chain can be used to improve the response speed, ~3µS response time is expected from this engineering optimization. Real time post mortem data analysis implemented in MPS master FPGA is also considered for future development to locate the root cause of fault conditions quickly and easily.

Conclusion

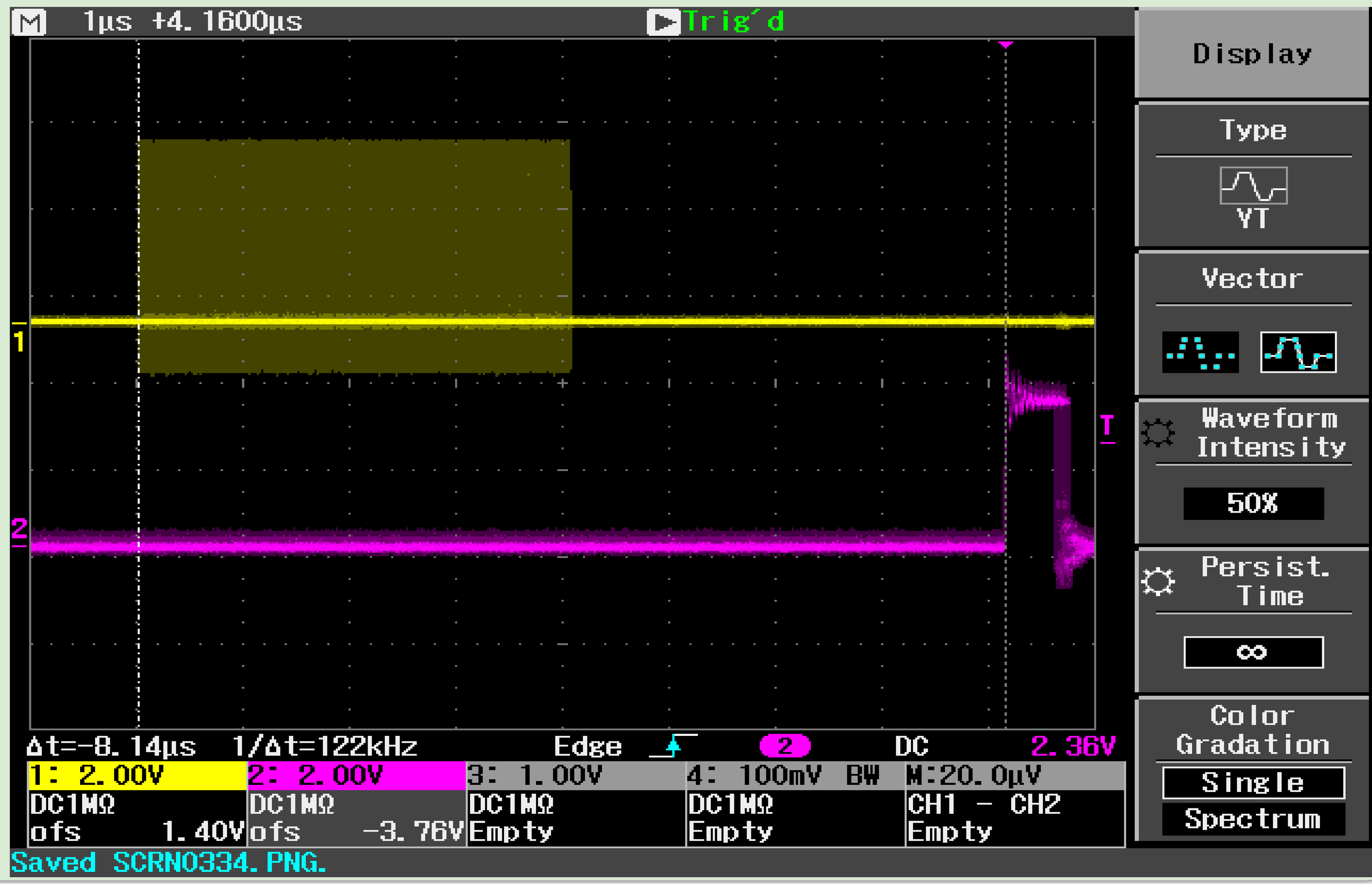
The MPS system prototype is built and function is verified. The worst case response time of ~8.1 µS from OK/NOK inputs to mitigation outputs is reached when query command is used to poll the status. A new approach of bi-direction loop structure for the slave chain and streaming mode for data collection is expected to achieve ~3µS response time. Real time post mortem data analysis is proposed to be implemented in MPS master FPGA and reliability assessment will be proceeded with the current MPS system prototype.

System Prototype

A MPS system prototype is built for performance demonstration, which includes FPS, Ion source fiber control system, MPS slave and master EPICS IOCs and Engineering Operator Interface (OPI). The FPS includes one FGPDB based master and one daisy chain of 8 slave nodes. GTS event generator and EPICS network server are also connected. The daisy chain fiber between master and the first slave is 210 meters, between slaves is 20 meters.



The test signal is an 8 ns pulse train which starts the first pulse right after data is sent from the slave, followed by the pulse which is 8ns delayed of previous one and is sent 4.096 ms(1024 query periods) after the query period when the previous one is sent. Slave 8 receives the test pulse and informs the master. Master latches the fault and the GTS time stamps of fault of slave and master. The worst case response time is the first test pulse. It is 8.074µs if measured with GTS time stamp and ~8.1µs if measured with Oscilloscope.



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