High Precision RF Control for SRF Cavities in LCLS-II

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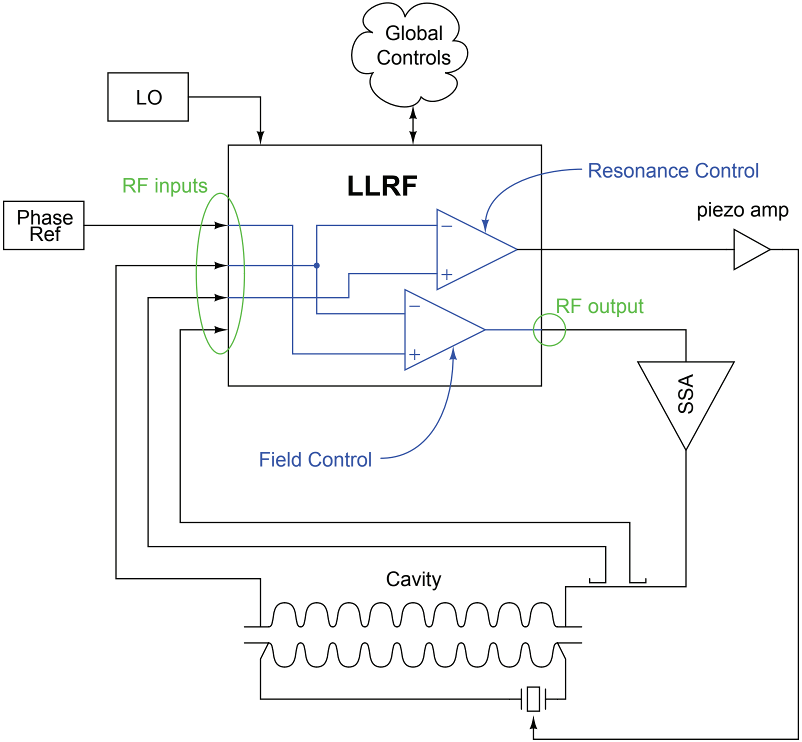
Outline

- A little LLRF background
  - Field control
  - Resonance control
- Hardware architecture selected for LCLS-II
  - Functional partitioning
  - Frequencies
  - Relationship with accelerator installation
  - Thermal design
- Chassis performance
- Test results from FNAL CMTS
  - Basic operation
  - Phase noise
- Summary and parting comments
  - Movie?

Abstract LLRF Feedback Topology

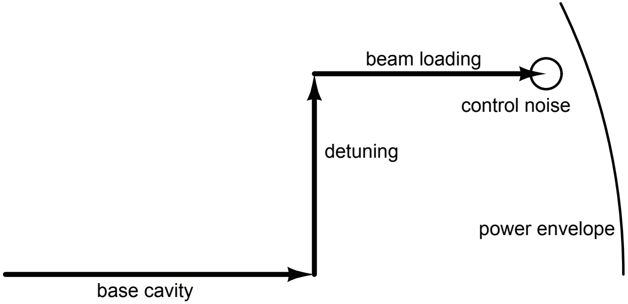


Strong Feedback for Field Control

Project requirement is 0.01° and 0.01%

- Broadband feedback – low-latency P-I style – is proven robust at resisting unpredictable disturbances
- SRF cavities have earned a reputation of producing unpredictable disturbances
- Prominent disturbance source terms
  - Microphonics + helium bath pressure fluctuation
  - SSA power supply ripple
  - Beam loading

Project selected amplifiers big enough to meet demands of 10 Hz detuning



Field Control Requirements and Drift

Core physics requirement is 0.01° and 0.01%

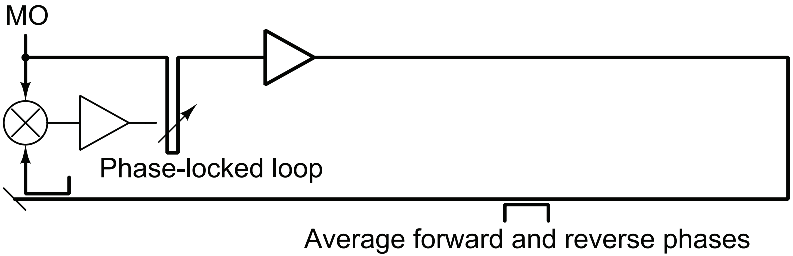
- "For frequencies above 1 Hz" due to operation of Beam-Based Feedback

Since we all know that brick-wall filters at 1 Hz don't exist, the most obvious technical interpretation of that statement is:

- If the error is passed through a first-order high-pass filter with cutoff 1 Hz, the resulting rms error is less than 0.01° and 0.01%.

That conclusion is weak, especially in times when the beam (and therefore BBF) is off. Cavities could reach full 5° long-term drift limit in < 9 minutes.

System has been architected and designed for low (not zero) drift and drift rate. The key element of that is a phase-averaging reference line.



Resonance Control

- Fine control of cavity resonance frequency using piezoelectric actuators
- Use waveform information from cav, fwd, rev to determine cavity detune

  - simplest method is to evaluate phase shift from fwd to cav signal, as long as cavity voltage is constant.
  - long term ($>10\,\mathrm{s}$) need to auto-correct for cable drifts
  - painful in the old analog days, several digital techniques available
- Start with simple I loop to track detune drift, nominal 1 Hz bandwidth
- Ongoing experiments at Fermilab to upgrade that to actively suppress narrow-band source terms

Resonance Control and Quench Detect

Real and Imaginary component of A (units s^{-1}) in cavity differential equation

$$\frac{d\vec{V}}{dt} = A\vec{V} + B\vec{K} + C\vec{I}$$

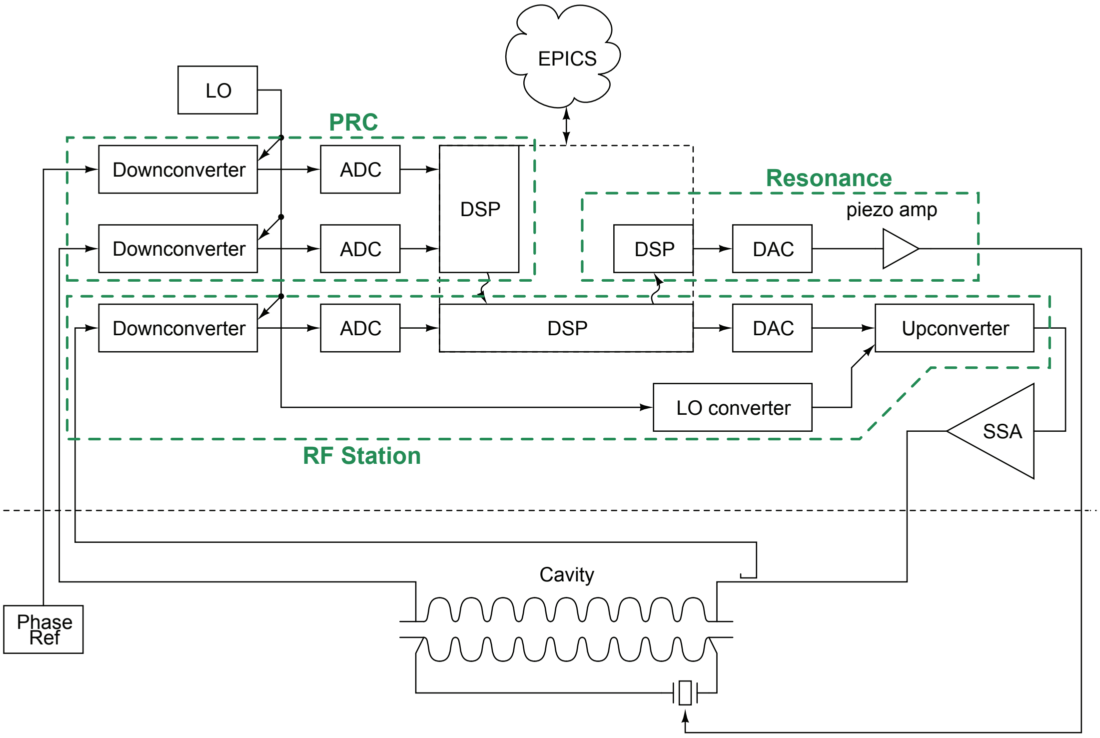
gives Q_L and cavity detune frequency. Compute this inside FPGA for quench detect interlock and running the tuning loop.

Explicitly (without beam)

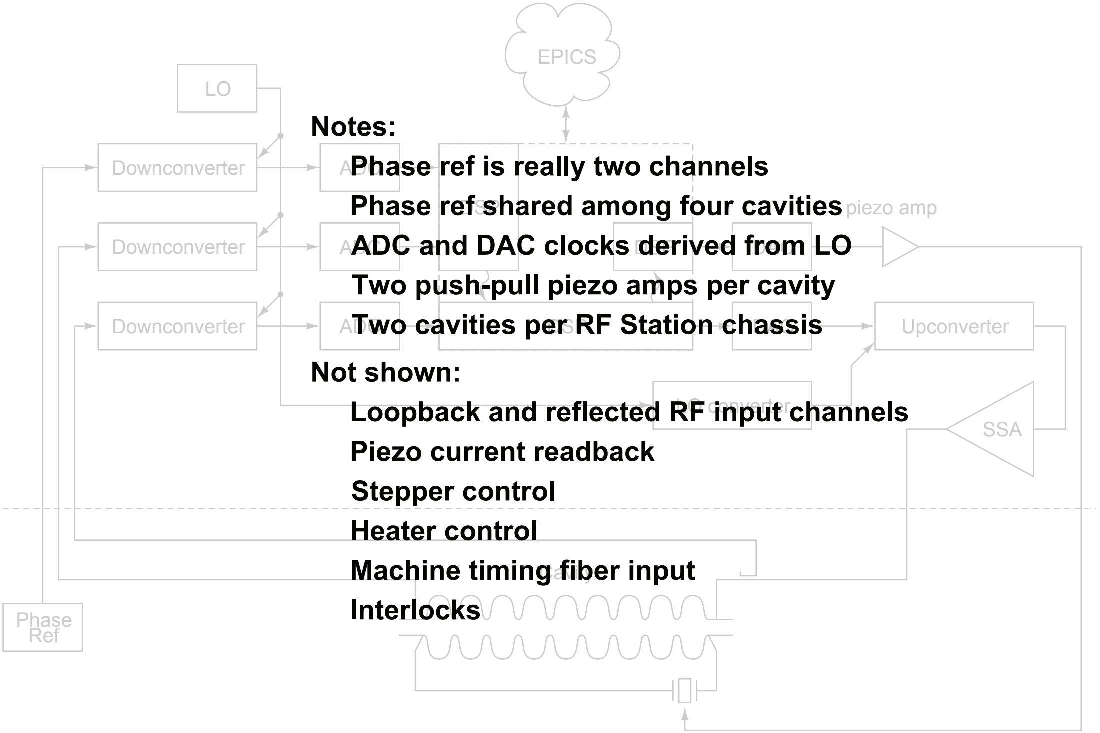
$$A = \frac{1}{\vec{M}_V} \cdot \left[\frac{d\vec{M}_V}{dt} - B'\vec{M}_K \right]$$

where B' has to be calibrated *in situ*. Has been tested in hardware.

Simplified hardware architecture



Simplified hardware architecture



Notes:

- Phase ref is really two channels
- Phase ref shared among four cavities
- ADC and DAC clocks derived from LO
- Two push-pull piezo amps per cavity
- Two cavities per RF Station chassis

Not shown:

- Loopback and reflected RF input channels
- Piezo current readback
- Stepper control
- Heater control
- Machine timing fiber input
- Interlocks

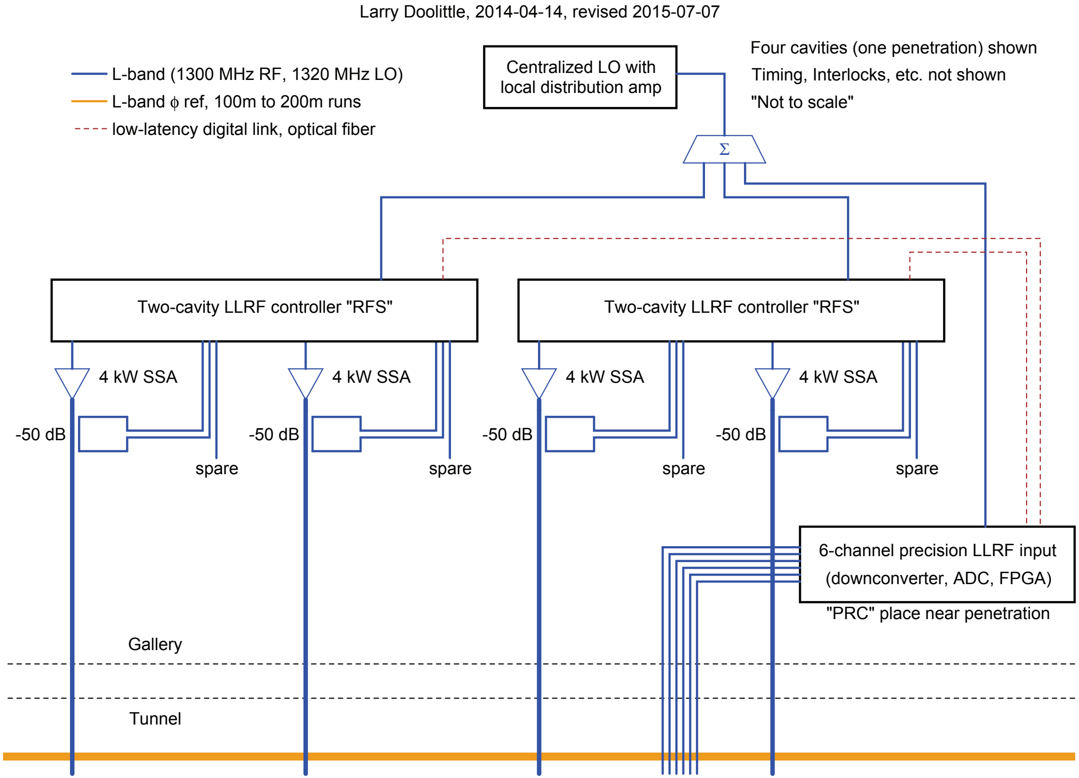
Frequency Relationships for Near-IQ Sampling

$$
\begin{aligned}
f_{\mathrm{RF}} &= 1300\ \mathrm{MHz} \\
f_{\mathrm{Clk}} &= 94.3\ \mathrm{MHz} = f_{\mathrm{LO1}}/14 \\
f_{\mathrm{IF1}} &= \ \ 20\ \mathrm{MHz} = f_{\mathrm{Clk}} \cdot \tfrac{7}{33} \\
f_{\mathrm{LO1}} &= 1320\ \mathrm{MHz} = f_{\mathrm{RF}} \cdot \tfrac{66}{65} \\
f_{\mathrm{IF2}} &= \ 145\ \mathrm{MHz} = f_{\mathrm{Clk}} \cdot \tfrac{203}{132} \\
f_{\mathrm{LO2}} &= 1155\ \mathrm{MHz} = f_{\mathrm{LO1}} \cdot (1 - \tfrac{1}{8})
\end{aligned}
$$

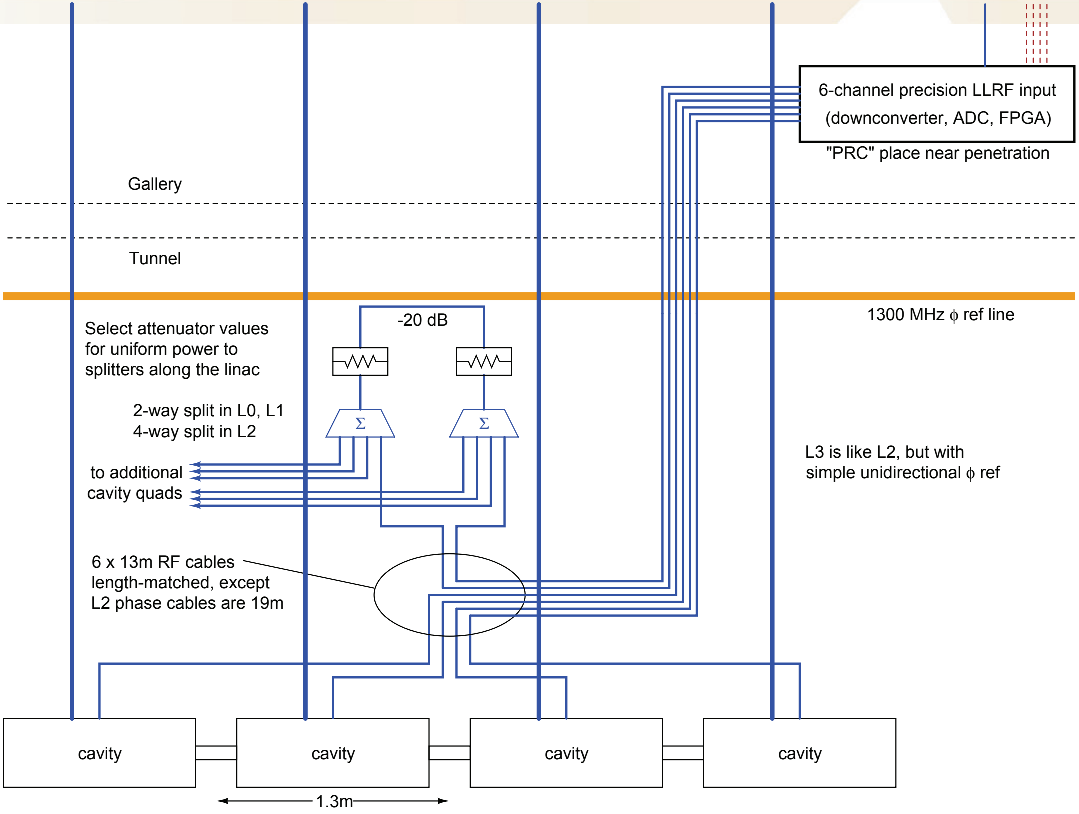
Unusual Split-LO design bypasses usual compromises in choosing IF

- Low 20 MHz IF for receiver reduces crosstalk & sensitivity to ADC clock jitter
- High 145 MHz IF for transmitter improves output sideband-select filter
- Circumvents usual problems with isolation between drive and input IF
- Receiver IF near middle of first Nyquist zone of 94.3 MS/s ADC
- Full TM_{010} passband (1274-1300 MHz) fits in first Nyquist zone of ADC
- Transmitter IF near middle of second Nyquist zone of 188.6 MS/s DAC

Meso-scale Hardware Architecture 1



Meso-scale Hardware Architecture 2



6-channel precision LLRF input (downconverter, ADC, FPGA)

"PRC" place near penetration

Gallery

Tunnel

1300 MHz ϕ ref line

-20 dB

Select attenuator values for uniform power to splitters along the linac

2-way split in L0, L1
4-way split in L2

L3 is like L2, but with simple unidirectional ϕ ref

to additional cavity quads

6 x 13m RF cables length-matched, except L2 phase cables are 19m

Meso-scale Hardware Architecture discussion 1

All long cables and analog components are phase-drift compensated

- Digital variant of field-tested phase-averaging reference line used for ∼150 m runs covering L0, L1, and L2
- Matched 13 m cables move probe and reference signals to gallery in L0 and L1
- Precision receiver channels will approximately track each other in phase (this can be checked on the bench), and the receiver temperature stabilization upgraded if needed (starts in an air-conditioned rack)
- Explicitly depends on beam-based feedback (slow is OK) to remove residual drift
- No drift compensation in L3 (but that linac operates on-crest)

Brings up “raw” probe cables for commissioning and troubleshooting

Simpler than more exotic phase calibration schemes

Meso-scale Hardware Architecture discussion 2

By centralizing precision receiver:

- Keep microphonically varying forward and reverse RF signals away from the critical probe RF
- Digitally replicate the reference digitizer result across four stations
- Isolate the most sensitive measurements from most sources of EMI
- Add "only" about 140 ns to field control loop latency
- LO must be shared between receiver and control station (cable drift is OK)

Modular chassis construction

- Leverages "standard" fiber links between FPGA
  - includes machine timing and global controls
- Accommodates separate chassis for resonance control and interlocks
- Good match for inter-lab collaboration
- FPGA board is upgradable on its own
  - all industry-standard interfaces (FMC, Ethernet, QSFP)

"Modularity is not a hack" – Daniel J. Bernstein

Thermal Design

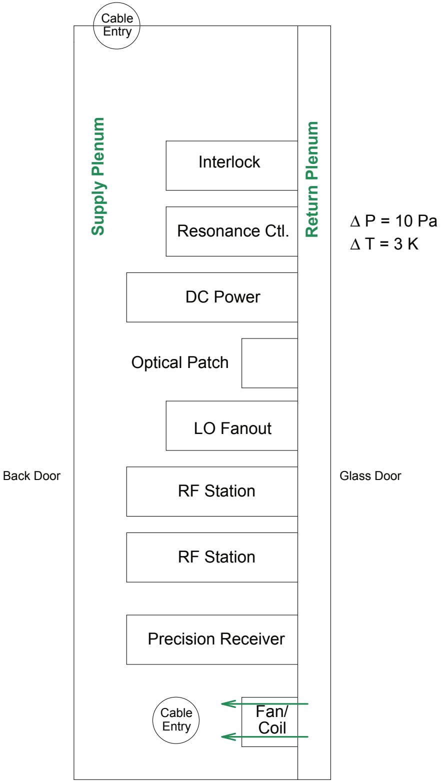
One rack supports 4 cavities

Total chassis power dissipation estimate/budget: $\sim$50 W/chassis × 5

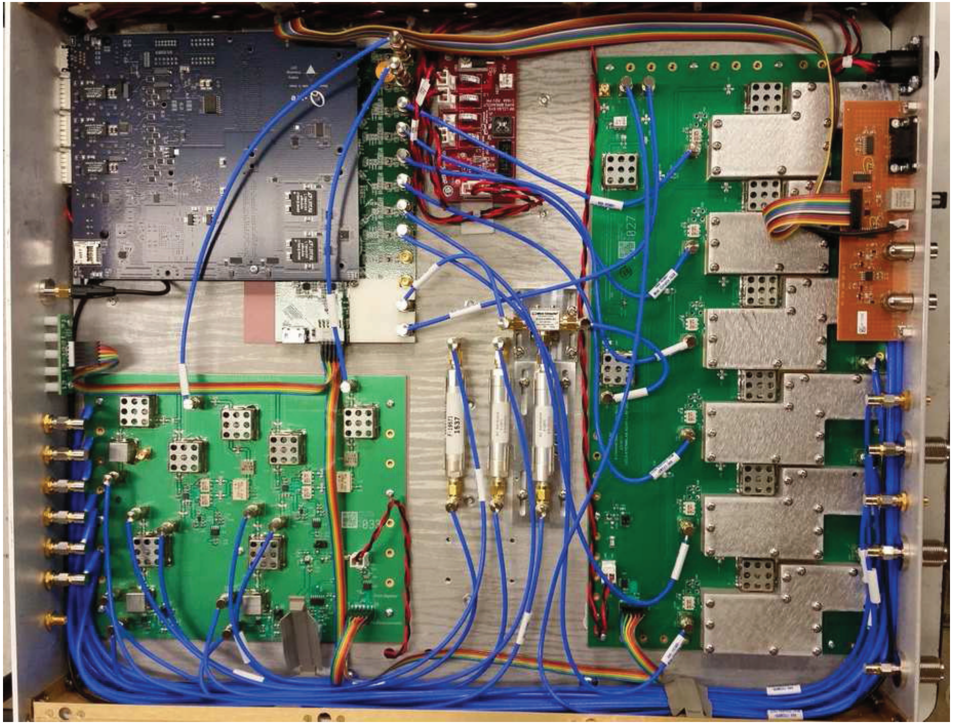
$250\,\mathrm{W}\ /\ 3\,\mathrm{K}\ /\ \rho c_P = 0.064\,\mathrm{m}^3/\mathrm{s}$

$0.064\,\mathrm{m}^3/\mathrm{s} \cdot 10\ \mathrm{Pa} = 0.64\,\mathrm{W}$

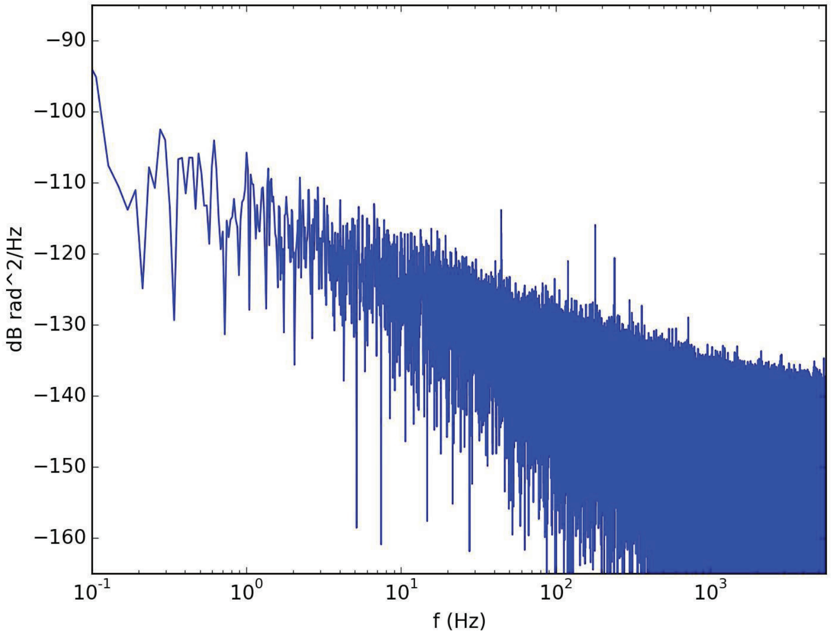
Front of rack can be opened for access to test points, without totally breaking airflow pattern and thermal management



Chassis assembled

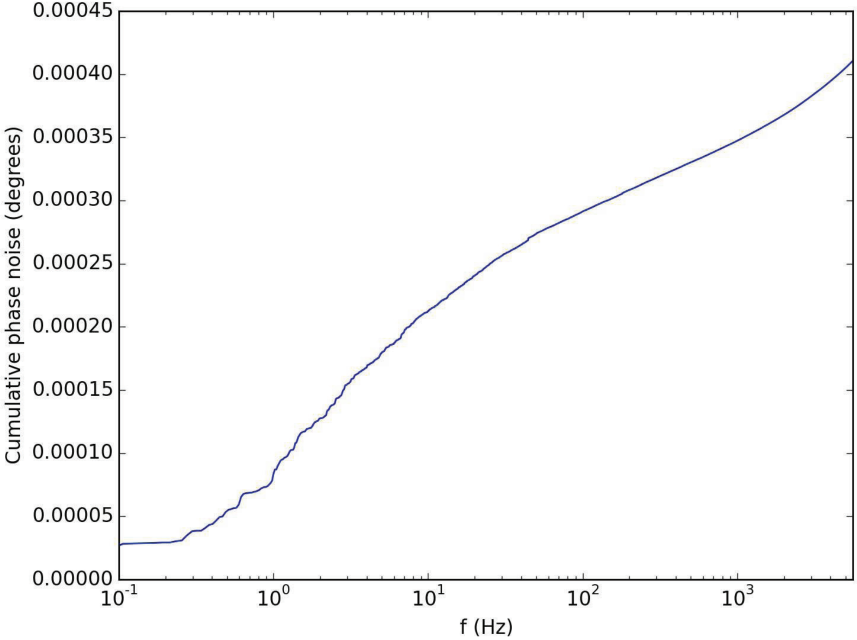


Chassis phase noise



Measured at 1300 MHz using passive splitter and short cables to two Rx inputs.

Chassis phase noise



Note 1 Hz high-pass included to represent beam-based feedback and to avoid logarithmic singularity of $1/f$ noise integral to DC.

Rack installed at FNAL CMTS

Power supply

Resonance control

reserved

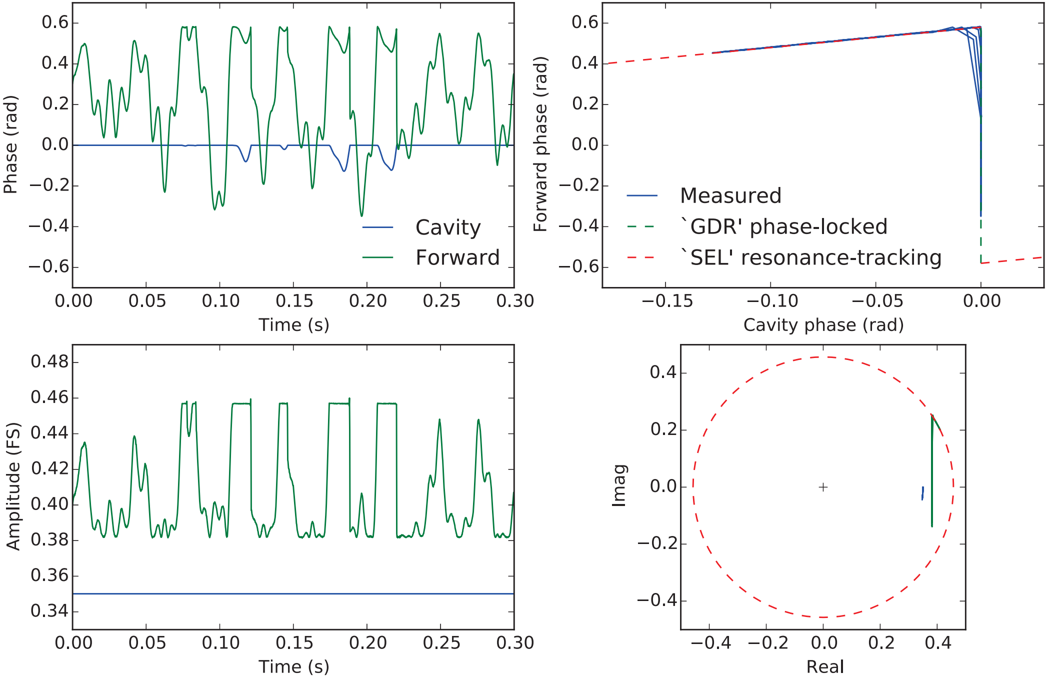
RF Station

RF Station

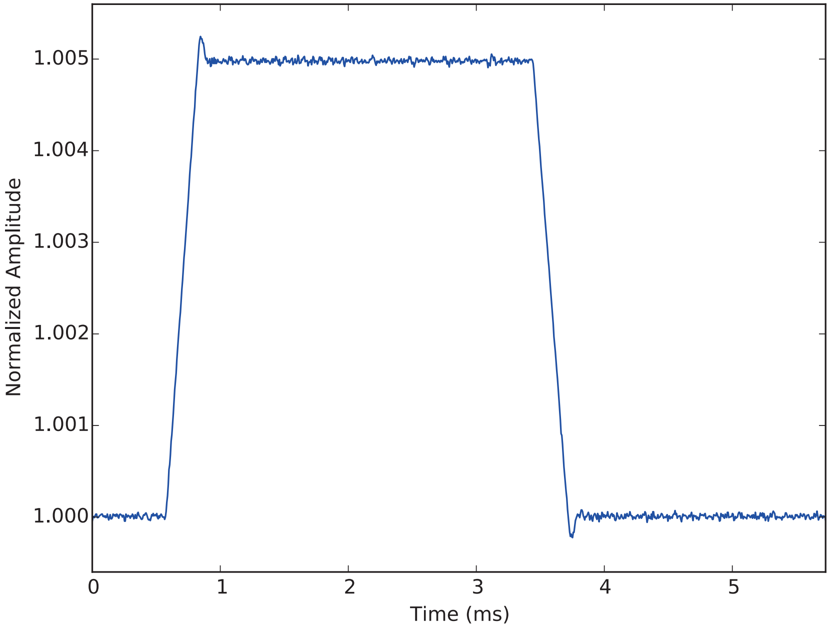
Precision Receiver

Phase-locking SEL w/IQ-clip works as intended

Phase-locking SEL with clip limits on Q component works as intended

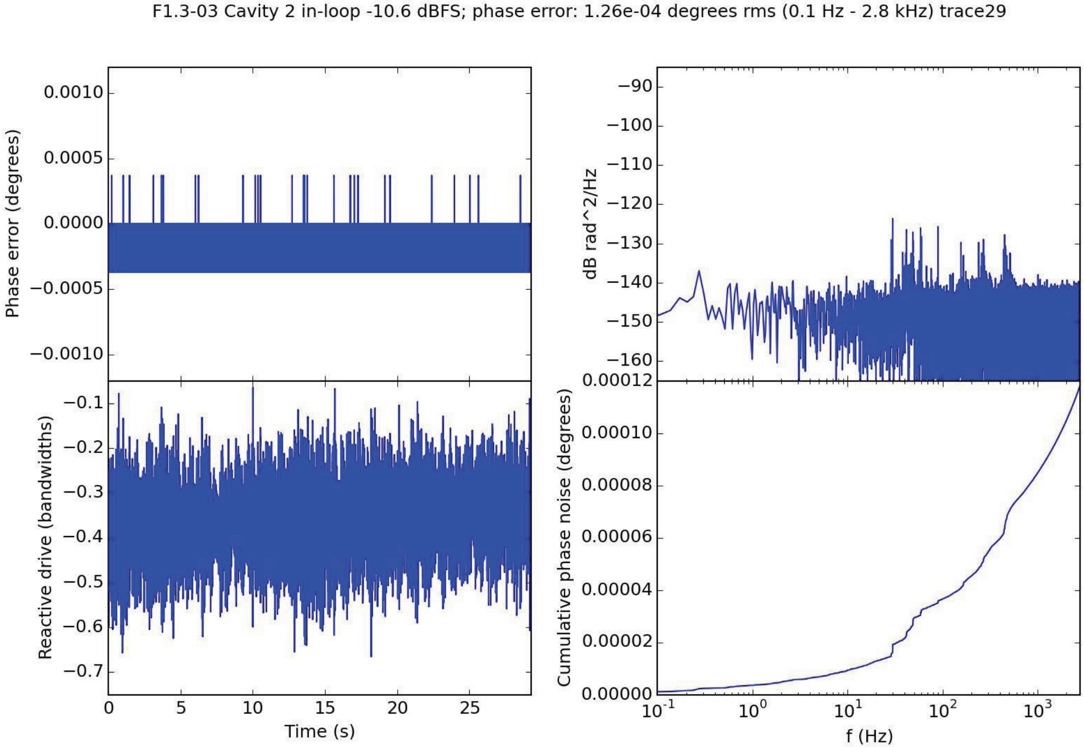


PI Gains can be set for reasonable transient



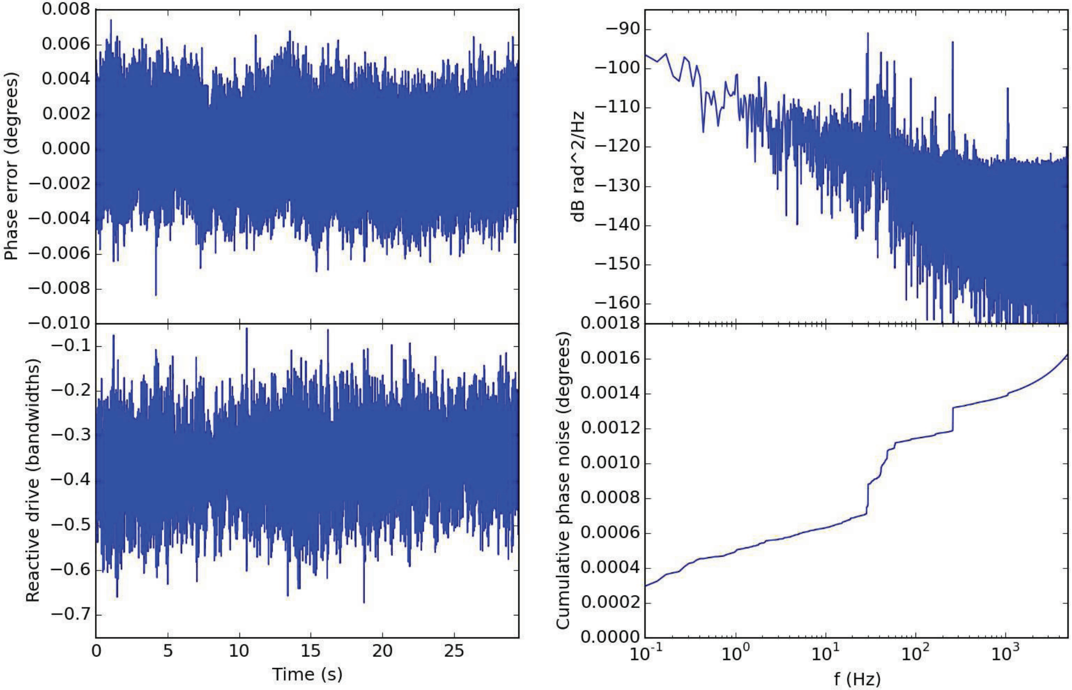
Response to 0.5% amplitude step in setpoint, slew-rate-limited due to clip limits and cavity pole.

In-loop phase noise

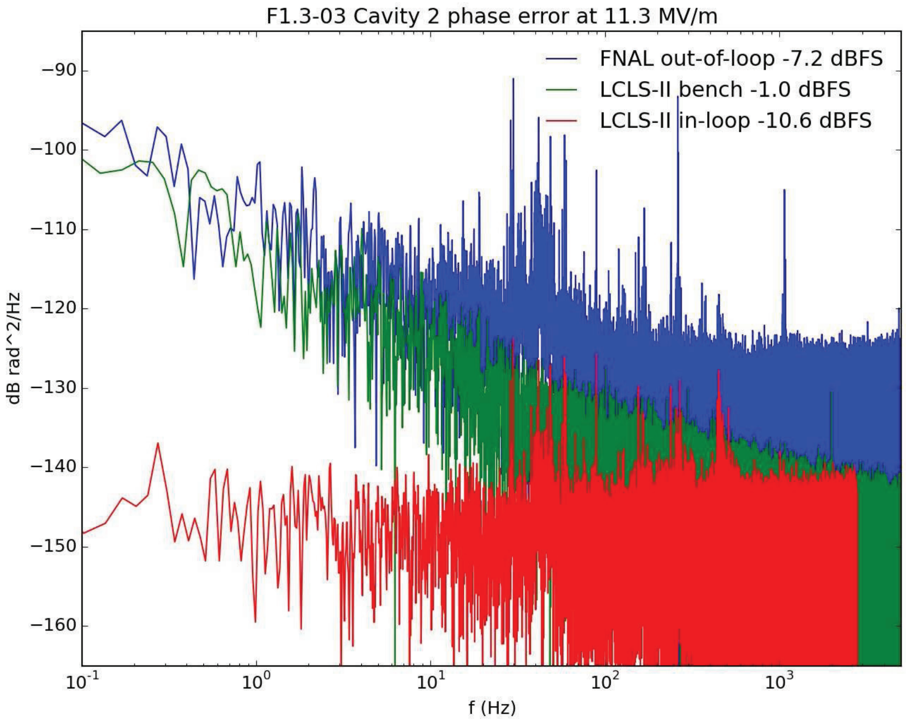


Out-of-loop phase noise

F1.3-03 Cavity 2 out-of-loop -7.2 dBFS; phase error: 1.63e-03 degrees rms (0.1 Hz - 5.0 kHz) 170705_1730_lcls2



Phase noise comparison



Cavity Phase noise spectra comments and *caveats*

- Signal strengths are different for the three curves
- 11.3 MV/m was administrative limit for that testing session
- Crosstalk from forward and reverse probes in FNAL system explains amplitude discrepancy for microphonics peaks; corresponding crosstalk on LCLS-II system is demonstrated $<$ -129 dB
- $1/f$ components appear as expected
- FNAL CMTS installation not set up to test drift behavior

Superficial conclusion is not wrong:

- Field out-of-loop error $<$ 0.018° peak-peak, 0.0016° rms, in 0.1 Hz to 5 kHz, better than spec; leaves margin for:
  - larger closed-loop bandwidth (goal 20 kHz)
  - phase-reference-line contribution
  - beam-loading effects
  - larger microphonics (this cavity had about 60% of detuning “spec”)
  - unknowns

Summary

The LCLS-II LLRF system uses mainstream LLRF construction techniques, with small tweaks added to address drift (improve operability):

- digital drift-compensated reference line
- batch- and length- matched cables
- thermal filtering for receiver chain components

Other new features introduced to improve crosstalk and ease RF design:

- electrically isolated precision receiver chassis
- low IF on Rx side, high IF for Tx
- digitally replicate one phase reference result across four cavities

Conclusion

Tests on Prototypes give evidence this system meets stringent performance specs based on the high quality electron beam needed for an X-ray light source

Architecture is modern and modular, will form a reliable and operable part of the larger LCLS-II controls.

Thank You!

谢谢

LCLS-II LLRF Collaboration Team

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