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DEVELOPMENT OF A 166.6 MHz DIGITAL LLRF SYSTEM FOR HEPS-TF PROJECT*

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Abstract

A 166.6 MHz superconducting RF system has been proposed for the High Energy Photon Source (HEPS), a 6 GeV kilometer-scale light source. A 166.6MHz digital low-level RF system for HEPS-TF project has been developed firstly. And the digital low-level RF system has been successfully applied to the horizontal high power test of 166.6MHz superconducting cavity. The cavity field stability has been successfully achieved about ±0.03% (pk-pk) in amplitude and ±0.02 degree (pk-pk) in phase while the cavity field voltage is up to 1.2MV. It can meet the field stability requirements towards ±0.1% in amplitude and ±0.1 degree in phase of HEPS project. Further study and optimization of the system is under way.

INTRODUCTION

The High Energy Photon Source (HEPS) is a 6-GeV, 1.3- km, ultralow-emittance storage ring light source to be built in the Huairou District, northeast suburb of Beijing, China [1]. Its main beam parameters are listed in Table 1.

HEPS RF system will include five 166.6 MHz/250 kW superconducting cavities and two passive 3rd harmonic 250kW superconducting cavities in the Storage Ring (SR), while six 500MHz/100kW normal conducting cavity in the Booster. Its main RF parameters are listed in Table 2. Prior to its official construction, a test facility namely HEPS-TF has been approved in 2016 to R&D and prototype key technologies and components [2].

Table 1: Beam Parameters of the HEPS Storage Ring

Parameter	Value
Energy	6 GeV
Circumference	1360.4 m
Current	200 mA
Energy loss/turn	4.4 MeV
Beam power	900 kW

Table 2: RF Parameters of the HEPS Storage Ring

Parameter	Fundamental	Harmonic
RF frequency	166.6MHz	499.8MHz
Number of cavities	5	2
Total RF voltage	5.4MV	3.2MV
RF power/station	250kW	250kW
RF field stability (pk2pk)	±0.1%, ±0.1degree	±0.1%, ±0.1degree

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Compared with analog low-level RF system, digital low-level RF system has more advantages, including its expansibility, flexibility, powerful function, lower cost and higher resolution and accuracy which are very essential for storage of high-current and high quality beam. It has been upgraded from the analog low-level RF system to digital low-level RF system in BEPCII RF system. The digital low-level RF system is based on SSRF 2nd generation LLRF board. With reference to the SSRF digital low-level RF system and based on the requirement of HEPS-TF project, we have independently developed the digital low-level RF system, including DSP board based on FPGA, RF analog front-end board and security interlocking board and so on.

In this paper, we will present the LLRF system design, prototype boards design and debugging, software design and the integration of 166.6MHz digital low-level RF system and the recent preliminary test results. We have integrated the digital LLRF system and successfully applied to the horizontal high power test of 166.6MHz superconducting cavity. A very good stability of the cavity field has been successfully achieved about ±0.03% in amplitude and ±0.02 degree in phase, much better than the requirements of ±0.1% in amplitude and ±0.1 degree in phase. That is the first digital low-level RF system independently developed by the RF Group of Accelerator Division, Institute of High Energy Physics (IHEP), Chinese Academy of Sciences.

SYSTEM ARCHITECTURE

The frame diagram of HEPS-TF RF system is shown in Fig. 1.

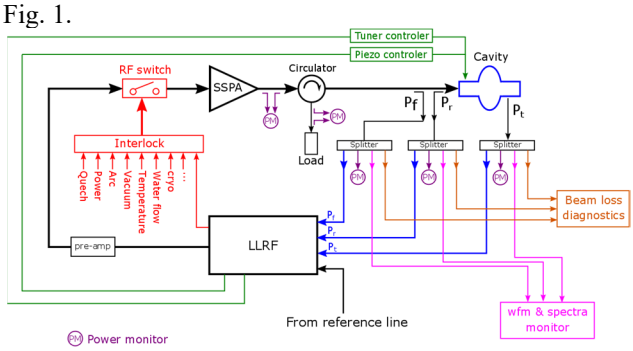

Figure 1: The diagram of RF system.

The RF system consists of three parts: superconducting cavity, solid-state amplifier and low-level RF system. The reference line provides RF reference signal to the LLRF system. The LLRF system generates RF excitation and drives the solid-state power amplifier after the RF switch. The solid-state amplifier amplifies the RF signal and feeds it to the superconducting cavity through the circulator, feeder and coupler to establish a radio-frequency field for

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particle acceleration. The low-level RF system will collect pickup signal of superconducting cavity, forward power and reflective power of superconducting cavity entrance, and complete feedback control of cavity field, cavity resonance frequency control, and quench protection of superconducting cavity based on these signals.

Hardware Architecture

The function of Digital low-level RF system mainly includes the amplitude and phase stabilization control loop of cavity field, cavity resonance frequency control loop, solid-state amplifier feedback control loop, CW/pulse mode and security interlocking and so on. Based on these functions and lessons from the domestic and foreign digital low-level RF systems, we have developed the hardware design of digital low-level RF system. The hardware of LLRF system mainly consists of digital signal processing (DSP) board, RF analog front-end board and security interlocking board. The main functions of the DSP board include feedback control loop of cavity field, digital arithmetic, clock frequency division and so on. The RF analog front-end board mainly implements the conversion between radio frequency (RF) signal and intermediate frequency (IF) signal, the function of power division, amplification and filter, and realizes the cooperation with the DSP board. The security interlocking system includes the interlocking board and PLC. When a fault occurs, the interlocking board will get it. After receiving the interlocking signal it will switch off the RF switch as soon as quickly to cut off the RF excitation.

DSP Board

The functional diagram of digital signal processing board (DSP) for low-level RF system is shown in Fig. 2. FPGA is the core chip of the board. EP3SL150F1152C2 chip under Stratix III series produced by ALTERA company is used. FLASH, SRAM, SDRAM, EPCS are configurated in the peripheral. In addition, it includes three 16-bit, 125 MSPS, 1.8 V, dual-channel high-speed analog-to-digital converters (ADC) AD9268-125, one 16-Bit, 800 MSPS, dual-channel high-speed digital-to-analog converter (DAC) AD9788, clock distribution chip AD9520, network communication chip LAN91C111 and CPLD chip EPM3512AQI208-10. As the core arithmetic processing chip, FPGA is mainly used for digital signal acquisition and processing, DDS signal recovery, loop arithmetic control and other logic control functions, as well as signal storage, parameter setting and communication. These functions are realized by a hardware description language Verilog HDL. AD9520 provides a multioutput clock distribution function with subpicosecond jitter performance, which is used to configure FPGA clock, ADC clock, DAC clock and to generate IF signal. IF signal is sent to the front-end board for mixing to generate local oscillator (LO) signal. CPLD implements the configuration of AD9520, ADC and DAC chips by serial interface SPI. The 16 bit high-speed analog-to-digital converter ADC completes IF signal acquisition, and the 16 bit high-speed DAC completes DDS signal output. Phase Detector performs analog phase detection. Slow SDAC can performs bipolar voltage output conversion to drive Piezo controller.

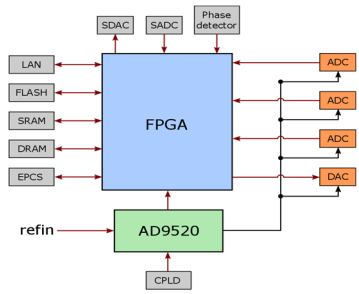

Figure 2: Functional diagram of low-level digital signal processing board (DSP).

The prototype DSP board is shown in Fig. 3. It consists of 12 layers of printed circuit board, including 3 layers of power supply, 3 layers of GND and 6 layers of signal. The board is mainly divided into power distribution circuit, ADC and DAC, FPGA and its peripherals, network communication circuit, clock distribution circuit, analog phase discrimination circuit, motor-driven photoelectric isolation circuit, serial ADC and DAC, CPLD configuration circuit and so on.

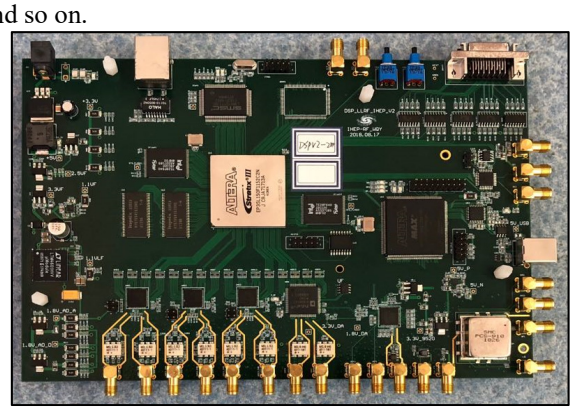

Figure 3: The first prototype DSP board.

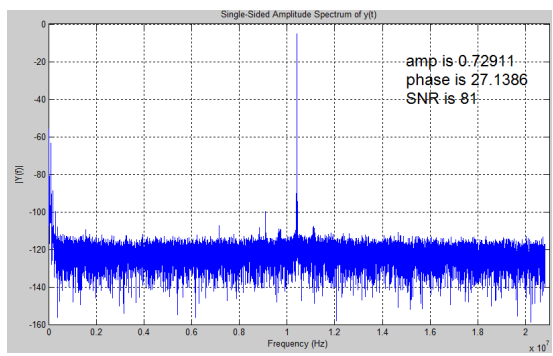

Figure 4: The SNR of one of ADC channel.

The first prototype DSP board has been fabricated and has passed the basic functionality test, and some good results have been produced in the SNR measurements of the RF signal I/O channels as shown in Fig 4.

RF Front-end Board

The principle diagram of the RF analog front-end board is shown in Fig. 5. It offers five down-conversion channels

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and one up-conversion channel. The RF reference signal has four power divisions, one of which is fed into the DSP board to produce Intermediate frequency (IF) signal, which returned to the RF analog front-end board and mixed with the RF signal to generate LO signal. The LO signal is then mixed with the RF signal and IF signal, so as to realize the signal frequency down-conversion and up-conversion.

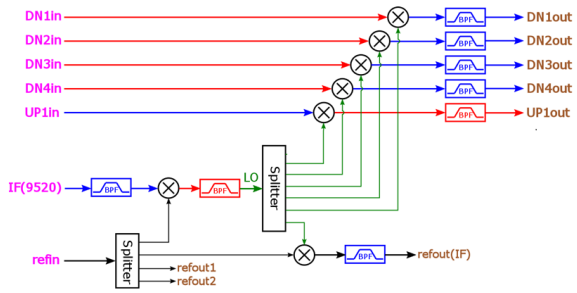

Figure 5: The diagram of RF front-end board.

The first prototype of LLRF analog front-end board is shown in Fig. 6. The board mainly uses mini-circuit RF chips, including power dividers, mixers, amplifiers, attenuators, low-pass and band-pass filters etc. The working frequency range of the designed board covers the frequency range about 100MHz-1.3GHz. Under different RF frequency, only SAW surface acoustic filters with different frequency are needed to filter LO signals and RF signals respectively. SAW filters of LO signals and RF signals can also be replaced by external LC band-pass filters. Low-pass filters of corresponding frequency are adopted according to the frequency selection of IF signals. The design is flexible and suitable for different RF frequency.

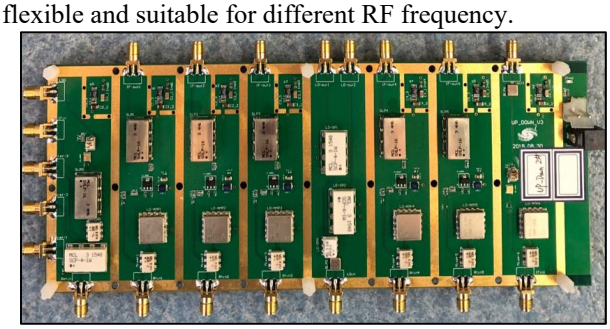

Figure 6: The first prototype of LLRF analog front-end board.

As can be seen from Table 1, channel isolations between channel 3 and channel 4 are the best which can reach 99.7 dB or more, while the isolations of channel 1 with other channels are the worst. In order to make the amplitude-phase loop of the cavity field to be more stable, the third channel is used to down-convert the reference signal and the fourth channel is used to down-convert the cavity field signal, and the first channel and fifth channels are used to down-convert the reflection and incident signals which require less stability accuracy, respectively.

The linearity and channel isolation of RF front-end are measured. The channel isolation measurement results are shown in Table 3.

Table 3: Channel Isolation of RF Front-end Board

Parameter	Ch1 dB	Ch2 dB	Ch3 dB	Ch4 dB	Ch5 dB
CH 1 as input	-	84	101.7	110.7	109.7
CH 2 as input	78.3	-	81.3	102.7	102.7
CH 3 as input	78	90.7	-	99.7	100.7
CH 4 as input	78	96.7	99.7	-	80.1
CH 5 as input	78	96.7	101.7	93.7	-

In addition, the linearity of the RF front-end board is measured, as shown in Fig. 7. The linearity is very well. It has a dynamic range about 40 db. When the IF output level is 10 dbm and the ADC reaches its full range, it still works well within the linearity range.

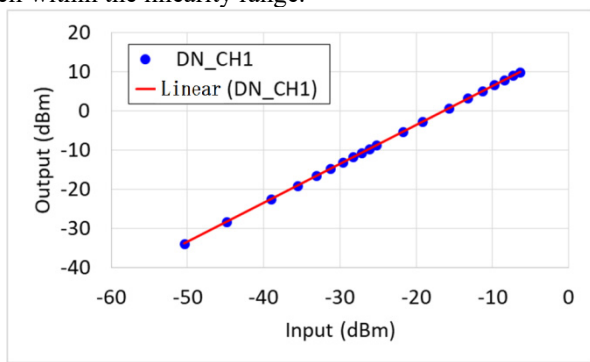

Figure 7: Up-conversion CH1 linearity of RF analog front-end board.

Firmware

The function of LLRF system is mainly implemented by the firmware of FPGA. It is mainly written by Verilog HDL, a hardware description language. It realizes the functions about stable feedback loops adjust the amplitude and phase of cavity field and also the resonance frequency of the cavity, quench detection of cavity field and so on. Firstly, the RF reference signal, cavity RF pick-up signal, incident power and reflected power RF signals of cavity were down-converted to intermediate frequency (IF) signals, and then they were sent to ADCs for data acquisition. With non-IQ algorithm the respective in-phase and quadrature (I/Q) vector signals were achieved. After the I/Q vector rotation of pickup signal, a narrow band cascaded integrator and comb (CIC) filter is used as a low pass filter. the I/Q vector errors between the set points and processed pickup values were sent to the PI controllers. The I/Q outputs of PI controllers were used to generate the output intermediate frequency signal to DAC with the direct digital synthesizer(DDS). The output IF signal was then up-converted to the RF signal to excite the solid-state amplifier. The resonance frequency control of the cavity was similar. the phase error between the incident power signal and the pickup cavity field signal was fed into the PI controllers of the stepper motor and piezo respectively. The output of the PI controllers were sent to their respective drivers to complete the resonance frequency control of the cavity. The stepper motor was used for coarse cavity tuning and the piezo actuator was used for fine cavity tuning.

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Cavity quenches introducing strong heat load fluctuations should be avoided to protect the cryogenic system. Automated prevention and detection of possible quenches is realized through measurement routines and gradient limiters implemented inside the control loop [3].the protection of cavity quench can fall into two categories, open-loop protection and closed-loop protection. Open-loop protection is usually used in the conditioning of cavity and coupler. Superconducting cavity needs to be open-loop conditioned and the cavity could suffer of field emission or quenches. At this time, cavity consumption will increase rapidly, which may cause impact on cryogenic system. Open-loop cavity quench protection can be judged by comparing incident power with reflected power. In the closed-loop case, the superconducting cavity has amplitude-phase feedback control loop and cavity resonance frequency control loop, so the cavity field in the superconducting cavity is relatively stable. but once cavity quench occurs, the stability of the cavity field can't be achieved even with increasing the incident power greatly, and so the cavity field will decrease significantly. it can be judged that superconducting cavity quench occurs at this time, when the RF excitation needs to be switched off or reduced to a small safety value.

The design of clock distribution scheme is mainly combined with the selection of IF frequency, ADC and DAC clocks and non-IQ sampling. the non-IQ sampling scheme provides a benefit of improved measurement precision. In contrast to IQ sampling, most of the harmonics no longer line up with the carrier frequency [4].Finally, we determine that the IF signal is 17 divide of RF frequency signal, and the clock is 3 divide of RF frequency signal, that is, the ratio of IF frequency to sampling clock is 3/17. The nominal RF frequency of HEPS-TF is 166.6MHz. Therefore, the chosen intermediate frequency (IF) of LLRF system is 9.8MHz, and the sampling clock of ADC and DAC is 55.3MHz. and then the local oscillator (LO) frequency is 176.4MHz.

Software Architecture

The software part is mainly responsible for the communication between hardware devices and computers, and the system integration of distributed control based on EPICS architecture. EPICS, experimental physics and industrial control system, is a set of Open Source software tools, libraries and applications developed collaboratively and used worldwide to create distributed soft real-time control systems for scientific instruments such as a particle accelerators, telescopes and other large scientific experiments. EPICS uses Client/Server and Publish/Subscribe techniques to communicate between the various computers. Most servers (called Input/Output Controllers or IOCs) perform real-world I/O and local control tasks, and publish this information to clients using the Channel Access (CA) network protocol. CA is specially designed for the kind of high bandwidth, soft real-time networking applications that EPICS is used for, and is one reason why it can be used to build a control system comprising hundreds of computers. The EPICS waveform records of I/Q signals are very useful for commissioning of the LLRF system.

The applications of IOC in LLRF system includes IOC of DSP board, IOC of PLC system, IOC of serial server and soft IOC of RF system. IOC of DSP board mainly completes communication and interaction between EPICS and DSP board, implements the main function of LLRF system control. IOC of PLC system is to connect RF system signals such as temperatures, water pressure and flow rate, motor position and tuner pressure into EPICS system, at the same time, it can realize slow signals interlocking and remote reset. The serial server IOC mainly completes the acquisition and processing of the signals of vacuum, power, radiation dose, cryogenic temperature and other signals of serial devices; the RF system IOC, as a soft IOC, completes the integration of RF system, including system function optimization, coupler automation conditioning, RF system self-startup, and various software algorithms. Some part of the algorithms are written by python, the state machine is written by SNL, and CSS is used as the OPI. The main LLRF system OPI is shown as Fig. 8.

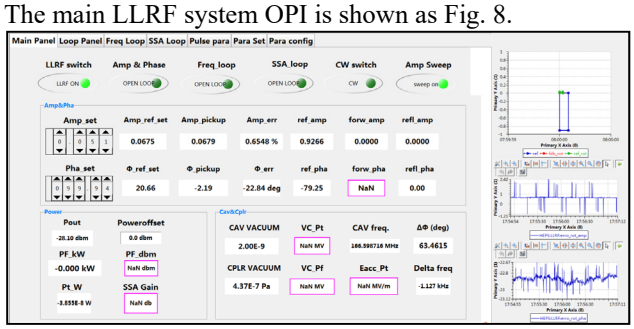

Figure 8: The main LLRF system OPI.

EXPERIMENTAL RESULTS

The HEPS-TF LLRF system was integrated after the debugging of LLRF hardware and software, as shown in Fig. 9. It was demonstrated in the 166.6MHz superconducting cavity horizontal high power test. Firstly, The off-line self-closed loop test of LLRF system was done in which the superconducting cavity was replaced with a 166.6MHz band-pass filter. The long-time amplitude and phase stability of LLRF system reach ±0.03%(pk-pk) and ±0.02 degree(pk-pk), respectively. The measurement result is shown in Fig. 10.

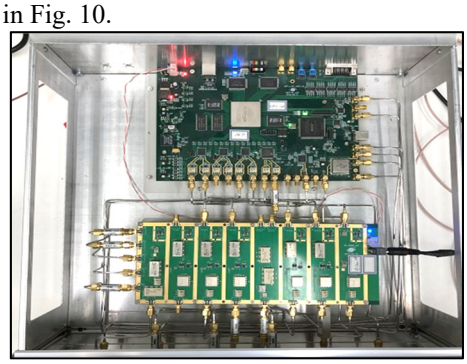

Figure 9: The LLRF control crate integrated with DSP board and analog front-end board.

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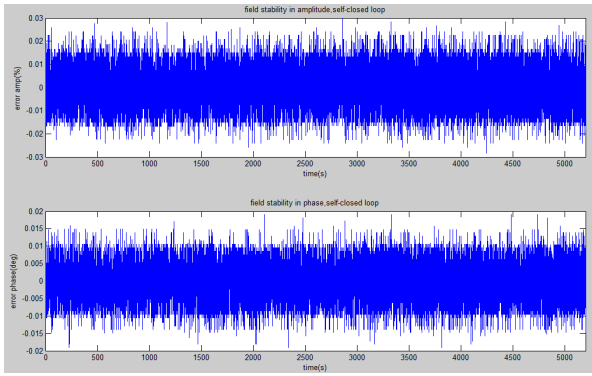

Figure 10: The amplitude and Phase Stability within 90 minutes by self-closed loop of the LLRF system.

The 166.6MHz superconducting cavity horizontal high power test has been done recently, and the self-developed digital LLRF system has been successfully applied in this test. The LLRF system successfully worked well without problem. and some software bugs found during the operation were already fixed. In this horizontal high power test, coupler conditioning, superconducting cavity conditioning, Q0 measurement, microphone effect, Lorentz detuning, auto cavity frequency tuning with motor and Piezo coordinately were mainly carried out, and the functional control of LLRF system was constantly improved. At 2K temperature, the Q0 value of the superconducting cavity at 1.2MV is more than 7e8. At last, the cavity field stability has been successfully achieved about ±0.03%(peak-peak) in amplitude and ±0.02 degree(peak-peak) in phase when the cavity field voltage is 1.2MV. it can meet the field stability requirements towards ±0.1% in amplitude and ±0.1 degree in phase of HEPS project. The test results are shown in Figure 11.

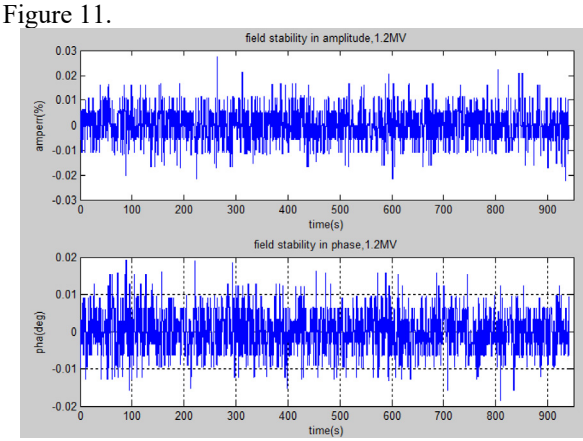

Figure 11: The amplitude and phase stability within 15 minutes when the cavity voltage is 1.2MV.

SUMMARY

This paper mainly describes the system architecture of HEPS-TF RF system, the customed digital low-level RF system includes the design, implementation and debugging of DSP board, RF analog front-end board and security interlocking board, and the design and implementation of software architecture. The digital LLRF system has been successfully applied to the horizontal high power test of 166.6MHz superconducting cavity. The cavity field stability has been successfully achieved about ±0.03%(peak-peak) in amplitude and ±0.02 degree(peak-peak) in phase when the cavity field voltage is 1.2MV.

ACKNOWLEDGEMENT

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REFERENCES

[1] G. Xu *et al.*, "Progress of Lattice Design and Physics Studies on the High Energy Photon Source", in *Proc. 9th Int. Particle Accelerator Conf. (IPAC'18)*, Vancouver, Canada, Apr.-May 2018, pp. 1375-1378. doi:10.18429/JACoW-IPAC2018-TUPMF052

[2] P. Zhang *et al.*, "A 166.6 MHz Superconducting RF System for the HEPS Storage Ring", in *Proc. 8th Int. Particle Accel-erator Conf. (IPAC'17)*, Copenhagen, Denmark, May 2017, pp. 1049-1051. doi:10.18429/JACoW-IPAC2017-MOPVA079

[3] Ch. Schmidt *et al.*, "Recent Developments of the European XFEL LLRF System", in *Proc. 4th Int. Particle Accelerator Conf. (IPAC'13)*, Shanghai, China, May 2013, paper WEPME009, pp. 2941-2943.

[4] T. Schilcher, "RF applications in digital signal processing", Paul Scherrer Institute, Villigen, Switzerland