CHARACTERIZATION OF A WIDE DYNAMIC-RANGE, RADIATION-TOLERANT CHARGE-DIGITIZER ASIC FOR MONITORING OF BEAM LOSSES

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Abstract

An Application Specific Integrated Circuit (ASIC) has been designed and fabricated to provide a compact solution to digitize current signals from ionization chambers and diamond detectors, employed as beam loss monitors at CERN and several other high energy physics facilities. The circuit topology has been devised to accept positive and negative currents, to have a wide dynamic range (above 120 dB), withstand radiation levels over 10 Mrad and offer different modes of operation, covering a broad range of applications. Furthermore, an internal conversion reference is employed in the digitization, to provide an accurate absolute measurement. This paper discusses the detailed characterization of the first prototype: linearity, radiation tolerance and temperature dependence of the conversion, as well as implications and system-level considerations regarding its use for beam instrumentation applications in a high energy physics facility.

INTRODUCTION

A Beam Loss Monitoring (BLM) system is employed throughout the accelerators at CERN. The aim of the system is threefold: ensure machine protection, provide diagnostics information and aid machine setup. Different kinds of radiation monitors are employed, depending on the accelerator, measurement and expected signal, among them ionization chambers and diamond detectors. The monitors are exposed to the secondary particles shower that is initiated when a high-energy particle escapes from the beam and impacts against the vacuum chamber. The number of particles that are lost from the beam and the energy deposited in the machine components – such as the LHC superconducting magnets – are reconstructed from the output signal provided by the monitors, which are situated in studied locations along the rings, injection and extraction lines, and dump targets.

The BLM system for a large accelerator like the LHC has several channels – over 4000 – and it extends over a significant distance. The system is built in layers: the analog output signal of the monitors is digitized by data acquisition cards located in the tunnel, implementing a Current to Frequency Converter (CFC) and providing a conversion code every 40 µs. The front-end acquisition boards transmit the data to the Threshold Comparators (TC), located in VME crates on the surface, via double redundant optical links. The TCs collect, analyze the data and optionally trigger a beam abort, when losses that could potentially compromise the machine are detected. A Combiner and Survey (CS) card installed in the same VME crate receives and handles the beam abort signals. The data are then forwarded for logging and display [1].

In this context, this contribution discusses the state of the research that has been carried out at CERN, regarding the first step of the data processing outlined above: data acquisition from the monitors.

Table 1: Specifications

Parameter	
Dynamic range	1×10^6
Input polarity	double
Minimum detected current	1 nA
(through averaging)	1 pA
Linearity error	$< \pm 10\,\%$
Integration window	40 µs
Total ionizing dose	10 Mrad in 20 years

REQUIREMENTS

The requirements for the BLM front-end acquisition are listed in Table 1.

The intensity of the ionizing radiation detected by the particle monitors can span several decades, as a consequence of the characteristics of the accelerator, the operational status of the machine, the location in which the monitor is installed and the background radiation. For this reason, the different kinds of beam loss monitors designed and employed at CERN are able to provide a linear response over a wide dynamic range (DR) [2].

Since before the beginning of operation of the LHC, an effort has been made in the BE/BI/BL section to study and design a single-gain acquisition board, able to cover the whole dynamic range of the input signal [3]. This work follows the same approach as the currently operational LHC

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design and aims to provide further improved performances.

The reasons behind the requirement for double polarity operation in this design are: flexibility, reliability and resistance to interference. During machine operation, some interference – eg. an external coupling to the HV power supply line – could lead to the signal to be digitized appearing of opposite polarity for a short duration of time. The minimum requirement for the front-end design is avoiding saturation. In the case of an input range extending to both signal polarities this problem is not present. Additionally, in this case both positive and negative HV power supplies can be used to bias the monitors. The circuit topology presented here is able to digitize positive and negative charge inputs, covering the $-1.05\,\mathrm{mA}/1.05\,\mathrm{mA}$ range, without any change in configuration.

The analog to digital conversion performed by the front-end will inevitably be affected by an error. Since the data provided by the front-end is to be compared with threshold values in the TCs, the requirement for the front-end is to provide a measurement affected by an error well below the uncertainty level of the threshold values [4]. For this reason, a linearity error equal to 10% or better is required.

The integration time has an important impact on the design of the front-end: as the input current is integrated over shorter time intervals, the front-end design becomes more challenging, since the A/D conversion has to occur with the same dynamic range but over a shorter time frame. The integration time is dictated by machine requirements. For the LHC, and for this design, it is fixed to $40\,\mu\mathrm{s}$ [1, 3].

The digitized output from the front-end electronics is, after processing, compared with threshold values provided by simulations, available in terms of charge. It is hence necessary that the measurement data can be re-conducted to charge values, in Coulomb. For this reason, each front-end circuit needs to have available on board an absolute charge reference, which has to be common to all interfaces. Additionally, the charge reference shall be insensitive, within the maximum allowed error, to drifts due to temperature and ionizing radiation effects.

The radiation tolerance has an effect on the location where the front-end electronics can be installed: as the monitor is exposed to ionizing radiation, either ability to withstand the radiation effects or a cabling infrastructure to carry the analog signal to a location where the radiation level isn't of concern are required. Employing custom layout techniques and opportune design choices, the radiation tolerance that can be achieved with an ASIC allows the user to place the front-end electronics close to the detector. This option provides advantageous features: the measurement is carried out in loco, with an analog front-end loaded by the minimum capacitance, then the results transmitted digitally, reliably and at high data rate, as digital transmissions have a low sensitivity to noise and interference. The disadvantage is additional complexity inherent in analog integrated circuit (IC) design.

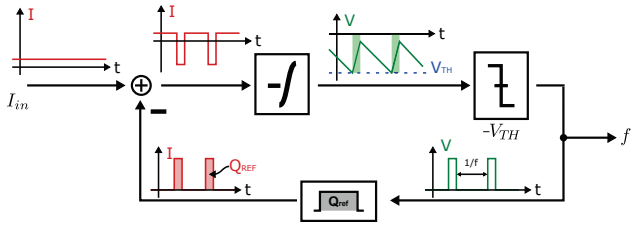

Figure 1: Charge-balance current-to-frequency conversion scheme.

CIRCUIT TOPOLOGY

Current-to-Frequency Conversion

The topology here presented has its roots in the charge-balance CFC architecture [5]. A Current-to-Frequency Converter produces a series of pulses at a frequency f_c that is proportional to the input signal level. Referring to Fig. 1, the input current is integrated until a threshold (V_{TH}) is reached, then a pulse triggers the subtraction of a fixed charge (Q_{REF}) from the integrator, and another cycle begins. The charge subtraction is implemented summing, at the input node, a current $-I_{REF}$ for a fixed time T_{REF}, generated by a timing circuit (eg. one-shot).

It is possible to show that the ideal relationship between the oscillation frequency f_c and the DC input current I_{IN} is given by Eq. 1.

$$f_c = \frac{I_{IN}}{Q_{REF}} \tag{1}$$

The charge collected in a time interval $(0,\, T_W)$ can be estimated simply counting the pulses in the same interval (Eq. 2, quantization error neglected):

$$N_c = \int_0^{T_W} f_c\, dt = \frac{\int_0^{T_W} I_{in}\,(t)\; dt}{Q_{REF}} = \frac{Q_{IN}}{Q_{REF}} \tag{2}$$

The conversion does not depend on many circuit parameters: in particular, it does not depend on the value of the threshold voltage and the capacitors values, linking output voltage and input charge in the integrator. The quantization error is stored in the integrator and added to the next measurement, allowing decreasing the minimum detectable signal increasing T_W or, equivalently, summing together multiple consecutive samples. These features make the topology interesting for implementing the front-end electronics of a BLM system.

The main limitation is the dynamic range that can be achieved: at the upper end, increasing the input level, bandwidth limitations will prevent the generation and summation of an accurate charge packet, and, as a result, the minimum value for Q_{REF} is fixed. At the lower end, the input current can decrease until the point where the accumulated charge in T_W is below Q_{REF}, minimum detectable signal, prompting the designer to reduce further the value of the reference charge, but Q_{REF} can only be reduced until the

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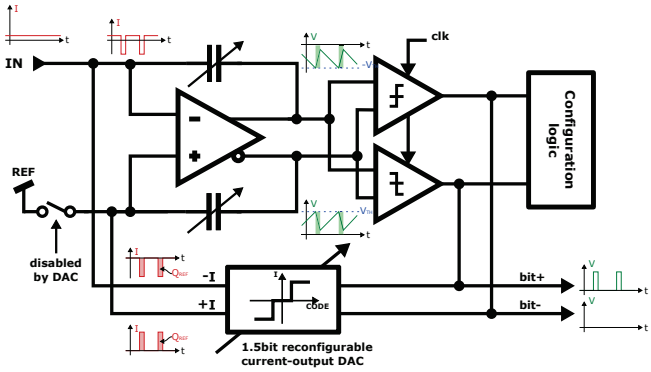

Figure 2: Circuit topology.

minimum value due to the aforementioned bandwidth limitation is met.

To further increase the dynamic range, it is possible, in principle, to extend the measurement time T_W, lowering the minimum detectable signal, see Eq. 2, but in many applications, such as the one under consideration, that is not an option.

A different approach has to be adopted to cover a dynamic range of six decades with a 40us integration time. Other solutions have been proposed in the literature: the CFC board employed in the LHC BLM system pairs the frequency conversion with a 12bit pipeline ADC, increasing the DR of the CFC converter of a more than three decades, but requires matching of the CFC and the ADC data [3]. See also [6, 7].

Circuit Topology

Since the maximum frequency at which the charge injection can be performed is behind the dynamic range limitation, and the frequency is set by Q_{REF} (Eq. 1), the input dynamics can be extended adjusting the reference charge to keep the front-end in the operative frequency range.

A simplified diagram of the circuit topology is shown in Fig. 2. Similarly to the CFC, the analog part of the circuit provides current integration, detection of threshold crossing and injection of charge packets to balance the integrator, implemented through a fully-differential integrator, with configurable feedback capacitance, two dynamic comparators and a configurable three-level current-output Digital-to-Analog Converter (DAC).

The integrator is fully differential (differential input / differential output) to take advantage of the better power supply rejection of differential structures, minimize the influence of noise, ease the requirements on the comparators and to reduce even-order harmonic distortion. An adjustment in the integrator is necessary: the value of the feedback capacitance needs to be scaled with the reference charge of the converter, or the requirements on comparators resolution would become challenging.

Additionally, due to the small unit capacitance, the routing parasitic capacitance can have a considerable influence on the ratio of feedback capacitances, especially for the highest sensitivity setting. To minimize this effect, the threshold voltages start at 1V for the highest sensitivity configuration and are decreased of a factor two for every sensitivity step, correspondingly, the capacitor values can be increased by the same factor.

Table 2: Subdivision of the Dynamic Range in Sub-ranges, in Terms of Absolute Values of DC Currents

Sens.	Min	Max	Overlap	DR
0	1 nA	200 nA	N/A	256
1	160 nA	4.1 µA	1.6	25.6
2	2.56 µA	65.5 µA	1.6	25.6
3	41 µA	1.05 mA	1.6	25.6

The comparators are responsible for generating the signals that trigger the charge injection: an additional one is present in Fig. 2 compared to Fig. 1, to allow operation with positive and negative inputs. The third output level in the DAC is introduced for the same reason. The comparators are clocked at 12.8 MHz and provide two symmetric differential thresholds.

The circuit-wide configuration is set by a logic circuit that monitors the comparators output. A first version of this logic was implemented on chip with a Triple Modular Redundant (TMR) design, while configuration inputs are available to disable it and implement the logic off-chip (for example in an FPGA). This strategy has been useful for testing the device and optimizing the algorithm.

The modulator input ranges for each sensitivity are listed in Table 2: an overlap factor equal to 1.6 has been ensured between the ranges to allow an hysteresis in the transitions.

A robust scheme has been implemented to provide the reference charge the A/D conversion: the charge packets are generated by enabling the current-output DAC according to a time reference provided by a 12.8 MHz clock, generated off-chip with a temperature-compensated piezoelectric oscillator. The DAC is biased by a current reference embedded on chip, based on a 1.2 V radiation-hardened band-gap reference, to minimize temperature dependence, with an optional external resistor for LSB step calibration.

The output code is generated counting the charge injections events, grouped by reference charge value, with a positive sign when it is a positive charge that has been injected, and a negative sign when a negative charge has been injected. The final output code is given by the sum of the weighted contributions of each reference charge, as shown in Eq. 3.

$$\left[\frac{Q_{IN}}{Q_{REF,0}}\right]_{\mathrm{D}} = N_{c,0} + \underbrace{\left[\frac{Q_{REF,1}}{Q_{REF,0}}\right]_{\mathrm{D}}}_{2^4} N_{c,1} + \underbrace{\left[\frac{Q_{REF,2}}{Q_{REF,0}}\right]_{\mathrm{D}}}_{2^8} N_{c,2} + \underbrace{\left[\frac{Q_{REF,3}}{Q_{REF,0}}\right]_{\mathrm{D}}}_{2^{12}} N_{c,3} \quad (3)$$

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The ratio of the reference charges has been opportunely selected to be a power of 2, hence the weighing operation is performed with a bit shift.

The ASIC has an additional operation mode: the integrator outputs are connected to an ADC and the configuration of the front-end is set externally by the user, implementing a setup similar to [3], with the additional advantages of having a selectable full-scale charge (8 pC, 164 pC, 2.56 nC or 42 nC, adjustable within 20 %) and double polarity operation. The fully differential integrator outputs are matched to common radiation-tolerant ADCs, such as [8]. This mode provides an alternative radiation-tolerant solution.

FIRST PROTOTYPE AND MEASUREMENT RESULTS

The prototype was designed using a three-metal 0.25 µm CMOS technology and then ported to a six metal stack to be submitted in a Multi-Project Wafer (MPW). The prototype has two channels, each one as shown in the diagram in Fig. 3.

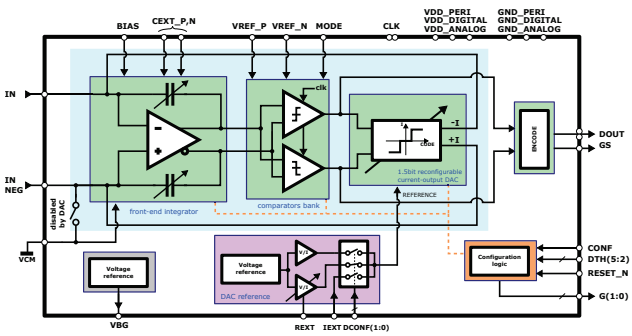
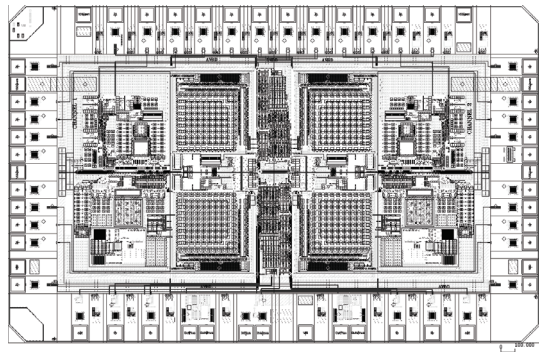


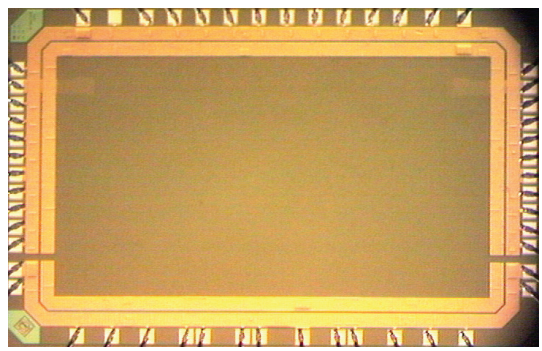
Figure 3: Diagram of a single A/D channel.

The chip layout and a full micrograph are shown in Fig. 4a and Fig. 4b, respectively. In the layout, it is possible to see two channel arranged horizontally, with the analog part on the outside and the digital circuitry in the middle, separated from the sensitive parts. Considering the channel on the left side, the left half of the analog part consists of the DAC and the charge reference, on the right hand side it is possible to see the capacitors and the amplifier in between. On the right of the amplifier there are the comparators, which bridge the analog and the digital parts. The chip size is 2.4 mm x 3.775 mm.

The test-bench setup has been developed as follows: an analog board hosts the DUT, providing separated analog, digital and pad power supplies, biasing and voltage references. The analog board is connected to the instrument providing the test stimuli and to an optional secondary board with an Altera Cyclone IV FPGA to set the configuration remotely and provide the measurement results over TCP/IP. A set of software tools have been developed to read, process and display the data, and control the instruments through a GPIB-TCP/IP bridge.



(a) Layout of the chip.



(b) Microscope picture.

Figure 4: Layout and microscope picture of the fabricated prototype.

Table 3: Device Characterization Summary

A/D converter	
Integration time	40 µs
Input current range	−1.05 mA to 1.05 mA
Input charge range	−42 nC to 42 nC
Offset	12 fC
(currently WIP)	300 pA over 40 µs
Default LSB step	50 fC ±20 %, adjustable
Dynamic range	120 dB
Linearity error	< ±5 %
Peak S/N ratio	53 dB
SFDR at 999Hz, 1mA	50 dB
Total ionizing dose	10 Mrad(Si)
Supply voltage	2.5 V
Clock	12.8 MHz
Power	40 mW
Reference charge	
Drift with TID	3 % at 10×10^6 rad(Si)
Drift with temperature	< 600 ppm/°C

The results from DC, AC, temperature and radiation tolerance (TID) measurements are summarized in Table 3.

The linearity error is defined as $2(y_m - y_{id})/(y_m + y_{id})$, where y_m is the measured output code and y_{id} is the output code expected by fitting the measurement points. It is limited by different effects: at low input signals, the current

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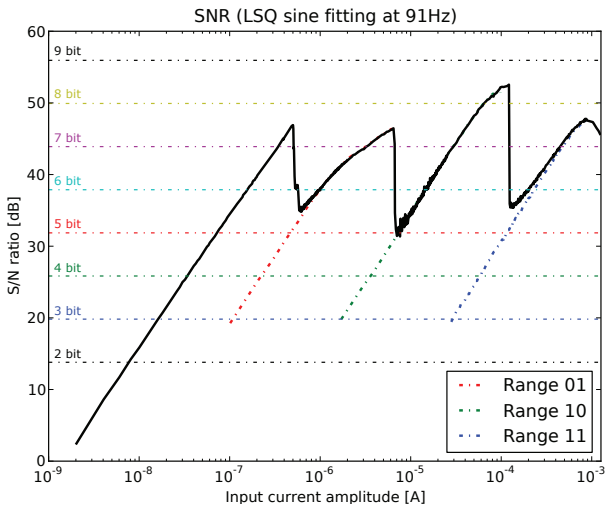

Figure 5: Measured SNR.

leakage of the input structures provide an additional charge that is superimposed to the test stimulus and introduce a measurement error. As the input signal increases, the front-end switches between different configurations (sensitivities). The transistor matching imperfections introduce a different linearity error for every input signal range. Near the full-scale, dynamic effects cause an additional error in the injected charge. Overall the linearity error is within $\pm 5\,\%$.

Additionally, in the current setup, there is a spurious input signal of variable amplitude below $1\,\mathrm{nA}$. The reason is probably a ground loop effect and it is currently being investigated. Because of that, the offset in Table 3 is $12\,\mathrm{fC}$ ($300\,\mathrm{pA}$ integrated for $40\,\mu\mathrm{s}$), the expectation is that the effective device offset is $40\,\mathrm{aC}$ ($1\,\mathrm{pA}$ integrated for $40\,\mu\mathrm{s}$).

Figure 5 plots the measured SNR versus input amplitude for a sinusoidal current stimulus at a frequency equal to $91\,\mathrm{Hz}$. In the figure, the measurement is compared with the theoretical peak SNR for traditional A/D converters and with the measured SNR of each configuration, obtained disabling the configuration logic. The SNR increases with the amplitude, as an effect of the reduced weight of the quantization error, until the amplitude falls in the next range: at this point the sine wave is partially digitized with a coarser quantization step and, correspondingly, the SNR drops. The same effect repeats every time the front-end configuration changes.

FFT spectra were acquired with a sinusoidal input current at a frequency close to $1\,\mathrm{kHz}$ and amplitude equal to $1\,\mathrm{mA}$. The measured SFDR is $50\,\mathrm{dB}$ and it is limited by third order harmonic distortion.

The radiation tolerance – Total Ionizing Dose (TID) effects – has been investigated at CERN in an X-ray irradiation facility. A tungsten tube provided an X-ray beam with a peak at $20\,\mathrm{keV}$ and a dose rate of $47.5\,\mathrm{krad(Si)/min}$. The characteristics of the device have been measured at logarithmically spaced total dose values, up to $10\,\mathrm{Mrad(Si)}$, followed by a 1 week annealing cycle at $100\,^{\circ}\mathrm{C}$. From the beginning to the end of the irradiation cycles, the full scale charge drifts of approximately $3\,\%$.

Measurements taken in a climatic chamber in the $13\,^{\circ}\mathrm{C}$-$43\,^{\circ}\mathrm{C}$ range showed a negative temperature dependence of the reference charge with the temperature, in absolute value below $600\,\mathrm{ppm}/^{\circ}\mathrm{C}$ and in reasonable agreement with simulations (within $30\,\%$). An external resistor can be provided to further reduce the temperature coefficient.

CONCLUSIONS

The $120\,\mathrm{dB}$ DR ASIC presented provides a compact and flexible solution to convert a wide dynamic range charge to a digital code. The IC operates DC-coupled to the detector, it has an on-chip charge reference and it digitizes positive and negative currents. The ASIC has been irradiated with X-rays up to $10\,\mathrm{Mrad}$ with only minor changes in the circuit performance.

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