SYSTEM ARCHITECTURE FOR MEASURING AND MONITORING BEAM LOSSES IN THE INJECTOR COMPLEX AT CERN

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Abstract

The strategy for beam setup and machine protection of the accelerators at the European Organisation for Nuclear Research (CERN) is mainly based on its Beam Loss Monitoring (BLM) systems. For their upgrade to higher beam energies and intensities, a new BLM system is under development with the aim of providing faster measurement updates with higher dynamic range and the ability to accept more types of detectors as input compared to its predecessors. In this paper, the architecture of the complete system is explored giving an insight to the design choices made to provide a highly reconfigurable system that is able to fulfil the different requirements of each accelerator using reprogrammable devices.

INTRODUCTION

During the upgrade of each injector line at the European Organisation for Nuclear Research (CERN), an up-to-date Beam Loss Monitoring (BLM) system will be included for the monitoring of the beam losses and machine protection. That is, apart from the high reliability and availability expectations from the system, the architecture chosen should provide a generic, highly configurable and high-performing system.

The acquisition part should provide the ability to accept several detector types as input. In the majority of the cases, it is foreseen to use ionisation chambers similar to those developed for the LHC. Nevertheless, several other types, e.g. secondary emission monitors, diamonds and Cherenkov detectors, will need to be used also in some locations to cover particular cases. For the transport of the signal between the detector and the front-end coaxial double shielded cables are employed and wherever possible all cables pass through enclosed cable trays. That is, make use of any possible means for noise reduction.

The digitisation of the detector current output will use a new design concept and is currently under implementation. The input channel circuit should be able to measure a current input from 10 pA to 200 mA. That is, a dynamic range of 10^{11}.

Further, the processing part of the system will combine the information gathered by each channel and keep several moving integration windows between 2 μs and 1.2 s. The calculated values for each channel will be checked continuously against predefined threshold values both at the hardware and software level, as well as will be forwarded in the control room and databases for online observation and later analysis. The BLM system, through its direct connection to the beam interlock system, will have the ability to either block all upcoming injections, when the machine protection thresholds get exceeded, or selectively block specific upcoming injections, by tracking losses for each individual beam cycle destination separately.

The system is making use of reprogrammable devices, i.e. Field Programmable Gate Arrays (FPGA), to allow flexibility and target all injectors' requirements. A block diagram of the architecture of the system can be seen in Fig. 2.

ACQUISITION ELECTRONICS

The acquisition electronics are comprised by the digitiser modules, the control module and the crate that provides the hosting and interconnections.

Acquisition Crate (BLEAC)

The acquisition crate (BLEAC) can support up to eight 6U sized acquisition modules. It is based on a custom designed backplane that provide connection for 64 input channels and to each inserted module the needed connection to the power supply voltages and control signals.

The crate's backplane provides in addition support for direct injection of a remotely adjustable reference current either via a dedicated input or via an internal current source. To achieve this each channel's input pass through a relay contact. This option will be used in the future firstly for an automatic calibration procedure and secondly for a channel connection check. That is, the system will be able to guarantee the full dynamic range and maximum linear response possible of each channel, as well as check regularly the complete channel's connection and its ability to trigger the beam interlock.

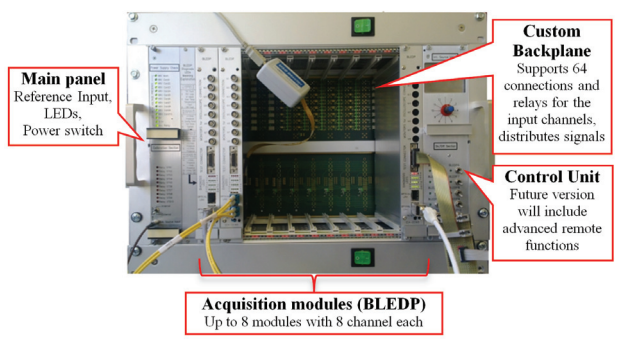

Figure 1: Picture of the BLEAC acquisition crate.

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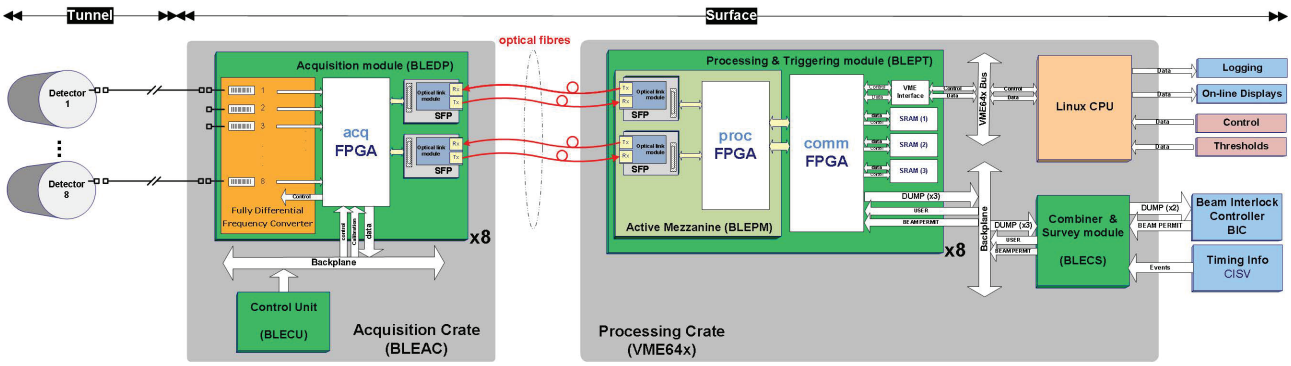

Figure 2: Overview of the BLM system under development for the Injector Complex at CERN.

The reliability of the system and its correct connection is further enhanced by the options to provide the geographical address of each connected module in the crate and the monitoring of the high voltage power connection.

Acquisition Module (BLEDP)

The acquisition part has the ability to use two methods: (a) based on a fully differential integrator principle assisted by an ADC that can be used in the range between 10 pA and 30 mA and (b) a direct measurement using a fast ADC to be used in the range between 20.3 μA and 200 mA. A picture of the prototype module is shown in Fig. 3 and more information on the methods used can be found in [1].

Depending on the input current level, an FPGA embedded in this module controls which circuit will make the measurement in the next acquisition period. This allows reaching an enhanced dynamic range that can be explored with continuous measurements having no blind time making it an additionally favourable option for critical mission applications like machine protection.

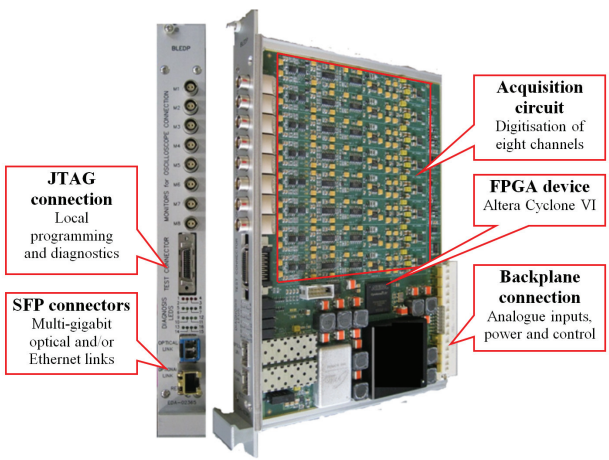

Figure 3: Picture of the BLEDP acquisition module.

Most of the control operations of the analogue circuitry are handled by the FPGA device. That is, the FPGA defines the start and stop of the acquisition period, it keeps a count of the number of pulses occurred in the acquisition period, clocks the ADC circuitries, directs which acquisition technique is active for each channel and makes differences of the recorded ADC values. Finally, it processes the data, i.e. merges the values acquired in the counter and the ADCs, and provides the integral of the losses measured for each channel over the last 2 μs period. More details on the merging algorithm employed can be found in [2].

The advantage of this configuration is that there is no need of a manual gain selection. The two modes partially overlap and the switch between the 2 ranges is managed directly by a dedicated part in the FPGA logic that observes the input data in regular intervals. If the maximum level of the low range measurement method is reached, the FPGA switches the circuit to the high range method. Consecutively, when the value of the high input range method falls below a threshold, the FPGA switches the circuit back to the low range mode. The sum of all parts acquired is calculated in real-time internally in the FPGA and a sample summarising the beam losses measured for each channel in the last 2 μs is published.

PROCESSING ELECTRONICS

The processing modules are hosted in VME crates together with the front-end computer and timing receiver modules.

VME Crate

The crates are making use of the extended VME64 [3] specification. This extension defines a set of features that can be added to VME and VME64 boards, backplanes and sub-racks. Some of the features included are a 160-pin connector, a P0 connector, and geographical addressing.

In order to make the best out of those features, CERN Beam Instrumentation group has defined a custom-made backplane for the P0 connector [4]. Some of the features it provides include connections to form two daisy-chain links between the processing modules, general purpose I/Os, broadcast lines for distributing the timing events, and additional supply voltage outputs.

The system makes use most of those features, e.g. for broadcasting timing events to the inserted modules, allowing synchronisation of the acquisitions with the beam cy-

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cles, or for daisy-chaining their beam permit signals, augmenting the reliability by minimising the number of connections.

Processing Modules (BLEPT)

Each VME crate can accommodate up to eight processing and triggering (BLEPT) modules. These modules are comprised by one of the standard CERN Beam Instrumentation carrier boards, i.e. the DAB64x [5], and an active mezzanine with an FPGA device, i.e. Altera's Cyclone IV with 150K logic elements. The mezzanine also provides two SFP connectors that can accept standard modules. Two types are expected to be used depending on the configuration required. That is, the bidirectional multi-gigabit optical link or the gigabit Ethernet type.

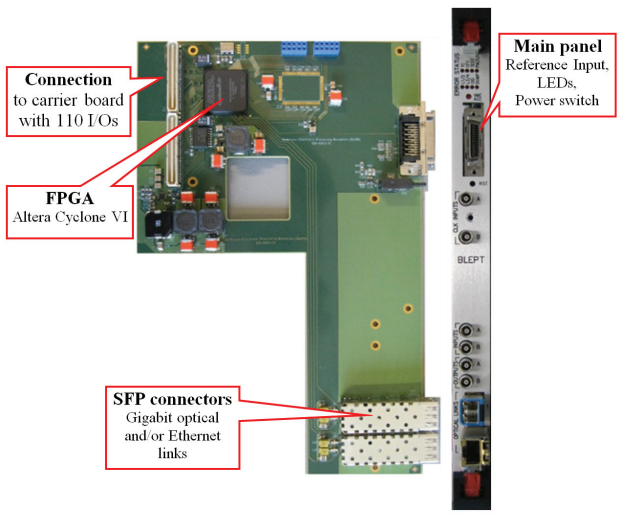

Figure 4: Picture of the BLEPT's Active Mezzanine.

The mezzanine's design shares many of the digital components found in the acquisition module. That is, it makes use of the same FPGA device and SFP modules allowing quick development and guaranteed interoperability. Figure 4 shows a picture of the prototype version of the mezzanine's PCB.

The backbone of the carrier board is also an FPGA. In this system's configuration it is used to handle the communication with the front-end CPU and the interlock lines. This involves the publishing of the processed data and statuses information collected from the whole chain of modules to the VME communication channel, and directing the final decisions regarding beam injection and circulation.

The board provides two distinct connections via the VME P0 connector for the beam interlocking features. With the appropriate parameters set, the FPGA device will direct the requests from each of its connected monitors to one of the outputs. In this way, it will be possible to combine detectors from several locations but separate their requests for blocking beam injections by destination.

Combiner and Survey Module (BLECS)

The final receiver of the two beam permit lines is the Combiner and Survey module, named BLECS, and is located at the last slot of the processing crate. The two beam permit lines are daisy chained through each of the processing modules using the custom-made backplane in the crates. If any of the modules decides to break any of these lines a beam interlock request will be given to the Beam Interlock System [6].

As an additional reliability feature, those lines will be used by the BLECS module to provide a continuous supervision of the operation of the processing modules in the crate. Thus, it will be able to discover immediately a module's disconnection from the crate, failure in the power supply or error in the configuration of the FPGA and request an interlock for each of those cases.

Finally, the BLECS will have also the task of distributing the synchronisation signals to the beam cycle timing events to each of the processing modules in the crate, as well as, initiating all the system sanity checks procedures and confirm the successful results on regular intervals.

INSTALLATION

Noise Immunity

In order to cover the large dynamic range requested, especially in the lower end where external interference could be critical, several measures have been taken to provide a high level of noise immunity in the system.

The screen of the high-voltage power cable used is grounded on the power supply side and open on the detector side to remove noise from any possible ground loops. The return path connects through the signal cable.

For the transport of the induced signal a coaxial double shielded cable is being used. The internal screen wiring will be used to provide shielding from low frequency noise and will have a connection to the ground only on the electronics side and have the detector side "floating". Consecutively, the external screen wiring will be aimed to provide shielding from high frequency noise and will have a ground connection from both ends. Figure 5 shows a schematic diagram of the cables and the connections realised.

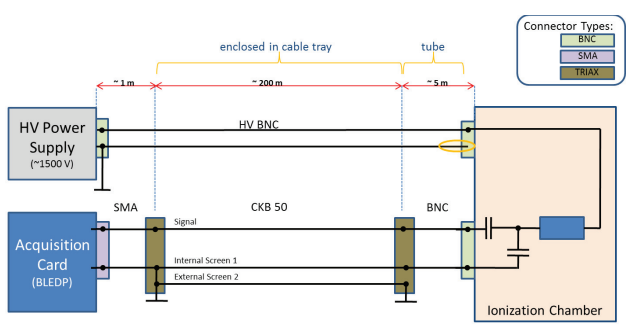

Figure 5: Schematic diagram of the cabling installation.

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Finally, the acquisition electronics are electrically separated from the rest of the system hosted in a dedicated crate isolated from noisy parts like the front-end CPUs. The acquired signals are transmitted to the processing crates using optical links.

Reliability Enhancements

Due to the criticality of the system several measures have been taken also though the installation configuration to augment the reliability of the system.

Each of the detectors is powered using a separate cable. In the case of cable disconnection, e.g. due to connector failure, cable cut or erroneous manual intervention, the loss of the monitoring ability will be isolated to a single detector. The disconnected detector will be discovered in the next iteration of the regularly executed connectivity check, i.e. in less than 24 hours.

For the detectors' powering, a secondary power supply is installed in parallel to the main power supply, but at a lower voltage of approximately 50 V. Therefore, the secondary will be idling without the need of supplying any current up to the case of failure of the main supply.

STAND-ALONE MEASUREMENT SYSTEM

For assisting the development phases as well as later serving as a stand-alone measurement system, the BLEDP's reconfigurable FPGA device is exploited further by embedding a soft-core CPU with a custom-made server. The server exposes on-demand, through a Gigabit Ethernet connection and the TCP/IP protocol, different types of data in the network. A block diagram of this setup of the system is shown in Fig. 6.

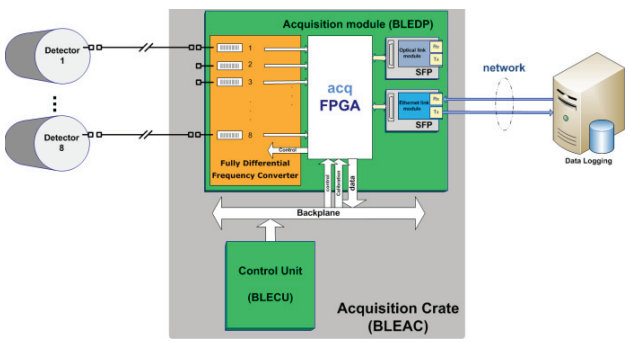

Figure 6: Block diagram of the system configuration dedicated to detailed measurements using a gigabit Ethernet connection.

The additional complexity in the development of this version of the system was mainly in the communication protocol and the accompanying client application realised with the purpose of commanding, collecting storing and viewing the different types of data. The hardware modifications needed are really simple since the gigabit Ethernet module replacing the optical link in the SFP connector can be connected directly to the cable network and includes the additionally need hardware components.

The TCP/IP and UDP stacks are integrated in the FPGA firmware through a NIOS-II system-on-chip and the Triple Speed Ethernet (TSE) IP core provided by Altera Corp.

The server included in the FPGA has been developed with the C programming language and has been realised to accept commands, collect, package the data requested and finally transmit them to the connected client. The client application has been developed with the JAVA programming language and apart from sending the commands and requesting for specific data, it is also able to display online summaries of the received information and store and display with more processing capabilities the received data.

More information on the development of the measurement version of the system can be found in [7].

SUMMARY

For the upgrade of each injector line at the European Organisation for Nuclear Research (CERN), an up-to-date Beam Loss Monitoring (BLM) system is under development with a highly versatile architecture. All modules employed host reprogrammable devices that can be tuned to match the requirements of each machine. Special attention has been given for the system to provide detailed low noise measurements and high reliability interlocking features.

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