DEVELOPMENT OF NEW BPM ELECTRONICS FOR THE SWISS LIGHT SOURCE

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Abstract

PSI is currently developing new BPM electronics for the Swiss Light Source (SLS). Although the present "DBPM1" system that was designed 12 years ago still allows to achieve excellent beam stability and uptime, the development of a new system is motivated by long-term maintenance, improved performance in line with increasing user requirements, and new features and functionality provided by latest electronics technology. The new system is based on a generic modular BPM electronics platform developed by PSI that will also be used for linac based Free Electron Lasers (FEL) like European XFEL and SwissFEL. The hardware and firmware architecture of the present prototypes as well as first test results will be presented.

PRESENT SLS BPM SYSTEM

The Swiss Light Source is operational since eleven years and delivers high brightness photon beams to experimental stations. One of the most important properties of the machine is high stability and reproducibility of the electron orbit at the location of the radiation source points. The high stability is maintained by a fast global orbit feedback (FOFB) [1]. The feedback consists of 72 BPMs and 72 corrector magnets grouped in 12 sections as presented in Fig. 1.
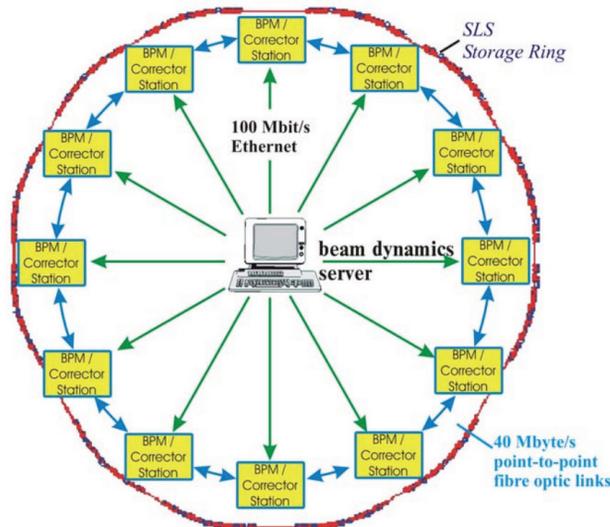
Figure 1: Overview of SLS global orbit feedback.

Each section typically contains six BPMs. The horizontal and vertical position of the six BPMs is calculated in a single DSP board and the data is exchanged with adjacent sections through fibre optic links. This structure allows, on the same DSP board, calculation of the current set values for six vertical and six horizontal dipole corrector magnets from 18 beam position readings, with an update rate of 4 kHz.

BPM UPGRADE DEVELOPMENTS

The planned upgrade of BPM system is motivated by long-term maintenance, improved performance and future user requirements. By using the latest FPGA, ADC and RF technology, the resolution and latency of the new BPM system can be improved significantly. In contrast to the present system where the 500MHz signals from the button pickup electrodes are mixed to a 36MHz IF that is sampled by 12-bit ADCs at 31MSPS, the new electronics will (under-)sample the 500MHz pickup signals directly. The system will be based on a generic modular electronics framework developed at PSI [2]. While the present BPM digitizer boards just provide button pickup signal amplitudes and the FOFB DSP boards are used to calculate a calibrated beam position and related data like RMS values, the new BPM electronics will take over this functionality and provide calibrated position data to the control system and to a new global fast feedback network via multi-gigabit fiber optic links.

General Layout

Figure 2 shows the different modules of the present prototype electronics for the new SLS BPM system. The 500MHz signals of the button pickup electrodes are received by an RF front-end (RFFE) that performs amplification and filtering (no mixers). The RFFE is connected to four 16-bit ADCs of a mezzanine, where two mezzanines are plugged onto one FPGA carrier board (GPAC = Generic PSI ADC Carrier).
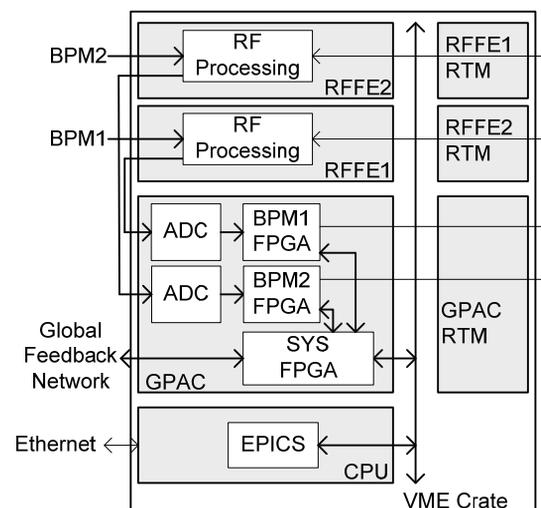
Figure 2: Block diagram of the new SLS BPM system.

Digital Electronics

Figure 3 presents a photo of GPAC board. Two so-called "BPM" FPGAs on the GPAC are used for application-specific tasks, i.e. to perform digital downconversion, calculate beam positions for different bandwidths, etc.

Figure 3: Photo of the GPAC carrier.

The "System" FPGA on the GPAC contains generic firmware used for different BPM types (SLS, SwissFEL, E-XFEL), e.g. the control system interface. GPAC and RFFEs are using the VME64x form factor that provides the desired amount of PCB area to efficiently implement the required functionality. In addition to a VME64x interface for use in VMEbus based environments like at SLS, the GPAC also provides several multi-gigabit interfaces that support different protocols (Ethernet, PCIe, custom protocols) for control, timing and feedback system integration. This allows to use the BPM electronics also in non-VME environments, where one GPAC with up to four RFFEs can be plugged into a cost-efficient customized standalone crate called MBU (Modular BPM Unit) that was primarily designed for the E-XFEL BPM cavity and button BPM systems.

RF Front End Electronics and ADC

Our modular design approach, where digital back-end, ADC and RFFE are separated on three PCBs with standardized interfaces, allowed us to get a first prototype for the new SLS system just by recombining already existing FEL BPM hardware. For the first performance tests and firmware development we used the GPAC FPGA carrier board with a 6-channel 16-bit 160MSPS ADC mezzanine designed for the European XFEL undulator cavity BPM, and with a 500MHz RFFE that we currently use for the SwissFEL Test Injector Facility (SITF) – see photo in Fig. 4. This RFFE is used for resonant stripline BPMs [3] where we have a special 5GSPS waveform digitizer that is not suitable for the SLS ring BPMs since it only supports recoding of 1024 samples in single-shot mode with limited (~10Hz) rep rate.
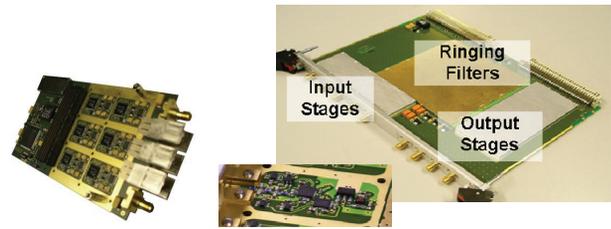
Figure 4: Left: Photo of a 16-bit ADC mezzanine card. Right: Photo of a 500MHz Stripline BPM RFFE.

Although the performance we obtained with this setup is already very promising (see measurement results in a following section), we are currently developing the first prototype of an RFFE that is optimized for the SLS. Figure 5 shows its block diagram. While the stripline RFFE only has on-board temperature sensors that would allow a feed-forward correction of temperature-induced beam position drift, the new RFFE has on-board heaters and temperature sensors that enable active temperature stabilization. In addition, we have foreseen a pilot tone with programmable frequency and amplitude that can be used both for self-tests and for off-line or on-line calibration.
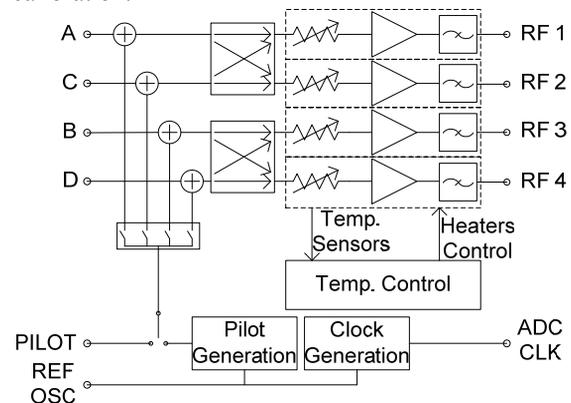
Figure 5: Block diagram of SLS RFFE.

A crossbar switch allows to swap the pickup signals of opposite buttons at the RFFE inputs to average out drifts and nonlinearities by re-swapping the inputs in the BPM FPGA. Further improvements include an increase of the gain range beyond the 31.5dB of the stripline RFFE.

Firmware Implementation

The advantage of FPGA technology gives great flexibility in project customization according to the machine specific requirements [4]. Growing size and speed of state-of-the-art FPGA chips allows implementation of high resolution computations and more features in a single chip. Therefore, the complete ADC signal processing from raw data to calibrated beam position and charge was implemented in the BPM FPGA (see Fig. 6), using only VHDL code for all computations, with the goal to make the design portable, compact, fast and efficient.
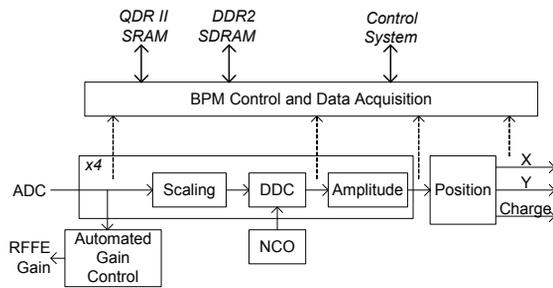
Figure 6: Block diagram of the BPM firmware.

The fast ADCs directly sample the 500MHz RFFE output signals at an adjustable sampling rate up to 160MSPS. Unlike the present system there is no analog intermediate frequency (IF). The aliasing effect converts 500 MHz to IF of e.g. 20 MHz at 160MSPS. The sampled ADC data is scaled in order to compensate for channel amplitude imbalance and then processed in a digital downconverter (DDC). The DDC converts the IF frequency to base band, where both the bandwidth and data decimation rates can be changed during operation e.g. via the control system interface. The DDC I and Q (in-phase and quadrature) output values of the DDC are converted to the signal amplitude using the CORDIC algorithm. The whole signal processing chain from ADC data to amplitude calculation is replicated four times for each RF channel. The very last VHDL component calculates X and Y position of the beam in single-precision floating point format, as well as the charge as fixed-point integer.

The BPM Control and Data Acquisition firmware component shown in Fig. 6 has two main functions. It allows to read and set parameters of the signal processing chain during run time, including a reconfiguration of the DDC and its FIR filters, thus allowing to adapt the system to different accelerators without having to modify and recompile the FPGA firmware. Furthermore, the component has interfaces to memory chips connected to the FPGA. The QDR II SRAM of the present GPAC prototype is able to collect 512k samples per ADC at the sampling frequency rate. This allows detailed on-line analysis of the RFFE output signal in the frequency domain. The second DDR2 SDRAM records charge and position data, where the max. duration depends on the update rate of the output data. For the final version of the GPAC that is currently being developed [2], we are planning to use DDR3 RAM both for ADC raw data and position/charge data storage, thus supporting sampling depths much larger than 512k samples.

The Automated Gain Control component shown in Fig. 6 measures level of the ADC signals and controls the gain level of the RFFE channels.

Digital Downconverter

The digital downconverter was implemented as a cascade of several filters. The block diagram is presented in Fig. 7. The IF waveform from ADC is mixed with sine and cosine waveforms of the same frequency generated in a numerically controlled oscillator (NCO) component.
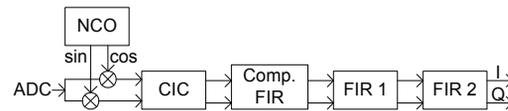
Figure 7: Block diagram of the digital downconverter.

The frequency generated by the NCO module can be changed in run time with 2 Hz resolution. Together with the arbitrary ADC clock frequency generated in RFFE this gives possibility to optimize the frequencies as necessary to avoid aliasing of unwanted frequency components in the base band. A cascaded integrator-comb (CIC) filter was chosen as a first filtering stage after the mixer. Due to simplicity of CIC implementation in FPGA it can run at the ADC clock frequency of e.g. 160MHz. The 5th order of CIC is a compromise between desired high rejection of aliased images and possible size of the accumulator in the integrator part (48 bits in a DSP48E primitive). As shown in Fig. 8, the drawback of a CIC filter is a slope in the pass band. Therefore the CIC filter is followed by a compensation filter implemented as 8th order finite impulse response (FIR) filter with decimation ratio of 2. The resulting amplitude response characteristic with a very flat passband without slope (see Fig. 8) minimizes e.g. the dependency of the measured betatron oscillation amplitude on the betatron tune for beam studies in turn-by-turn mode.
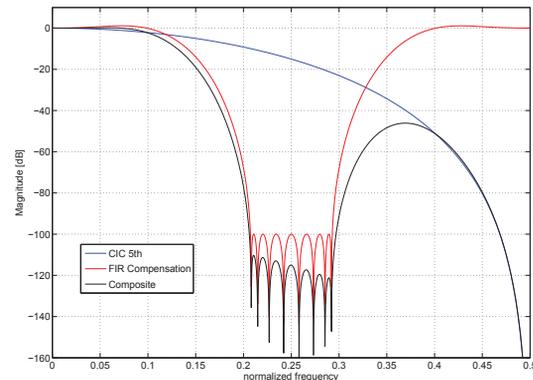
Figure 8: Magnitude response of CIC, compensation and composite filters.

The compensation filter eliminates the decaying characteristic of CIC filter in base band. The shape of the compensation filter is optimized to give an overall flatness of the DDC better than 0.01 dB in a frequency range from 0 Hz to $0.01 f_s$. For $f_s = 160$MHz the upper frequency corresponds to 1.6 MHz which is still higher than the base band used for feedback. The composite filter gives more than 100 dB dynamic range in the base band.

The composite filter is followed by two 1024-tap FIR filters with decimation from 1 to 16. The filter order can vary from 1 to 1024 where order 1 corresponds to bypassing of the filter. These filters are implemented with a single multiplier each. This limits the maximum order of the filter to the product of decimation factor of previous stages and the current FIR filter. The total

decimation of the downconverter is from 8 to 16384 which corresponds to an output update rate from 20MHz to 9.765kHz at f_s = 160MHz. The decimation ratios of CIC, FIR1, and FIR2 can be changed together with the coefficients of FIR1 and FIR2 in run time. The run time parameter change makes the DDC flexible, with the possibility to adapt the parameters to a given operation mode.

MEASUREMENTS

Test Setup

Figure 9 shows the setup that we used for first lab tests of prototype hardware and firmware.
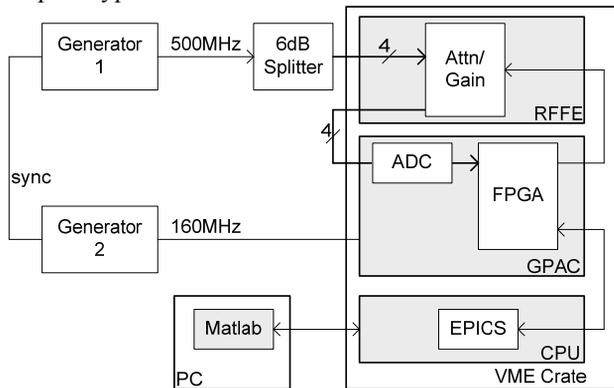
Figure 9: Block diagram of the BPM test setup.

The EPICS server running on a commercial VME CPU board provided the interface between the GPAC firmware and Matlab scripts running remotely on a PC. All settings for the DDC were generated in Matlab using its signal processing toolbox.

Measurement Results

The first step was to measure position and charge in order to test the DDC and to see where and how much the performance of the non-SLS-specific hardware needs to be improved for the final, SLS-specific electronics version.
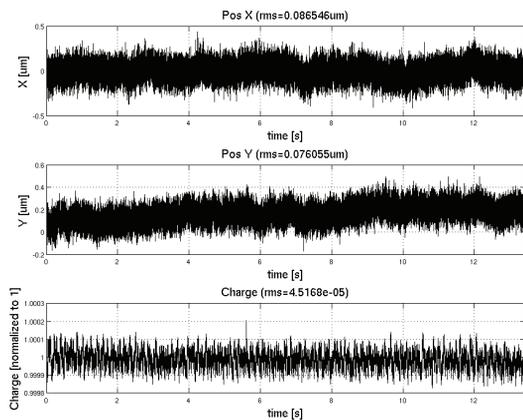
Figure 10: Short term position and charge measurement.

Figure 10 presents plots of position and charge taken over more than 13 seconds with update rate of 39.0625 kHz. The update rate is equal to 160 MHz divided by overall decimation factor of 4096. The pass band of the DDC is 2 kHz. The measured accuracy of the system is better than 100 nm, using 10 mm as a geometry factor.

Figure 11 shows the dependency of the measured position and charge on the ambient temperature.
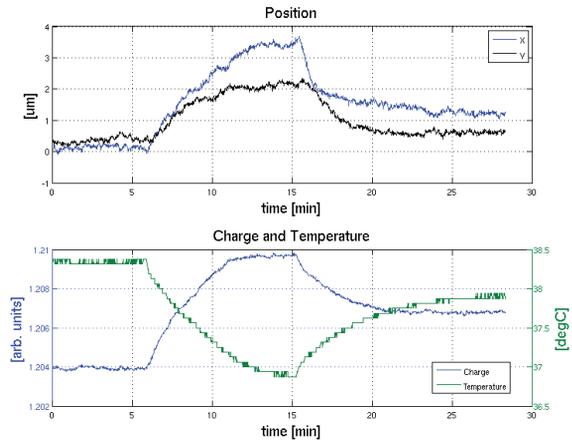
Figure 11: Position and charge versus temperature.

Position, charge and temperature of the RFFE board were measured over 28 minutes. The fan level of VME crate was increased in minute 6 to generate a temperature drop in the crate. In minute 16 the fan level was reduced back to its initial value. Obviously the temperature change of the board has influence on channel amplitudes and in case of charge it is ~0.3% per $^{\circ}$C. In case of position measurements the temperature dependency is in the order of 2µm/$^{\circ}$C.

The last measurement was done to check if position change is linearly dependent on temperature change. Figure 12 presents the amplitude change versus temperature change of the RFFE board.
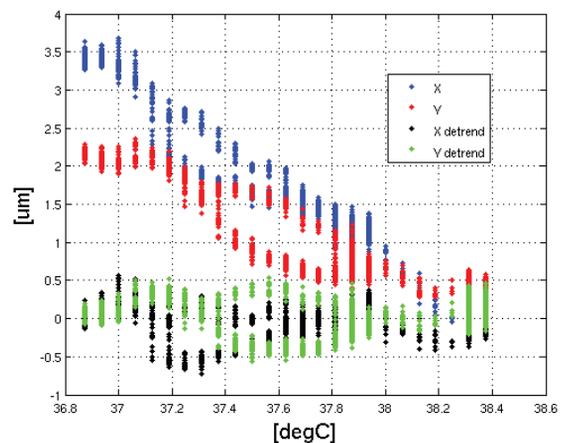
Figure 12: RFFE channel amplitude versus board temperature.

As one can see the dependency is linear but with slightly different coefficients. The blue and red curve

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presents the original data. The hysteresis visible on both is due to fact that the temperature sensor was not located directly on the RFFE board. Knowing the coefficients of temperature dependency the position can be corrected in feed forward mode in firmware as presented by black and green curves. In this case the measurement accuracy would be improved by at least factor of 5. However active temperature control of the new RFFE board should give better results due to temperature measurement directly on the board with higher resolution sensor.

STATUS AND OUTLOOK

RFFE

While the noise performance of the SITF stripline RFFE already meets our goals for SLS, the new SLS-specific RFFE that we are currently developing aims for minimal long-term drift, where we will experimentally determine via lab and beam tests what long-term drift is obtained by the different employed suppression mechanisms (active temperature stabilization, pilot tone, crossbar). Beam pattern and bunch charge dependence of position and noise will also be measured, although the top-up injection and filling pattern feedback of the SLS relaxes the respective requirements for the electronics, thus leaving noise and drift as main optimization criteria.

ADC

For the ADC board, we are considering a redesign of the presently used 6-channel ADC for the SLS, since we need only four channels there and not six like for the E-XFEL cavity BPMs for which the ADC board was actually designed. Moreover, for the SLS the clock distribution can be simplified, since the ADC delay shifters are needed for E-XFEL but not for SLS. This may also reduce clock jitter, although the jitter of the present pre-series FEL ADC is already low enough for the SLS.

GPAC Hardware

While the present GPAC uses Xilinx Virtex-5 FPGAs, we are currently developing a new version based on Artix-7 / Kintex-7 FPGAs, mainly for cost and long-term maintenance reasons: these chips are significantly cheaper, need less power, and the availability of FPGAs and design tools is longer.

GPAC Firmware

So far we implemented all parts of the FPGA firmware necessary to perform efficient tests of the overall system, including the complete ADC signal processing chain (DDC, position calculation), ADC and position data storage in external RAM, and full VME-based control system access to measurement data, filter settings, etc. Features still to be implemented include the automatic gain control, as well as the interface to the global feedback network. EPICS-based GUIs for efficient control and readout of the BPM system for lab tests have been implemented. However, while BPM data analysis tasks like calculation of FFTs are presently done on high-level, the final system will perform these tasks on FPGA level.

CONCLUSION

The modular BPM electronics framework developed by PSI for the European XFEL and SwissFEL BPM systems will allow to upgrade of the SLS BPM system with significantly reduced development effort, by re-using or adapting already existing hardware and firmware modules. Although tests with the present SLS BPM prototype hardware are already very promising, the still high reliability of the present SLS system does not require to meet a specific deadline for the SLS upgrade, thus enabling us to do the necessary new developments of the new SLS systems in parallel to higher-priority FEL BPM developments (1st beam in SASE undulators expected end 2015 / 2016), with the goal to re-use the final FEL BPM hardware and firmware developments for the new SLS system and thus to minimize our long-term maintenance effort for hardware and firmware.

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