

SIGNAL EQUALIZER FOR SPS E-CLOUD/TMCI INSTABILITY FEEDBACK CONTROL SYSTEM*

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Abstract

The 4 GS/sec Ecloud/TMCI instability control system in development for the CERN SPS requires 1.5 GHz of processing bandwidth for the beam pickups and signal digitizer. An exponentially tapered stripline pickup has sufficient bandwidth, but has a phase response that distorts the beam signal in the time domain. We report on results from the design and implementation of an equalizer for the front end signal processing with correction for the pickup and cable responses. Using a model of the transfer functions for the pickups and the cabling, we determine a desired frequency response for the equalizer. Design for the circuitry and component value fitting is discussed as well as board construction and reduction of parasitic impedances. Finally, we show results from the measurement of an assembled equalizer, and compare them with simulations.

DEFINITION OF THE PROBLEM

Electron clouds and transverse mode coupling induce intra-bunch instabilities for high intensity beams in circular accelerators [1]. A feedback instability control system is in development to sample the vertical displacement of the bunch at 4 GS/sec such that the transverse head-tail modes can be detected and the necessary correction signal applied [2].

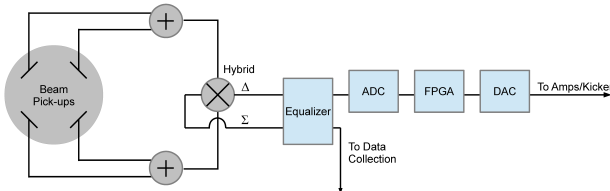


Figure 1: Instability control system diagram.

In order to measure the higher order transverse modes we need a pick-up with a bandwidth of up to 1.5 GHz. Exponentially tapered stripline couplers have sufficient bandwidth and flat frequency response at high frequencies, however, the phase response of the pick-ups distorts the beam signal [3]. Also, the long cables between the beam tunnel and signal processing introduce further distortion of the beam signal. The combination of these responses results in the deviation from the Gaussian as seen in Figure 2, and equalization is needed to recover original signal. An accurate time domain picture of the bunch is critical because

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this information will be used to apply a specific correction signal centered on the bunch.

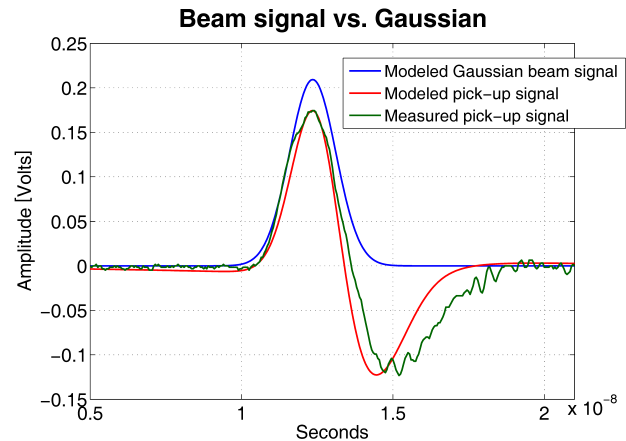


Figure 2: The beam shape is expected to be close to Gaussian, however the pick-up and cabling cause distortion in the time domain. Shown above is the modeled pick-up signal (red) and a measured signal (green).

The responses of the pick-up and cabling have been modeled and measured for the system at the SPS [4]. The transfer function of the pickup is modeled as

$$H_p(s) = \frac{s}{s + \frac{c}{2L}} * (1 - e^{-(a + \frac{-2Ls}{c})})$$

where L is the pick-up length and equals 0.375 m, a is the coefficient that describes the exponential taper and equals 2.48, and c is the speed of light. This is plotted in Figure 3.

The cable transfer function is represented by

$$H_c(s) = e^{\frac{1}{2}(-a_0(1+j)0.707\sqrt{\frac{s}{\pi}} - a_1\frac{s}{2\pi})}$$

The coefficients a_0 and a_1 are the measured cable coefficients. For the current cables $a_0 = 1.05 \times 10^{-4}$ and $a_1 = 3.5 \times 10^{-10}$. The transfer function magnitude and phase are plotted in Figure 4.

The equalization can be done with either software or hardware. A digital signal processing approach is attractive because any desired transfer function can be used and it can be changed easily, however, for our system this approach becomes too computationally intensive. For a software implementation the processing cost increases by n^2 whereas with a hardware equalizer circuit it is possible to do n channel parallel processing. Also, the cabling and pick-ups are unlikely to change often. For these reasons, an analog equalizer circuit has been designed.

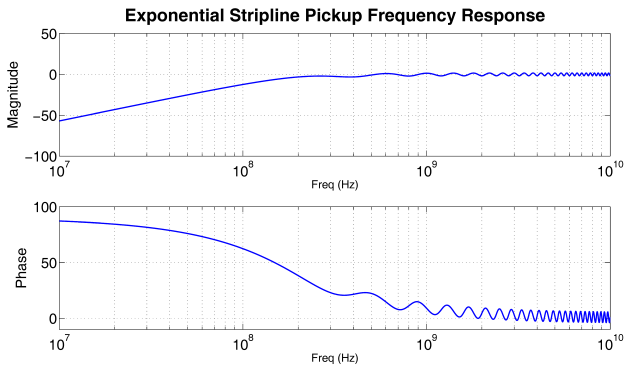


Figure 3: Model of exponentially tapered stripline pickup shows a frequency response similar to a differentiator.

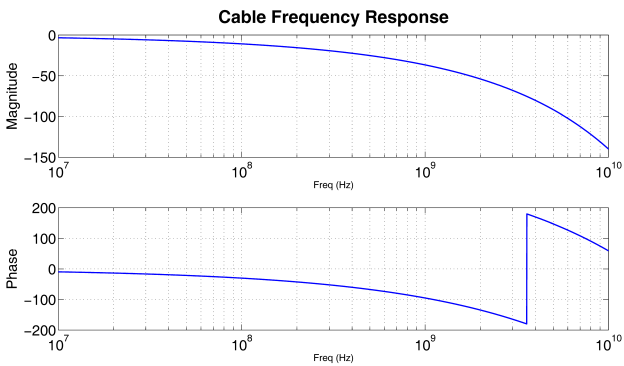


Figure 4: Model of cable between beam pipe and control room shows a frequency response similar to a low pass filter.

DETERMINATION OF IDEAL EQUALIZER

The ideal equalizer would have a frequency domain behavior equal to the inverse of the transfer function of the pick-up and cable. The current system, which monitors the beam position without feedback, uses this inverse transfer function in an offline software equalization. In designing an analog implementation, we first fit a polynomial to the ideal equalizer transfer function which suggests a circuit topology. System functions of linear, lumped, finite networks are real rational functions and can be represented as the ratio of two real polynomials, where the z_m are the zeros and the p_n are the poles of $G(s)$ [5].

$$G(s) = H * \frac{(s-z_1)(s-z_2)\dots(s-z_m)}{(s-p_1)(s-p_2)\dots(s-p_n)}$$

A polynomial fit with one pole and two zeros fits well up to 500 MHz, and suggests an easy implementation with a simple passive low pass filter. If it is determined that greater than 500 MHz is necessary, a more complicated circuit can be designed.

INITIAL CIRCUIT TOPOLOGY AND OPTIMIZATION

A low pass filter can be implemented with a variety of passive components. A distributed element solution is often used for high frequency filters, however it is impractical for our bandwidth due to the large areas needed for each element. Instead, we use a lumped element implementation with surface mount components to try to minimize unwanted parasitic elements. Various low pass filters were modeled and fit using a simple optimization algorithm.

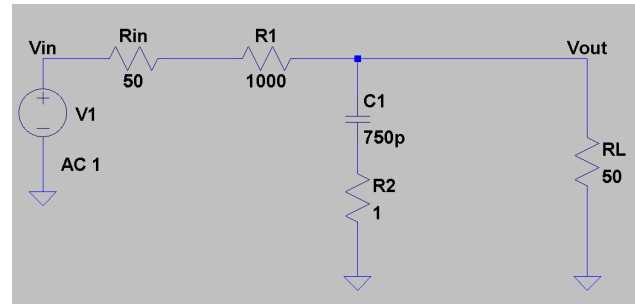


Figure 5: Simple low pass topology capacitor implementation, with frequency response results shown in Figure 6.

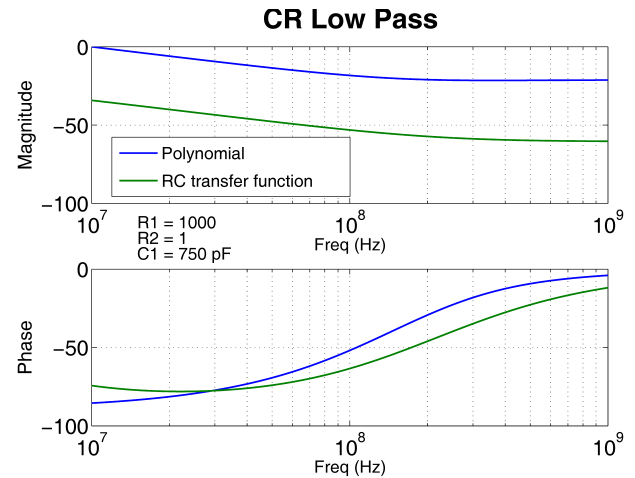


Figure 6: Frequency domain fit results for simple low pass topology as shown in Figure 5.

Our initial circuits had problems with parasitic components causing resonances within the desired bandwidth. Each circuit element can be modeled as a resistor, capacitor and inductor, the values of which can be measured and included in the model (see Figure 7).

Figure 8 shows the results from including these parasitics elements in the modeling step. The original circuit without parasitics included fits the ideal polynomial fit well, however, when actually building the circuit there was resonance at 100 MHz. Then, by adding the parasitics into the model before optimizing the component values the fit is again good and resonances are not found in the desired bandwidth.

Additionally, added to the optimization code was the option to put multiple resistors or capacitors in parallel,

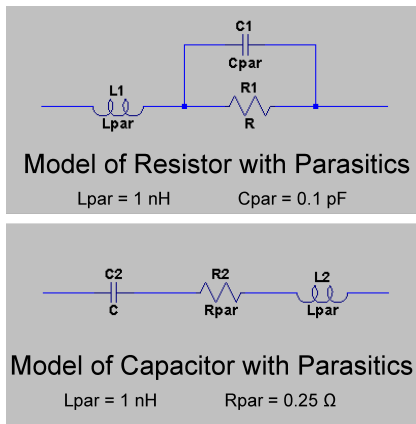


Figure 7: Models used for resistors (top) and capacitors (bottom) with parasitic impedances included.

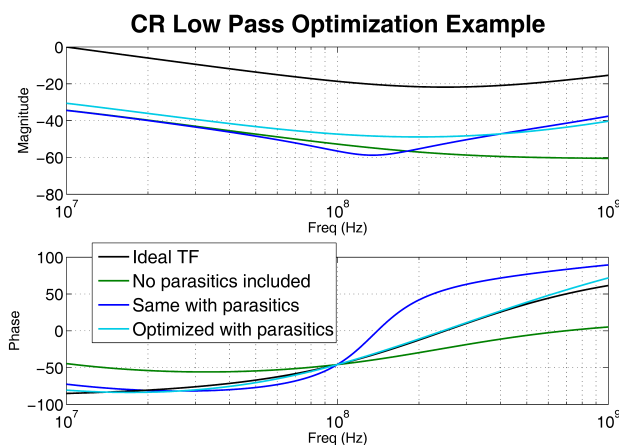


Figure 8: Component optimization with and without parasitics included in the model.

thereby reducing the overall parasitic impedances. Finally, we used a matching T network at the output in order to work into a higher load resistance, which helps in getting realistic component values. Using the optimization code and mocking up a variety of solutions led to a topology that achieved a good fit of the polynomial.

CONSTRUCTED CIRCUIT RESULTS

The circuit design was chosen to balance the requirements of a good fit and low loss of signal. Amplifiers with low noise figure were chosen to recover the magnitude lost in the equalizer. The frequency domain results can be seen in Figure 11.

To test the equalizer a measured pick-up signal was discretized, played out through the system 4GS/sec DAC, run through the equalizer and measured with an oscilloscope as shown in the top and bottom panels of Figure 12. To detect the higher order modes the system must have a bandwidth of 1.5 GHz, but for a first implementation, a bandwidth of 500 MHz will be able to measure the beam offset and the lower order modes.

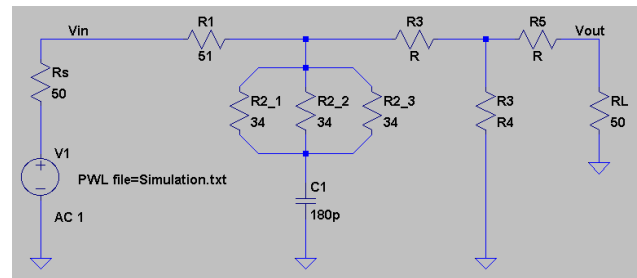


Figure 9: Circuit Design with component values chosen by optimization algorithm and three resistors in parallel to reduce the effect of parasitic inductance.

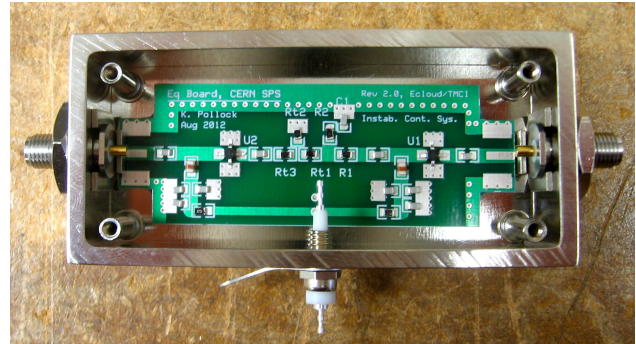


Figure 10: Constructed circuit with one amplifier on either end of the circuit. Input is on the left, output on the right, and DC biasing for the amplifiers at the bottom. Circuit components are 0805 surface mount.

CONCLUSIONS

A hardware equalizer has been designed, constructed and tested for use on the front end of a feedback instability control system, replacing the current software implementation and allowing the system to operate in feedback mode. In designing an analog equalizer we found that the parasitic elements associated with lumped element circuits made circuit design difficult, and proceeded by including the parasitic elements in the modeling. The resulting equalizer cir-

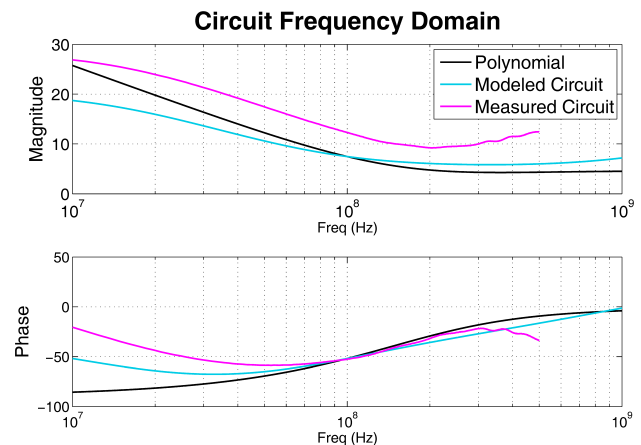


Figure 11: Frequency Domain Measured Circuit Results. The modeled and measured magnitudes have amplification included.

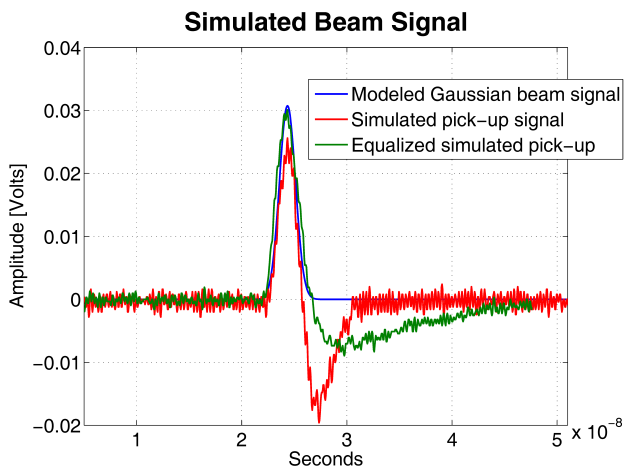


Figure 12: Pick-up signal discretized and played out through a 4GS/sec DAC (red), and then through equalizer (green).

cuit has a low pass topology and has a transfer function that fits well to 500 MHz.

Next we will need to determine whether a higher bandwidth equalizer is needed to resolve higher order modes within the bunch. The same methods developed for this initial equalizer can be used to design higher bandwidth equalizers, or equalizers with a different frequency response for new front end pick-ups or cabling. Finally, the same procedure could be used to create a pre-equalizer for the back end of the system. The kicker has a low pass frequency response with a cut off at 200 MHz, so a high pass equalizer could be designed to correct the time domain signal seen by the bunch.

This initial version of the equalizer will be tested at CERN on the SPS in the fall of 2012.

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