RADIATION DAMAGE IN DETECTORS AND ELECTRONICS

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Abstract

Coping with radiation-related effects is a constant challenge to the detectors and electronics deployed at high intensity and luminosity accelerators. Work associated with the LHC R&D collaborations has extended the range of understanding of these effects to unprecedented integrated dose levels. At the same time the availability of deep submicron technology and a variety of process variations available in IC production have redefined the tools available to build electronics to accommodate irradiation. This paper will briefly review our current understanding of the mechanisms of radiation damage and techniques to extend the lifetimes of detectors and electronics.

RADIATION EFFECTS IN SILICON AND SIO₂

I will concentrate here on the standard electronic materials – silicon and its oxide. We can divide the world of radiation damage into electromagnetic and bulk damage components. Ionizing radiation, such as x-rays, gammas, and electrons, create free charge in materials, which affects properties and performance. Hadrons (neutrons, pions, protons) can also produce "bulk" damage – damage to the silicon crystal lattice by displacing atoms from their usual sites. Electronics, because of the thin sensitive layer, tend to be most sensitive to ionization and the associated accumulation of charge in the material. Detectors are sensitive to both, with the most important damage often coming from bulk effects.

BULK DAMAGE – EFFECTS ON DETECTORS

Particle Physics detectors are unusual structures in the microelectronics world. They are fabricated with lightly doped, float zone, silicon, they use rather thick structures to collect a large signal, and they have a regular array of electrodes.

Displacement Damage in Silicon

Hadrons can interact and cause significant damage to the silicon crystal lattice. The amount and type of damage depends on the particle type and energy. The damage is usually quantified by the amount of Non-Ionizing Energy Loss (NIEL – KeV cm^2/g) or displacement damage (MeV-mb). For convenience damage is usually scaled to the NIEL of 1 MeV neutrons. However the pattern of energy loss depends on the type of particle and the pattern of damage clusters left by the particle.

Atoms scattered by inceident hadrons leave both vacated lattice sites (vacancies) and "free" atoms (interstitials) known as Frenkel pairs. The pattern of energy deposit is important – low energy transfers will leave sparse "point defects." Higher energy transfers can leave clusters of defects. Frenkel pairs in these clusters have a higher probability for recombination. The defects can have energies inside the bandgap, and act as additional donors or acceptors with energy levels different than the usual dopants. They can also act as generation centers for leakage currents. Other defects can act as traps for charge carriers and affect the charge collection efficiency of detectors. Vacancies and interstitials can also interact with the impurities in the silicon, and either be activated or passivated. Finally, they can recombine to anneal away some of the initial bulk damage.
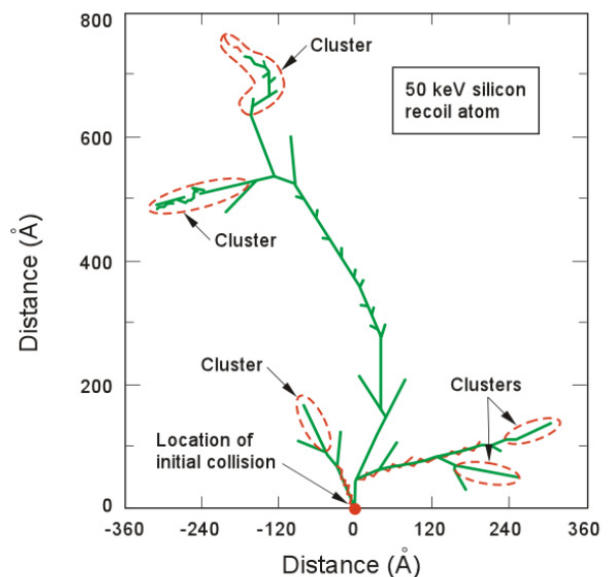

Figure 1. Simulation of damage caused by a 50 KeV silicon recoil nucleus [1].

The simplest effect, caused most efficiently by midgap states, is an increase in overall leakage current. This is a almost universal effect, and does not seem to depend on the details of doping, impurities, or processing. It is parameterized by:

$$I_{det} = I_0 + \alpha \times flux \times Vol$$
$$\alpha = 2 - 3 \times 10^{17} A/cm^2 \tag{1}$$

There is a strong annealing effect in leakage current (Figure 2). The overall annealing time has several

components [3] but is independent of sensor doping or impurity concentration.

Charge traps are also generated by non-ionizing radiation. This effectively lowers the mean free path of the generated electrons and holes, resulting in a loss of signal charge as the integrated dose increases. A dose of 2.5×10^{14} cm^{-2} charged hadrons reduces the total charge collected by 20% in 280 micron-thick test diodes [2].
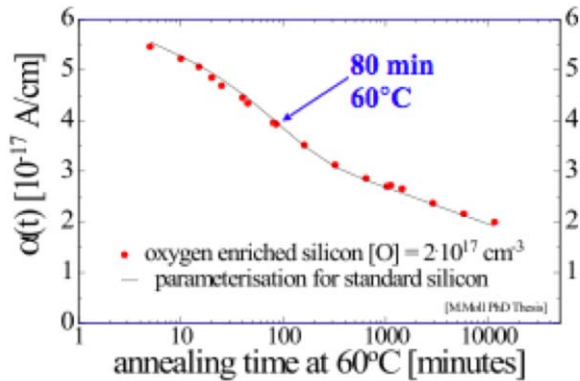

Figure 2. Damage constant as a function of annealing time at 60 deg C for standard (solid line) and oxygen enriched silicon [3].

The most significant effect for the lifetimes of LHC and Tevatron detectors is due to detector becoming more p-type as they are irradiated, due both to donor removal and acceptor creation. This is a complex process, which has been extensively studied by RD50. The most striking aspect is the "reverse annealing" that occurs when the detectors are exposed to temperatures above ~0 deg C. Defect complexes are generated by radiation which are not active at temperatures below ~-10. However, if the detectors are exposed to higher temperatures, these latent defect centers can be activated and contribute additional acceptors. The process has been characterized by [3]:

$$N_{eff}(\Phi) = N_{d0}e^{-c\Phi} + g_c\Phi + g_s\Phi e^{-t/\tau(t)} + N_Y(\Phi,t,T)$$

where the first term describes removal of donors, the second creation of acceptors, the third term describes "beneficial" annealing, and the fourth so-called "reverse" annealing. The reverse annealing term forces detectors exposed to high radiation doses to be kept cold to keep the effective p-type doping concentration low and maintain reasonable operating voltages. The parameterization is described in detail in reference [3]. Phi is the 1 MeV neutron equivalent flux. Silicon with a higher concentration of oxygen has been found to be less susceptible to reverse annealing for pion but not neutron exposure.

Detectors can be engineered to be more radiation hard by:

- Operating single-sided devices to eliminate capacitors, which need to stand off the bias potential, which increases as the devices become more p-type.
- Using oxygenated detectors.
- Design of implants and metallization to reduce internal fields and increase breakdown voltage.
- Utilizing thinned detectors, since depletion voltage is proportional to thickness squared. A subset of this technology comprises the "3D" sensors, which use deep holes etched into the silicon to reduce the effective distance between electrodes while keeping charge collection of a full thickness detector [4].

The most operating experience for heavily irradiated silicon detectors comes from the Tevatron, which has had large detector assemblies operating since 2002. Figure 3 shows the status of the operating voltage of the D0 silicon tracker as of May 2008.
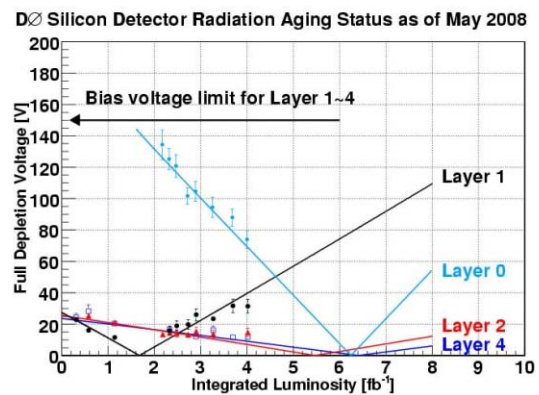

Figure 3. Depletion voltage as a function of integrated luminosity for several layers of the D0 silicon detector. Layer 0 is at ~1.6 cm, layer 1 at 2.5 cm and layer 4 at 9.6 cm. Points were measured during special runs where charge collection was measured as a function of bias voltage. Lines are fits to the model described in the text.

IONIZATION DAMAGE – EFFECTS ON ELECTRONICS

Although electronics are also affected by bulk damage to their crystal structure, modern electronics typically depend on highly doped structures near the surface of the silicon. This means that transistors, particularly CMOS, are sensitive to fields generated by charges induced in the silicon and SiO$_2$ structures by ionizing radiation.

Bipolar Transistors

Bipolar transistors depend on minority carrier diffusion from the emitter to the collector through a thin base. In this case the primary effect is bulk damage to the crystal structure. Traps are generated by displacement damage to the crystal structure. These can trap the charge diffusing from the emitter to the collector, effectively reducing the

transistor gain. The gain reduction depends on device geometry, type, switching frequency, temperature and current. For example, high currents through the base can saturate traps and increase the gain of irradiated bipolar transistors operating at high current [5].

CMOS

Modern high density electronics is based on the interaction of silicon and its oxide. The fact that precisely controlled thin SiO_2 insulating layers can be grown or deposited allows for fabrication of well-understood devices with extremely small feature size and excellent reliability. Radiation can affect the characteristics of the oxide, especially at the silicon-oxide interface, where there can be a high density of trapping states [6].

Figure 4 shows a typical MOS transistor with the current in an n or p channel controlled by a metal or polysilicon gate above a thin insulating silicon oxide layer. Ionizing radiation creates electron-hole pairs in the oxide. The electrons are relatively mobile and are collected by either the gate or channel fairly rapidly. Holes typically move more slowly, hopping from site to site until they reach the silicon-oxide interface. Here many of the holes are trapped by defects near the Si-SiO_2 interface. These trapped holes (Figure 5) generate a fixed positive charge, which can affect the characteristics of the transistor, generating shifts in the operating threshold of the device.
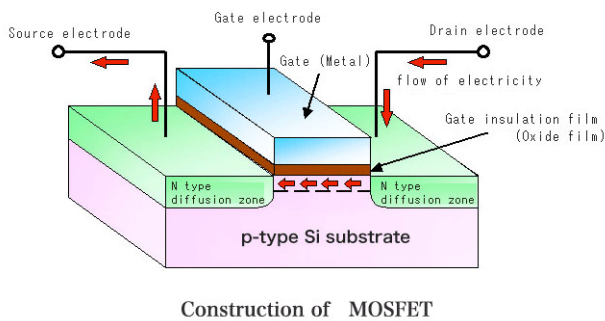

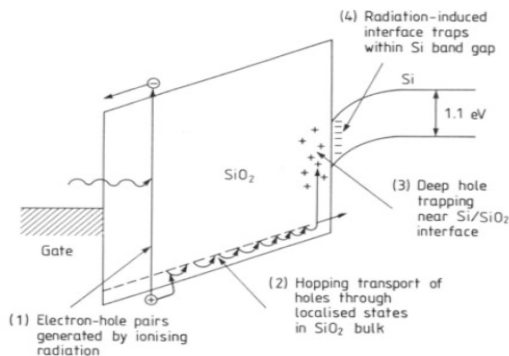Figure 4. Schematic of a MOS transistor.

Figure 5. Energy band schematic of the motion of electrons and holes produced in a silicon gate oxide.

PMOS and NMOS have different damage characteristics, since holes in pmos are attracted to the gate rather than the channel. The art of radiation-hard design in the past primarily involved fabrication of high quality oxides, which low densities of interface states. Defects could also be passivated by additional dopants or treatment in a hydrogen-rich atmosphere [8].

Gate oxides used in modern deep submicron electronics are much thinner than the ~100 nm oxide layers used in the early 90's micron-scale feature size semiconductors. Typical oxides are now less than 10 nm thick. At that thickness electrons can tunnel through the potential barrier at the silicon-oxide interface and neutralize the trapped holes. These transistors are "naturally" radiation hard, because there is no longer a fixed gate oxide charge to generate transistor threshold shifts (Figure 6).
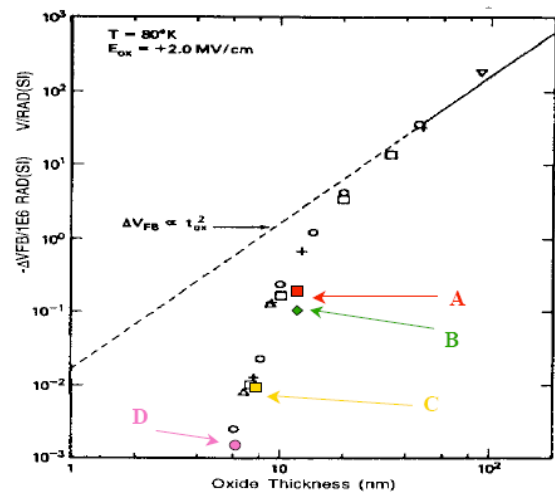
After N.S. Sacks, M.G. Ancona, and J.A. Modolo, IEEE Trans.Nucl.Sci., Vol.NS-31 (1984) 1249

Figure 6. Flatband voltage shift per megarad as a function of gate oxide thickness as predicted by Sacks et. al. [8].

However, the thin gate oxide is usually surrounded by a thicker field oxide. This field oxide will still trap charge and can provide a path for leakage current to flow from the source to the drain of the transistor. This effect can be avoided by altering the geometry of the transistor to a ringlike structure surrounded by a guard ring that does not provide a leakage path via the field oxide. This is usually called radiation hardness "by design" and is the basis for deep submicron electronics fabricated for readout of LHC detectors.

Single Event Effects

In addition to effects related to the total dose, local ionization caused by single particles can also affect electronics [9]. Charge deposition is usually characterized by the Linear Energy Transfer (LET), the energy loss per unit length of the ionizing radiation typically expressed in units of $MeV \cdot cm^2/mg$ of material.

Single event effects are characterized as:

- Single event upset (SEU). The change of state of a transistor due to radiation. This is usually reversible.
- Single event latchup (SEL). Latched change of state of a circuit due to radiation. May need to power cycle to reset.
- Single event burnout (SEB). Destruction of a circuit element due to radiation.

Modern three-dimensional device simulation programs allow designers to simulate the effects of ion impact on individual transistors (Figure 7).
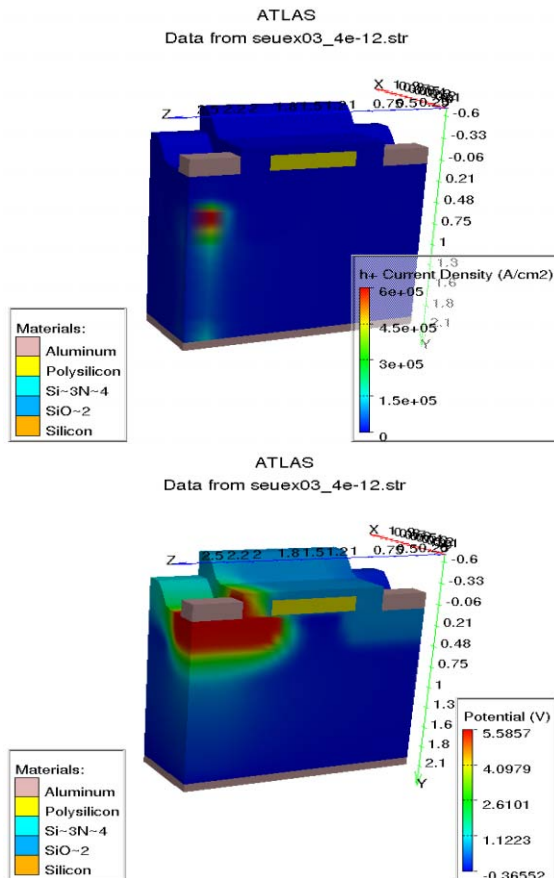

Figure 7. Simulation of the hole current density (top) and potential distribution (bottom) resulting from an ion impact on a typical MOS transistor structrure.

As transistor feature size goes down, less charge is needed to cause this state change, and single event effects become increasingly worrisome. Dynamic memory, which relies on the charge stored on a MOS capacitor is especially sensitive to SEU.

In CMOS, parasitic transistors can be formed in the implant/bulk/well regions. This can form a parasitic thyristor, which, if turned on by charge deposited in the bulk, can cause burnup if not current limited. The effects can by limited by:

- Use of thin, high resistivity epitaxial layers, which can limit parasitic currents.

- Trench isolation, which physically separates transistors.
- Silicon-on-Insulator (SOI) technology, which separates the device silicon from the bulk by a thin layer of oxide, reducing the area available for charge deposition.

Silicon-on-insulator is a particularly interesting technology [9]. SOI wafers are typically formed using a wafer bonding technology which can provide a structure with ~20nm thick device silicon on a 200-400 nm "buried" oxide bonded to a thick "handle" wafer. This structure isolates transistor from the bulk and lowers parasitic capacitance, allowing for faster response. However the buried oxide is still sensitive to trapped charge, which can act as a second gate, again affecting transistor characteristics [10, 11].

CONCLUSIONS

Increases in both understanding and technology have increased the range of total dose radiation hardness of silicon-based detectors and electronics by two orders of magnitude in the past two decades. Radiation damage Efforts by groups such as RD48 and RD50 [12-15] have revolutionized the understanding of bulk effects. Mitigation techniques based on detector design and high voltage operation allow for ~5-10 Mrad total dose exposures in the current generation of LHC detectors. New technologies, including thinned detectors, 3D electrodes, and devices with engineered defects promise further increase in the total dose tolerance. New parts must be carefully testing in a radiation environment that simulates the final environment [16].

Basic causes and effects in electronics have been carefully studied. However modern electronics constitute a moving target. The rapid advance of technology, with smaller feature sizes, thinner oxides, and innovative structures continue provide a new set of problems and opportunities.

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