PERFORMANCE OF FPGA-BASED DATA ACQUISITION FOR THE APS BROADBAND BEAM POSITION MONITOR SYSTEM*

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Abstract

The Advanced Photon Source (APS) monopulse beam position monitor (BPM) system, designed to measure single- and multi-turn beam positions, is one of three BPM systems currently in use to measure and control both AC and DC orbit motions. Recently, one sector of the monopulse BPM system was upgraded by replacing its 1992-era 12-bit signal conditioning and digitizing unit (SCDU) with a field-programmable gate array (FPGA)-based system for signal processing. The system consists of a repackaging of the broadband rf receiver modules together with a VME Extensions for Instrumentation (VXI) form factor housing eight 14-bit digitizers and one FGPA. The system will be described in detail, including an overview of its new functionality, and performance will be discussed. Of particular interest is the noise floor, which will be contrasted with the previous system and with other systems in use at the APS.

INTRODUCTION

The Advanced Photon Source broadband monopulse BPM system is designed to measure single- and multi-turn beam position used in a feedback system to control both AC and DC orbit motion. Presently, a VXI-based signal conditioning and digitizing unit (SCDU) is used for data acquisition. A monopulse rf receiver, located inside the SCDU, receives 10-MHz band-limited sum and difference signals from an in-tunnel filter-comparator and outputs beam intensity and normalized position [1]. Both signals are digitized via 12-bit analog-to-digital converters (ADCs), operating at the 271-kHz ring revolution frequency, and values are stored in registers. The Memory Scanner module, residing in the same VXI crate, reads the output registers and provides a programmable boxcar average. It also provides a high-speed fiber-optic port to stream data to the feedback system. The system has been in operation for more than ten years. Compared to today's technology, the SCDU is dated, and needs a technology upgrade. The planned upgrade was to remove the monopulse receiver from the SCDU for reuse, and replace the SCDU with an FPGA-based VXI data acquisition and processing module [2]. The new BPM Signal Processor (BSP100) contains eight ADCs, an embedded IOC, and a single Altera Stratix® II FPGA. It can acquire and process data for four monopulse receiver units. This paper describes the new system's functionalities and test results.

SYSTEM OVERVIEW

The new monopulse BPM system (shown in Figure 1) consists of five subcomponents:

- In-tunnel hardware (capacitive button pickups, matching networks, filter comparator, Heliax® cables)
- Receiver chassis
- Power supply chassis
- Fan unit
- BPM signal processor (BSP100)

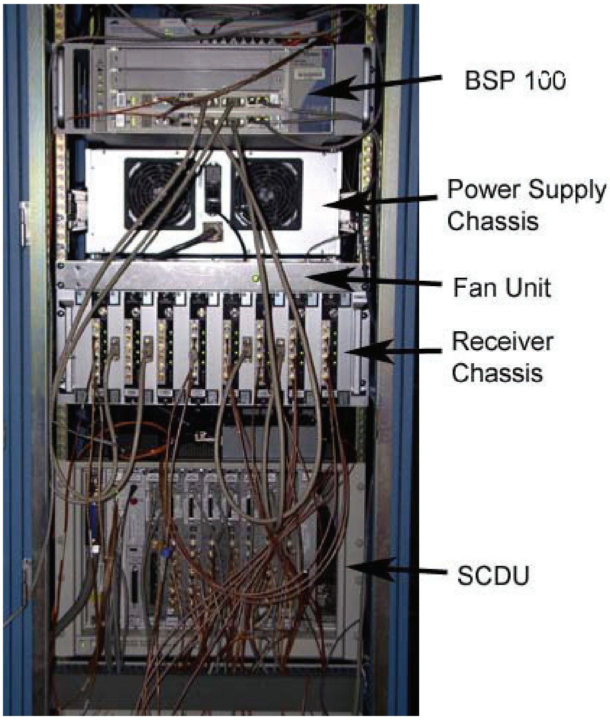

Figure 1: New monopulse BPM system installed at Sector 38.

The in-tunnel portion of the new monopulse BPM system, including capacitive button pickups, matching networks [3], filter comparator, and Heliax® cables, remains unchanged.

The monopulse receiver was removed from the SCDU and packaged together with an interface circuit board, mounted on a custom-designed heat-sink aluminum block, that can be plugged into a receiver chassis. The interface circuit board not only provides regulated power and filtering and I/O signal conditioning to the monopulse receiver, but also is capable of generating a 21-dBm,

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*Work supported by U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DE-AC02-06CH11357.

351.94-MHz self-test rf signal that can be used to diagnose rf front end in-tunnel hardware.

The receiver and power supply chassis have a standard 4U height by 19” wide form factor and provide electromagnetic interference (EMI) shielding of 50 dBm at the fundamental frequency of 351.94 MHz. Mounted inside the receiver chassis is a custom-built backplane, which provides power and interconnections for up to eight receiver modules to interface with two BSP100 modules.

The power supply chassis consists of four linear power supplies providing all of the required voltages to the receiver chassis via a shielded multi-conductor cable. This chassis was designed such that it can be installed either in front or on the back of the cabinet. This allows the new system to be installed with a minimum amount of disturbance at the location where space might be tight due to other installed equipment.

A variable fan unit mounted above the receiver chassis provides cooling for the receiver modules. The fan speed is controlled by temperature sensors.

The BSP100 is the heart of the new monopulse BPM system. It is a stand alone Experimental Physics and Industrial Control System (EPICS) input/output controller (IOC); an FPGA-based, C-sized VXI form factor, consisting of eight high-speed 14-bit digitizers (Analog Device AD6645) running at 88 MSPS (one fourth of the APS rf frequency); an embedded IOC; and a Stratix® II FPGA. Although the BSP100 is a VXI form factor, the backplane connections are for power only.

The FPGA major functional blocks are:

- An APS timing system receiver
- An acquisition control block
- A preliminary processing block
- A continuous processing block
- A triggered processing block

APS Timing System Receiver Block

The APS timing system receiver block provides timing synchronization of the embedded IOC and generates triggered signals for single-turn acquisition, digital oscilloscope, turn history, and slow beam history used by the triggered-processing block.

Acquisition Control Block

The BPM data acquisition is controlled by setting the appropriate bit in the acquisition control RAM [4]. Configuration control bits are:

- Plane switch bit: selects the monopulse receiver X or Y channel.
- Commutation switch bit: commutates between 0 and 180 degrees on the sum channel for offset compensation.
- Use this sample bit: selects a sample for further processing.
- Save this sample bit: selects sample for use with the oscilloscope mode.
- Self-test gate: controls the monopulse receiver self-test oscillator.
- Wrap marker bit: marks the end of the acquisition RAM contents.
- Turn marker bit: indicates the beginning of a new turn.

The control RAM can be configured to provide sample-by-sample control for 324 samples per turn, for up to 12 storage ring turns. Acquired samples are forwarded to the appropriate blocks for processing.

Preliminary Processing Block

The preliminary processing block (shown in Figure 2) reads the ADC values in the horizontal (x) or vertical (y) planes specified in the control RAM, computes a turn-by-turn average, and sends it to several other blocks for processing. Setting the “Save this sample” bit in the acquisition control RAM allows oscilloscope acquisition of all ADC values for about 12.6 turns, a single sample per turn for 4096 turns, or any combination in between.

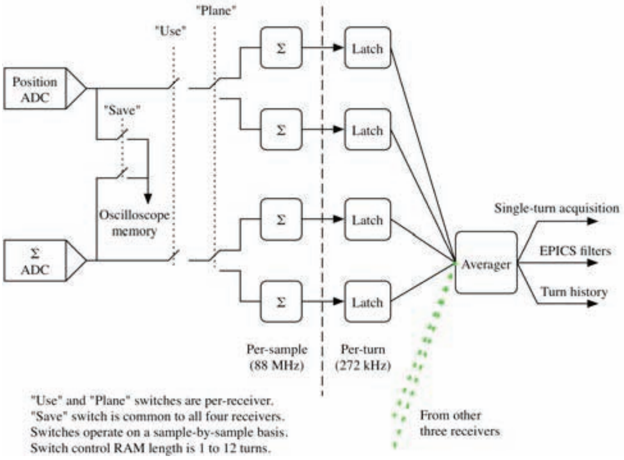

Figure 2: Preliminary Signal Processing.

Continuous Processing Block

The continuous processing block (shown in Figure 3) performs signal processing at a fixed rate. The sum and position signals for each plane are passed through a chain of low-pass decimating filters that result in three sets of process variables (PVs), labeled ms, msAve, and mswAve for historical reasons. The ms and msAve PVs have 10-Hz and 1-Hz signal bandwidth, respectively, and are updated at 10-Hz, whereas mswAve has additional averaging, with signal bandwidth, of 0.1 Hz, updated at 1 Hz. The noise power for sum and position signals for 1-Hz to 200-Hz and 1-Hz to 5-KHz bandwidths is also calculated in this block. Signal noise power is calculated by using the ‘root-mean-square’ (rms) technique. The averaged turn-by-turn values, from the preliminary processing block, are first bandpass filtered, squared, and then low-pass filtered to simulate the ‘mean’ operation. Finally the square-root is taken to obtain the rms values.

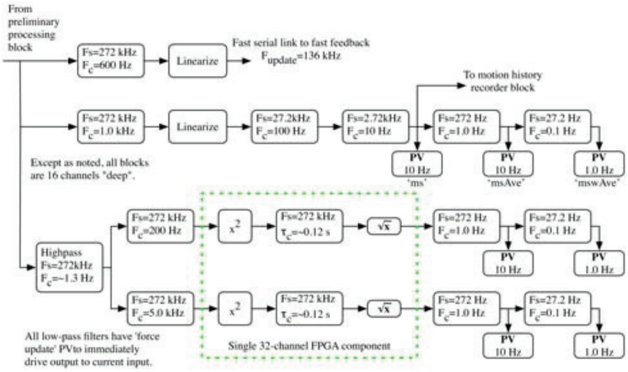

Figure 3: Continuous Signal Processing Block.

Triggered Processing Block

The triggered processing block provides data acquisition used for machine studies and postmortem analysis. Data is acquired and processed on an intermittent basis via a number of waveform recorders. Data acquisition is as follow:

1. An EPICS PV provides a signal to 'arm' the waveform recorder.
2. Upon being armed, it acquires data and stores it in a ring buffer.
3. After the specified number of pre-trigger samples have been acquired, it begins to look for a trigger condition.
4. When a trigger signal is detected, it continues acquiring and storing samples until the specified number of samples is reached, after which the recorder ceases acquisition and interrupts the EPICS IOC.
5. The EPICS generic transient recorder in the IOC reads the samples and makes them available as waveform records.

Oscilloscope Waveform Recorder

The oscilloscope waveform recorder records the raw signals from the ADC at the full sampling rate of 88 MHz. The buffers are 4096 samples deep with an equal number of pre- and post-trigger samples. The trigger signal is the logical OR of three sources; each can be individually inhibited. The sources are:

1. An EPICS PV aligned to the wrap condition from the acquisition control memory
2. An event programmed in the event receiver block
3. An external logic level

Turn-History Waveform Recorder

The turn-history waveform recorder records the turn-by-turn average sum and position values provided by the preliminary processing block at the turn rate of 272 kHz. The buffers are 262,144 samples deep. The trigger signal is the logical OR of four sources, each can be individually inhibited. The sources are:

1. An EPICS PV
2. An external logic
3. An event programmed in the event receiver block
4. A turn-average of a selected sum channel dropping below a specified threshold

The turn history tracks the average of predetermined 88-MHz samples collected during the preceding turn.

Slow Beam History Waveform Recorder

The slow beam history waveforms exist primarily for beam loss postmortem analysis The slow beam history waveforms are acquired and stored in the IOC generic transient recorder. Data samples are taken from the 2.72-kHz filter at a 100-Hz rate. The buffers are 2048 sample deep. The trigger signal is a logical OR of two sources, each of which can be individually inhibited. The sources are:

1. An EPICS PV
2. An event programmed in the event receiver block

Single-Turn Acquisition

The single-turn sum and position averaged values from the preliminary processing block are latched whenever a trigger signal is received. The trigger signal is normally derived from an injection trigger event. This allows information from the first through sixteenth turn to be acquired and will be used for injection optimization studies.

TEST RESULTS

Turn-History Waveform Recorder

Shown in Figures 4 and 5 are portions of the spectrum of horizontal beam motion during normal 24-bunch stored-beam operation. Here an EPICS soft trigger was used to trigger acquisition of a 262,144 (= 2^{18}) sample waveform. With each sample collected every 3.68 microseconds, the record length corresponds to 0.965 seconds. As a result, the FFT of the data has resolution down to 1.04 Hz and up to 135.8 kHz Nyquist, eliminating most aliasing problems.

Figure 4 shows the FFT spectral amplitude up to 5 kHz, while Fig. 5 shows the rms beam motion (square root of the integral of the power spectral density) in microns rms for the same data set.

These data were collected at a BPM location where the horizontal beta function is 3.8 meters. The largest contributions are from sources below 200 Hz, with prominent 60-, 120-, and 360-Hz components. Multiples of 360 Hz are also evident at 1440 and 1800 Hz. The 1.8-kHz line is amplified due to its proximity to the synchrotron tune, which is the broad peak extending from 1.8 to 2.1 kHz. It is likely that the 1.8 kHz is associated with the rf system high voltage power supplies, which induce small amounts of amplitude or phase modulation on the beam.

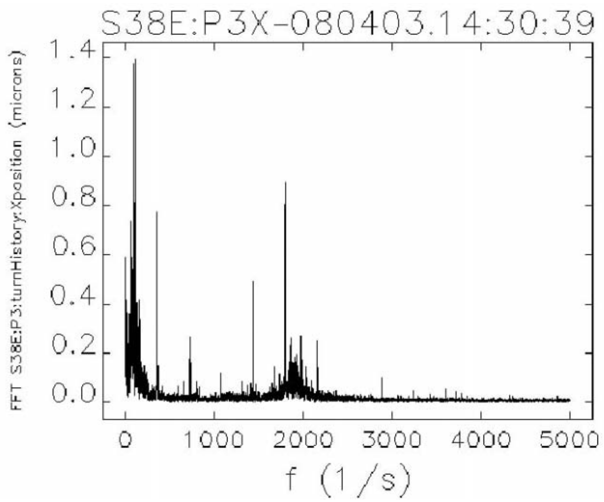

Figure 4: Frequency spectrum of horizontal beam motion during normal 24-bunch operation.

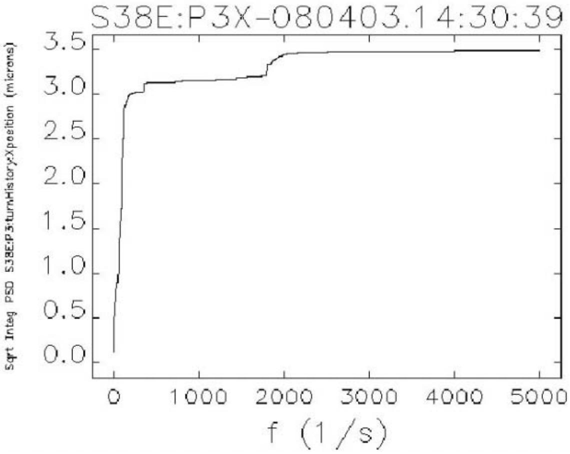

Figure 5: Integrated PSD of horizontal beam motion during normal 24-bunch operation.

An injection transient using the 2-Hz injection trigger derived from the EPICS event system was captured and is shown in Figures 6, 7, and 8 on vastly different time scales. In this case there were 24 bunches stored in the machine: however, the FPGA was configured to provide the average position of only the bunch being injected into. Six 88-MHz samples per turn for this bunch were averaged on a turn-by-turn basis vs. 6 * 24 = 144 samples per turn for Figures 4 and 5. In Fig. 6, data are shown for a full half second before and after the event.

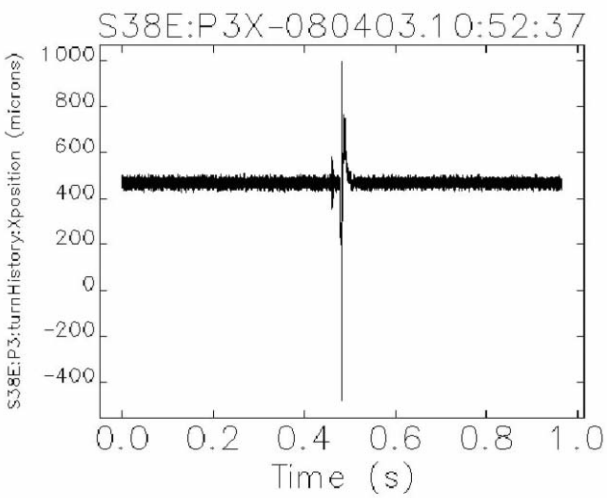

Figure 6: Beam motion during an injection transient captured with the turn history waveform recorder.

Figure 7 shows 80 milliseconds straddling the injection event. The slowest feature, resembling a sine wave starting just before 0.48 seconds, results from leakage fields from the injection thick septum magnet. The sharp spike occurring just after 0.48 seconds and shown in more detail in Fig. 8, is a residual 30-kHz betatron oscillation caused by the fast injection kickers. The small tone bursts near 0.46 seconds are of unknown origin, but also have a strong 30-kHz component and may be associated with the fast kicker power supplies.

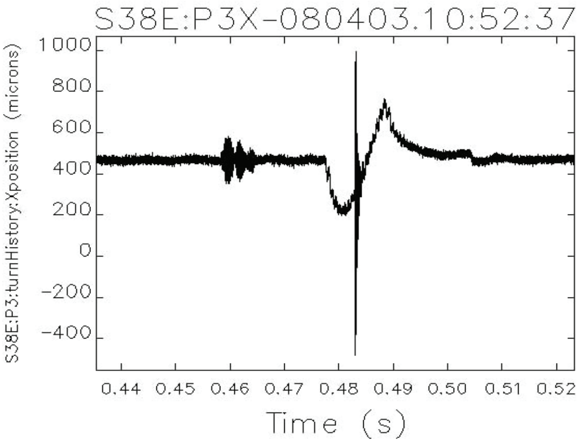

Figure 7: Beam motion during an injection transient (zoomed in).

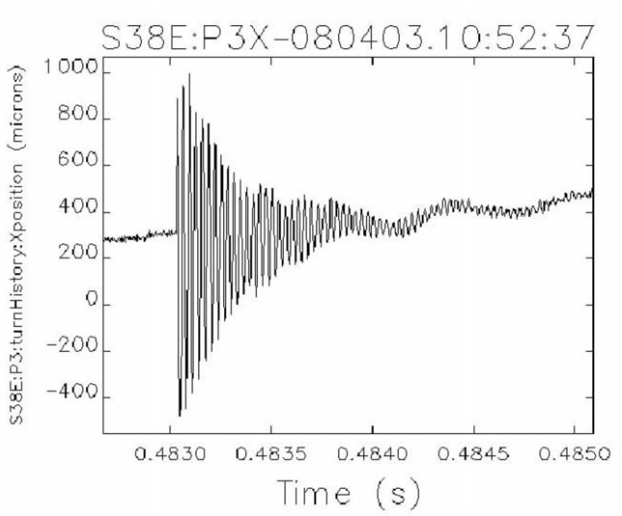

Figure 8: Residual 30k-Hz betatron oscillation.

Slow Beam History Waveform Recorder

Figure 9 shows the same injection transient event captured by using the slow beam history waveform recorder. As before, a 2-Hz injection signal was used to acquire 2048 samples at a 100-Hz sampling rate to obtain a waveform length of 20.48 seconds.

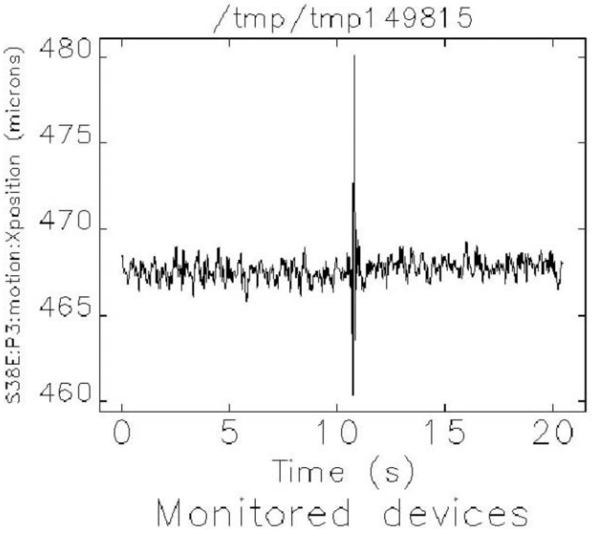

Figure 9: Beam motion during an injection transient captured with the slow beam history waveform recorder.

CONCLUSION

From the above results, one can clearly see the ability of the new monopulse BPM system to observe small beam motions over a large range of time scales. Coupled with the ability to trigger on injection, on beam dump, or on demand, it provides a set of very powerful diagnostics to support machine operation and accelerator physics.

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