STRIPLINE BEAM POSITION MONITORS FOR LCLS*

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Abstract

The Linac Coherent Light Source (LCLS) must deliver a high quality electron beam to an undulator for production of coherent X-ray radiation. High resolution beam position monitoring is required to accomplish this task. Critical specifications are a dynamic range of 0.08-8.0 nC with 5 micron resolution at 200 pC in a stripline pickup of 1 inch diameter. Processor electronics were designed, based on band-pass filtering the signals followed by direct digitization of the resulting pulse train. The processor consists of Analog Front-End (AFE) and Analog-to-Digital Converter (ADC) boards, packed into 19-in rack mount chassis, 1U high. The AFE board has a very low input noise, approximately 3 micro V rms in a 7 MHz bandwidth centered at either of two frequencies, 140 or 200 MHz, depending on the length of the stripline BPM used. The maximum gain is 34 dB with programmable attenuation of up to 46 dB in 1 dB steps. An on-board pulser sends a short calibration tone burst to the striplines to perform calibration between beam pulses. The ADC board has four 16-bit digitizers with a sampling frequency of 120 MHz. For the LCLS injector 22 prototypes of the processors were built and installed in 2007. Measured resolution at 200 pC is typically 3-5 microns. A production run of 53 improved processors are currently being installed and commissioned.

OVERVIEW

A beam position monitor consists of four stripline electrodes connected with low loss cables to a BPM Processor (Fig. 1). The BPM processor chassis consists of the Analog Front-End, ADC, and clock boards in a 19" rack-mounted chassis. A processor on the ADC board talks with the VME IOC (Input-Output Controller). The digitizer and the data acquisition system are described in references [1] and [2].

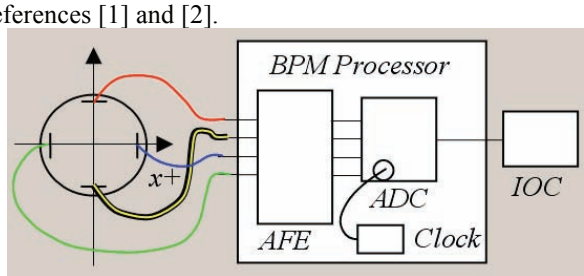

Figure 1: BPM system block diagram.

Twenty-two prototypes and 16 new production chassis are distributed along the Linac injector. Forty-three new BPM Processor chassis will be installed on LCLS this summer.

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Requirements

There are two critical requirements – dynamic range and resolution at 200 pC beam charge.

Table 1: Requirements for the LCLS BPM system

Parameter	Value	Comments
Dynamic Range	0.08 – 8 nC	40 dB
Resolution @ 0.2 nC	5 μm	
Stability	5 μm per hour	

ANALOG FRONTEND

Modern technology provides a variety of high dynamic-range, low noise RF amplifiers and low insertion loss filters applicable for the precision analog front-end design. Three RF amplifiers and three band-pass filters provide low noise amplification with gain programmable by two digital attenuators per channel, providing a total dynamic range control of 46 dB (Fig. 2).

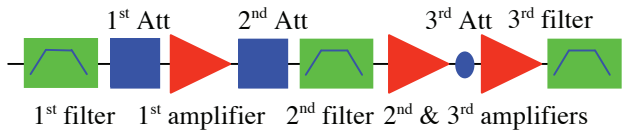

Figure 2: One channel of the Analog Front-End

Two rather different lengths of stripline pickups are used in LCLS: the typical linac BPM strips are 10 cm long, while the striplines intended to provide higher resolution for the linac-to-undulator section have 50 cm long striplines. Due to the difference in frequency response of the two type of striplines we construct BPM processors at two different frequencies, 140 MHz and 200 MHz. Bandpass filters define a bandwidth of 7 MHz at the operating frequency, either 140 MHz or 200 MHz.

Taking the component parameters from Table 2 we calculate an input-referred noise of 3 microvolts rms.

Table 2: Insertion loss (IL), Noise Figure (NF), Gain, IP3.

	IL, dB	NF, dB	Gain, dB	IP3, dBm
1st filter	2.5			
1st att	0.5			
1st amplifier		2.8	20.4	39
2nd att	0.5			
2nd filter	5			
2nd amplifier		3.3	14.9	40
3rd att	6			
3rd amplifier		3.3	14.9	40
other	1.4			

The output noise power density is measured at -134.5 dBm/Hz or 42 nV/√Hz or 110 μV rms in a 7 MHz bandwidth (see Fig. 3). The channel gain is 34 dB so the input noise is about 2.2 μV rms, close to the calculated 3 μV rms.

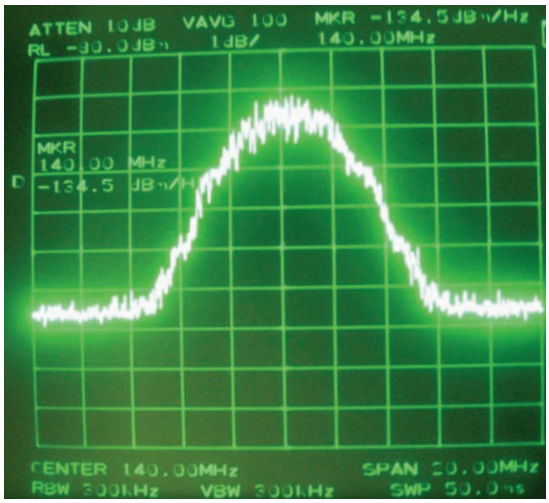

Figure 3: Analog Front-End noise spectrum. Vertical and horizontal scales are 1 dB/div and 2 MHz/div respectively.

Online Calibration

The BPM processor continuously self-calibrates between beam pulses. The AFE transmits short (~260 ns) tone-bursts at the processor frequency alternately on one of the striplines on each of the BPM axes (typically the Y^+ and the X^- striplines). The ratio of amplitudes of the signals detected on the two adjacent striplines calibrates the gain ratio of these processor channels and their associated cables. The calibration tone drive amplifier can put out as much as 2 Watts, adjustable via programmable attenuator down to 2 mW.

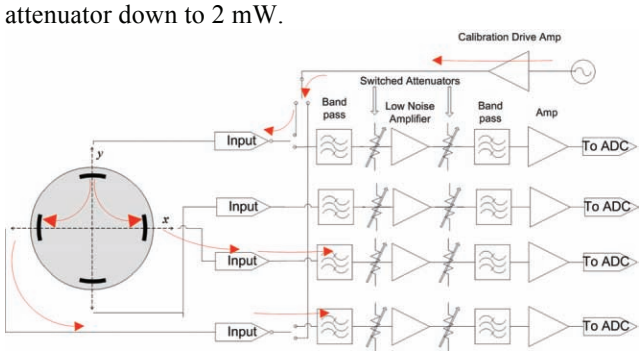

Figure 4: Calibration scheme block diagram.

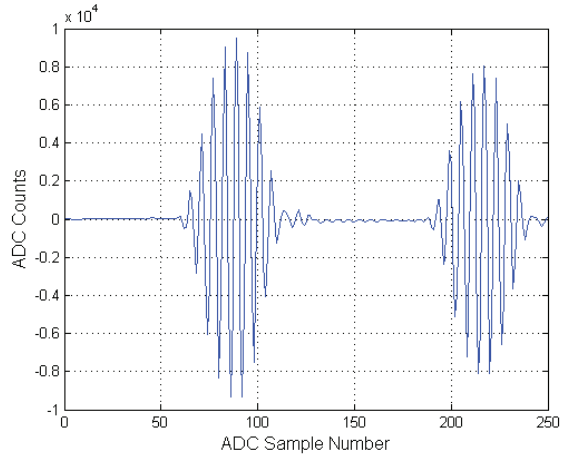

Figure 5: Calibrator tone burst detected by left and right striplines.

Output Limiter

An unwelcome feature that comes with high dynamic range amplifiers, used in the signal channels to achieve high linearity, is that the potential output power levels can overdrive the ADC inputs to damage. The AFE board therefore contains fast comparators at its channel outputs that shut down the outputs as an overvoltage is approached. The limited bandwidth of the signal channel allows a reasonably fast comparator to prevent transient overvoltages.

Control

A Xilinx FPGA controls programmable attenuators, generates the timing sequences for the calibrator and limiter, and communicates with the processor on the ADC board via a QSPI (queued serial peripheral interface) link.

ADC BOARD

The digitizer board is the Phase and Amplitude Detector[1] (PAD) board developed for LCLS low-level RF control carrying four Linear Technology Corp. LTC2208 16-bit ADCs capable of sampling at 130 MHz. We expect close to 12.4 effective bits on a 140 MHz signal according to specifications. The ADCs are clocked at 120 MHz. Since the input signal frequency is higher than the sampling frequency, the ADC under-samples the data, aliasing the 140 MHz signal to 20 MHz, while the 200 MHz signal are aliased to 40 MHz.

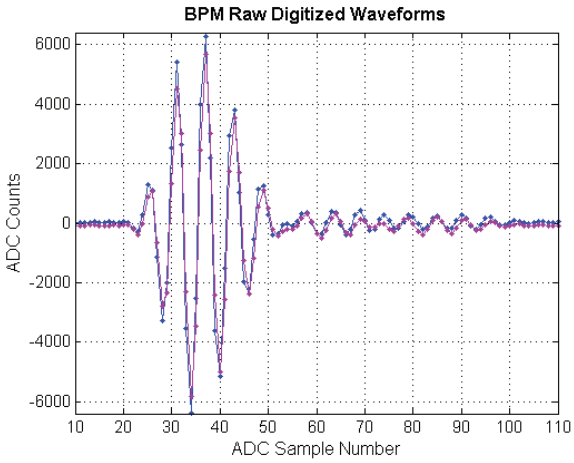

Figure 6: Beam signal digitized at 120 MHz.

A processor on the PAD board acquires BPM waveform data from the ADCs and transmits it over a dedicated network link to a local BPM IOC. A separate network links the PAD processor to the accelerator network for configuration and control.[2]

RESOLUTION

We evaluate BPM resolution in the presence of beam jitter which is much larger than the resolution by acquiring position synchronously over a large number of beam pulses from many BPMs. Then we use a least-squares linear fit to the shot-by-shot beam position in each BPM as a linear function of the positions measured in all the others. Using 17 of the LCLS stripline BPMs in the linac over 120 consecutive beam pulses we find an average position resolution of 4.8 microns rms at a bunch charge of 220 pC. Figure 7 shows pulse-by-pulse measurement of beam position at one particular BPM, the X and Y positions measured there versus that predicted by the best-fit linear combination of 16 other BPMs, and the X and Y positions with the beam jitter predicted by the other BPMs subtracted. The scatter of the measured position after beam jitter subtraction is taken as an estimate of BPM resolution.

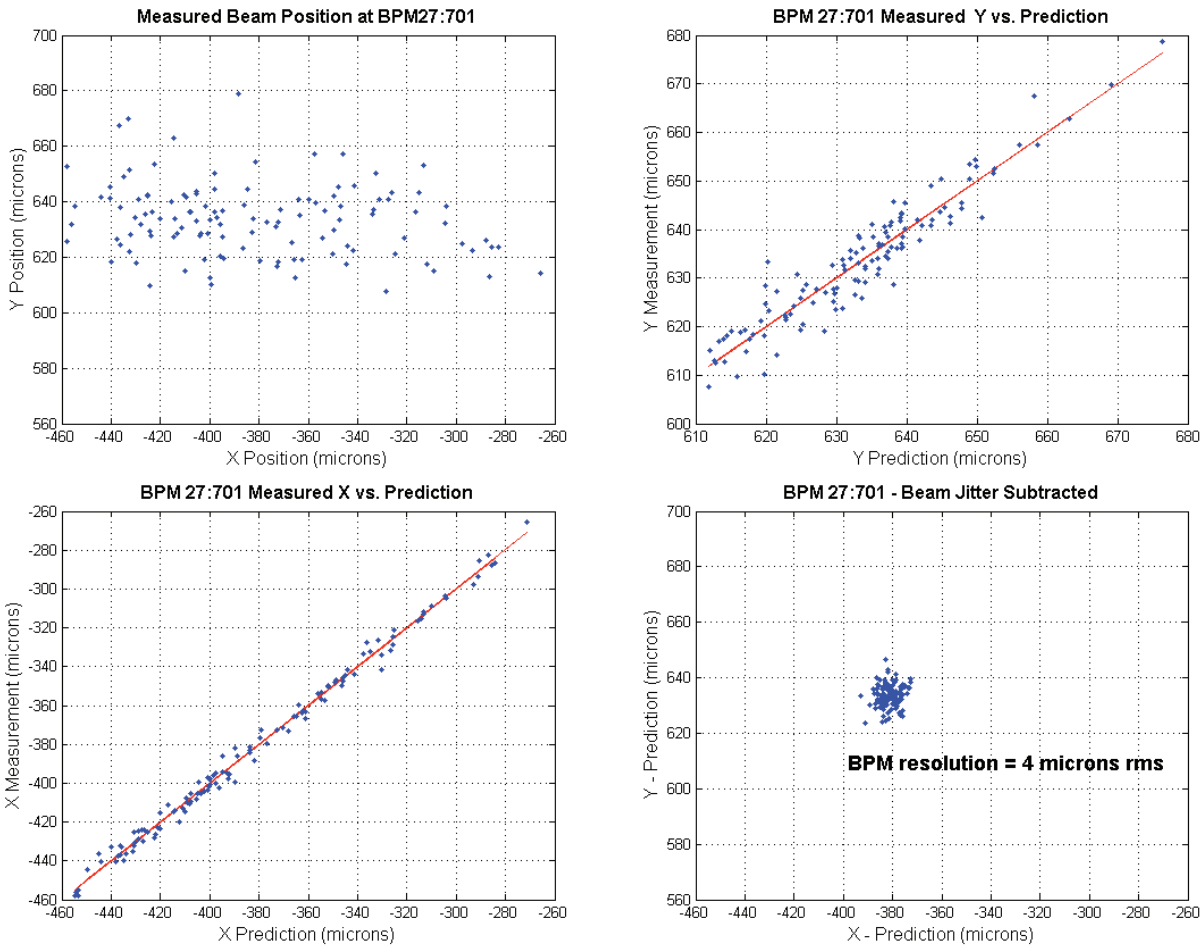

Figure 7: (a) X,Y position measured at BPM 27:701, (b) Measured Y versus Y predicted here from the other 16 BPMs, (c) Measured X versus X predicted here from the other BPMs, and (d) X ,Y with the beam jitter removed.

SUMMARY

Twenty-two prototype BPM processors were installed in the linac and commissioned in 2007. The prototypes design was revised, improved, and 53 production modules assembled and tested in February through April of 2008. The first 14 of these have been installed and commissioned with beam, demonstrating 5 micron rms resolution at 200 pC as required. The remaining BPMs will be installed this summer.

REFERENCES

[1] D. Kotturi, R. Akre, T. Straumann, "130-MHz, 16-Bit Four-Channel Digitizer", ICALEPCS'07, Knoxville, October 2007.

[2] T. Straumann, et al, "LCLS Beam-Position Monitor Data Acquisition System", ICALEPCS'07, Knoxville, October 2007.