NSLS-II RF BEAM POSITION MONITOR*

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Abstract

An internal R&D program has been undertaken at BNL to develop an RF BPM to meet all requirements of both the injection system and storage ring. The RF BPM architecture consists of an Analog Front-End (AFE) board and a Digital Front-End board (DFE) contained in a 1U 19" chassis. An external passive RF signal processor has been developed that will be located near the RF BPM pickups. The partitioning into two boards enables a flexible Software Defined Instrument. A model-based design flow has been adopted utilizing AWR VSS, Simulink, and Xilinx System Generator for algorithm development and AFE impairment performance analysis. The DFE architecture consists of a Virtex-5 with MicroBlaze embedded processor. An optional Intel Atom SBC is also supported. The AFE is based on a bandpass sampling architecture utilizing 16-bit ADCs. Long-term drift is corrected by inclusion of an out-of-band calibration tone. An RF BPM Calibration Tool is being developed for removal of systematic errors and performance verification. In this contribution we will present a detailed overview of the architecture, then compare simulation results to laboratory performance.

INTRODUCTION

An internal R&D program was started in August 2009 to develop an RF BPM for the 3GeV NSLS-II currently under construction at Brookhaven National Laboratory for the Injection System and Storage Ring. Since the start of the BPM R&D program was after the Critical Decision 3 award, the development timeline is aggressive. The development schedule mandates a proof-of-principle demonstrated August 2010.

As a state-of-the-art 3rd generation light source designed to deliver world-leading intensity and brightness, beam stability will be of utmost importance. The most stringent BPM stability requirement [1] is for the multi-bunch stored beam condition where vertical resolution, horizontal resolution, and long-term stability must be less than 200nm rms. It is well known that the most challenging requirement is the sub-micron long-term stability. The sub-micron horizontal, and vertical resolution correlate to the intrinsic signal-to-noise (SNR) of the pickup geometry [4] which can be met by proper analysis and design of the analog and digital processing.

The NSLS-II RF BPMs utilized in the Storage Ring are housed in thermally stabilized racks, regulated to +-0.1° C of the preset operational temperature. Based on tests of existing BPM technology in the NSLS-II thermally controlled racks it is possible to achieve sub-micron long-term gain drift without calibration. However, a dynamic calibration scheme has been incorporated to achieve long-term (i.e., 8 h) gain stability to meet the required 200 nm objective [4] over the operational range of 50-500 mA.

SYSTEM ARCHITECTURE

The NSLS-II RF BPM architecture consists of a passive RF Processor box located in the tunnel, the AFE, and DFE. Shown below in Figure 1 is the prototype BPM consisting of both AFE and DFE.

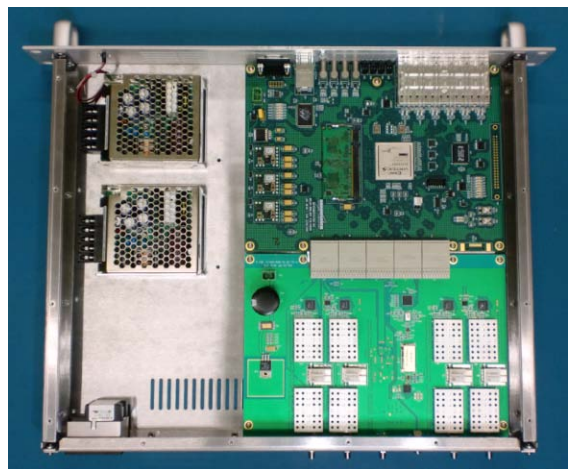

Figure 1: NSLS-II Prototype RF BPM.

The RF Processor box consists of a custom Diplexer designed by K&L Microwave, isolator, and 4-way power splitter. An illustration of the Passive RF Processor is illustrated below in Figure 2. The RF Processor is shown located on the girder directly below the BPM pickups. Four 1 m SiO_2 cables are connected from the pickup assembly to the RF Processor.

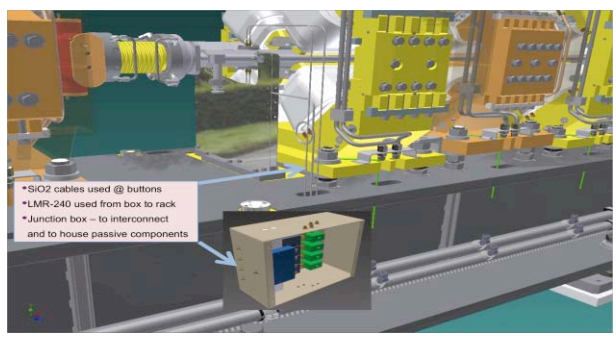

Figure 2: Passive RF Processor.

A detailed illustration of the RF Processor is illustrated below in Figure 3. One m of SiO_2 is used to connect the BPM pickup to the RF Processor. The RF Processor consists of an isolator and custom diplexer. The isolator presents a return loss of 18 dB over a 150 MHz

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bandwidth centred at the RF fundamental frequency of 500 MHz. The custom diplexer is used to combine an out-of-band calibration tone with the pickup signal. The prototype diplexer design consists of four independent diplexers used to process each channel. It is intended that the production design will incorporate all four diplexers into a single four channel monolithic design. The high band of the diplexer centred at 500 MHz consists of a 5th-order Bessel response. The low band of the diplexer passes a calibration tone over a 35MHz band centred at 465 MHz utilizing a Chebyshev response.

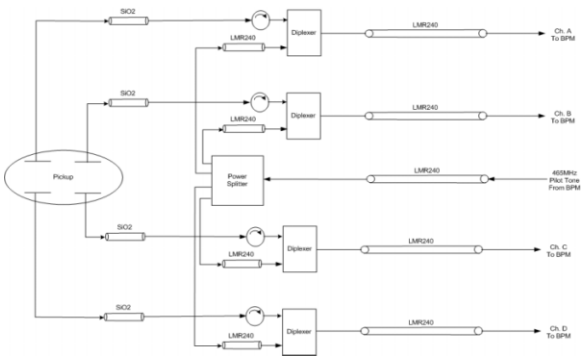

Figure 3: Tunnel Configuration - Passive RF Processing. RF Passive elements include Isolators, Diplexer, and 4-way Power Splitter.

An illustration of the prototype single-channel custom diplexer is shown below in Figure 4. A suspended microstrip topology is used to maximize Q while maintaining minimum insertion loss.

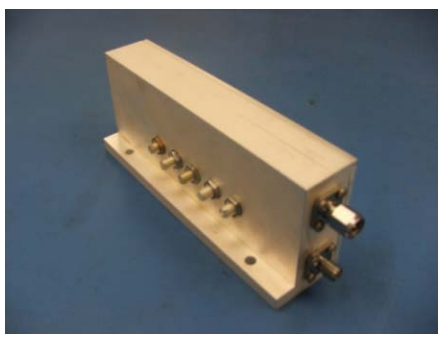

Figure 4: Prototype single-channel diplexer.

The measured 5th-order order Bessel response is shown below in Figure 5. The measured bandwidth is 8.5MHz, 3.8dB insertion loss, and maximum group delay of 83ns. The 5th -order diplexer high-band response was chosen to provide good pulse response characteristic which include minimal group delay distortion, linear in-band phase, and rapid decay of stored impulse energy measured in terms of "Time-Sidelobe" decay.

The Time-Sidelobe decay is illustrated below in Figure 6. The Bessel filter has a -40 dBc first Time-Sidelobe response compared to -10 dBc for the Chebyshev filter response. The composite output signal of the diplexer is transmitted to the RF BPM electronics via LMR200FR cable. Each RF BPM consists of an AFE and DFE that process four BPM channels. Slow Acquisition (i.e. 10Hz) and data on demand are transmitted to and EPICS IOC via Gigabit Ethernet. The Fast Orbit FeedBack (FOFB) is transmitted via a custom Serial Data Interface (SDI) link developed at BNL.

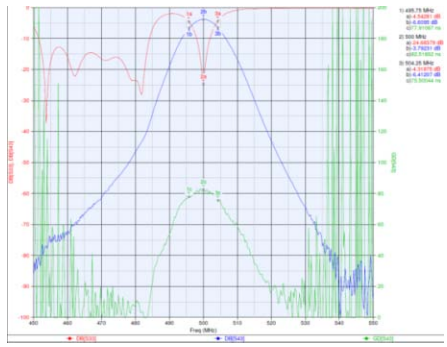

Figure 5. Measured Diplexer high-band response.

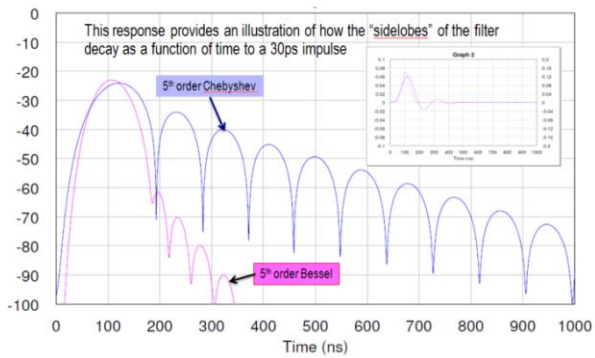

Figure 6: Diplexer high-band time-sidelobe response.

ANALOG FRONT END

The AFE employs a bandpass sampling architecture for the Storage Ring and Booster. The composite RF signal from the diplexer consisting of the BPM signal centred at 500MHz contained in a 8.5 MHz bandwidth along with a narrowband pilot tone approximately 25 MHz below the 500 MHz BPM signal are under-sampled at approximately 117 Msps by four independent 16-b ADCs. An alternate heterodyne architecture is currently under investigation to yield higher spatial resolution for the Injection system.

Careful consideration has been given to the design of the AFE to meet the long-term sub-micron gain drift requirement while achieving maximum dynamic range, and minimum distortion. Each of the four identical AFE receivers consists of two identical low-noise amplifiers, and two identical digital attenuators. Systematic gain variation is minimized by utilizing a minimal number of different components with each different component selected from the same die for each individual BPM. Each receiver also incorporates an inter-stage bandpass filter to minimize noise and distortion with sufficient bandwidth to pass the composite RF signal from the diplexer. A

drop-in compatible narrow band interstage bandpass filter is used for the injection system.

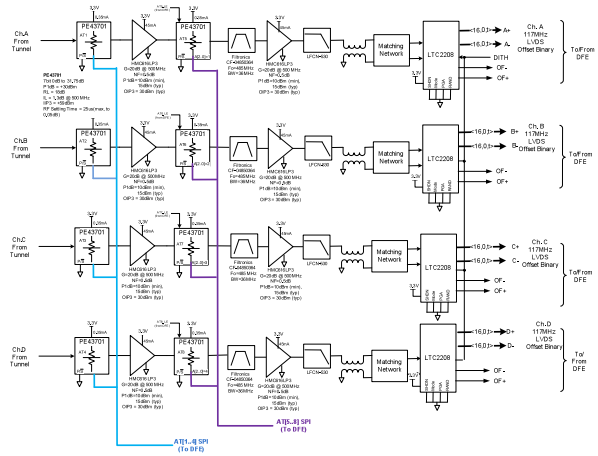

Figure 7: AFE functional block diagram.

The two Peregrine PE43701 Ultra CMOS digital attenuators provide 31dB of dynamic range with 0.25 dB resolution with an IIP3 of +59 dBm. The HMC616 amplifiers are tuned to operate over a band of 400-600 MHz, produce 20 dB of gain at 500 MHz, have an OIP3 of +37 dBm and a noise figure of 0.5 dB. The HMC616 amplifiers have a specified thermal gain dependence of 0.0003dB/0.1° C. Thermal gain dependence measurements of the HMC616 were conducted at BNL yielding a thermal gain dependence of 0.00016 dB/0.1° C, approximately a factor of four lower than the allotted gain variation to maintain 200 nm stability. The thermal gain stability of the HMC616 also revealed perfect thermal tracking at the maximum pilot tone offset frequency of 465 MHz, and the BPM signal frequency of 500MHz.

The AFE has been constructed using Rogers RO4350B RF laminate in conjunction with Rogers RO4450 bonding material. The AFE consists of 6 layers with an overall thickness of 0.93 inch. The AFE board thickness was chosen to match the DFE board thickness to ensure proper connection of the co-planer high speed inter-board connector.

AFE Simulation

An analysis of the AFE performance was first performed utilizing AWR VSS. The goal of the analysis was to design the RF BPM receiver to maximize dynamic range by simultaneous optimization of minimal noise figure, and maximum IP3 at the ADC input. Simulation results demonstrate an overall gain of approximately 22 dB, and a cascaded noise figure of 12 dB including cable losses. The simulated gain satisfies the theoretical gain required to translate the system noise floor to the lower limit of the ADC dynamic range in order to maximize the instantaneous SNR. Instantaneous dynamic range is more of an important factor for single-pass, and TbT processing since only minimal digital processing gain can be realized for these two conditions.

The simulated 1dB compression point of +14dBm ensures linear operation over the full-scale dynamic range of the ADC. The simulated IP3 at the ADC input is +36dBm. It is important to maximize the IP3 at the ADC input to simultaneously maximize immunity to intermodulation distortion at the ADC output.

AFE Laboratory Characterization

The entire RF BPM receiver was prototyped and characterized at BNL utilizing evaluation boards in conjunction with AFE layout development. The measured AFE performance is illustrated below in Figure 8.

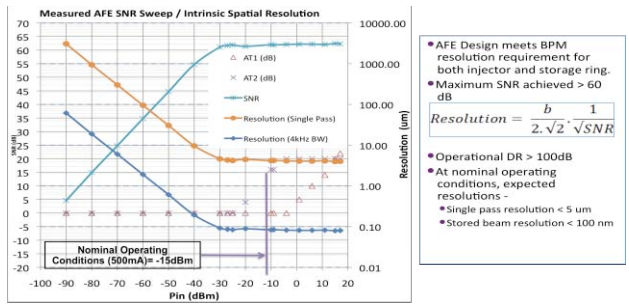

Figure 8: Measured AFE performance.

Data obtained by sweeping RF input using Agilent N5181A RF Signal Generator. The Rhode & Schwarz SMA100A RF Signal Generator was used to provide a 117MHz CW signal to the ADC with a measured RMS jitter of 72fs. Tests conducted with ADC clock synthesizer implemented on the AFE yielding a 312 fs RMS jitter resulted in negligible performance degradation.

The plot in Figure 8 illustrates the intrinsic RF BPM resolution for the case of instantaneous signal processing (e.g. no averaging, single-pass), and for the case of stored beam where an estimated 28 dB of processing gain will be realized. The measured AFE performance demonstrates >100 dB of dynamic range, 100 nm stored beam resolution, and 5um single-pass resolution over the operational dynamic range of 50-500 mA.

AFE Calibration

AFE calibration consists of two parts, a systematic gain normalization performed on each unit prior to installation, and a dynamic calibration utilizing an out-of-band continuous pilot tone inject at approximately -30 dBc at the ADC input. A preliminary assessment of the diplexer which combines the pilot tone and BPM signal exhibits a gain variation of approximately 1ppm/°C, yielding nearly an order of magnitude gain variation margin considering the 200 nm limit.

DIGITAL FRONT END

The digital half of the beam position monitor electronics is referred to as the Digital Front End (DFE) and is responsible for all digital signal processing of the button signals and communication of the results with the control system.

The DFE is shown below in Figure 9. It measures 9.5 by 7.5 inches and sits in the front half of the BPM chassis.

The main component of the DFE is a Xilinx Virtex-5 XCSX95T Field Programmable Gate Array (FPGA). The DFE will be iterated to incorporate a Virtex-6 for the production build. The FPGA handles the digital signal processing chain which will be discussed in the next section. The FPGA also instantiates a soft-core Microblaze processor, which is responsible for all communications with the control system and also coordinates all on-board functionality. Memory for the board is provided with a 256 Mbyte SO-DIMM DDR2 memory module.

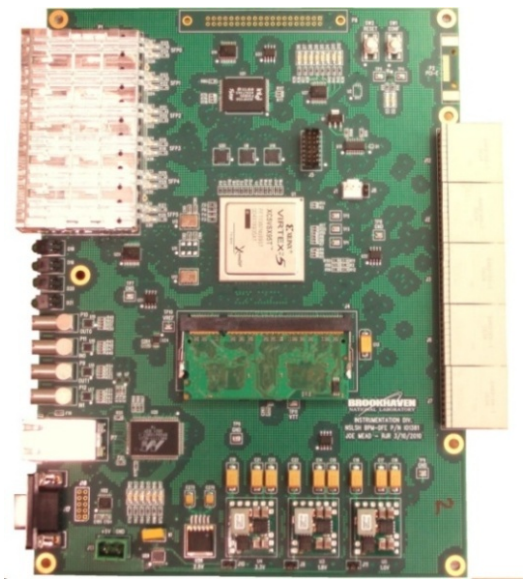

Figure 9: Digital Front End.

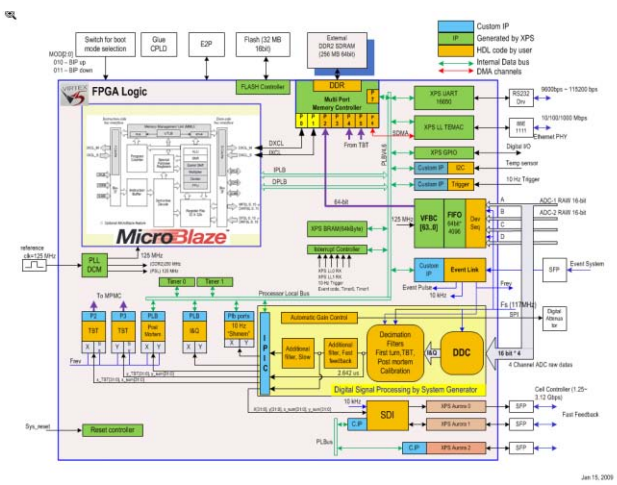

Figure 10: DFE architecture.

This memory provides the program memory space for the Microblaze as well as a large buffer for raw ADC data and turn-by-turn data. The total throughput of the memory is 4 GBytes/sec, which is enough to store continuous bursts of raw ADC data, turn-by-turn data, and provide program and data memory for the Microblaze.

For non-volatile memory the DFE has a single 256 Mbit FLASH memory. This FLASH memory stores the FPGA bitstream as well as the program data for the Microblaze. On power-up the FPGA configures itself from the FLASH memory. When the Microblaze comes out of reset it executes a small boot-loader program from internal memory. This boot-loader fetches the final program from FLASH and copies it to the DDR memory, from which it is executed.

Slow Acquisition and Control

For slow controls, communication with the control system is provided by a gigabit Ethernet interface. Using the Microblaze processor a TCP/IP stack is implemented for robust communication. This interface provides 10 Hz position data as well as on demand requests and configuration settings.

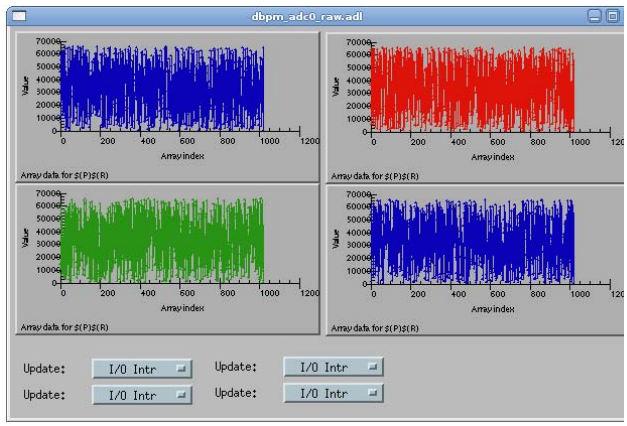

Figure 11: EPICS acquisition of raw ADC data via BPM SA port.

Fast Orbit Feedback

For other communications including fast-orbit feedback data the DFE provides 6 SFP modules, which supports data rates of up 3.2 Gbit/sec. For fast orbit feedback the data needs to be low latency and highly deterministic. This 10 khz updated data therefore bypasses the Microblaze and connects directly from the FPGA fabric to the high speed SERDES section of the FPGA. This data is transmitted to dedicated cell-controllers which can process the data and provide deterministic low-latency updates to the fast magnet power supplies.

AFE Interface

Finally, is the interface with the AFE, which is via five high speed differential Tyco Hm-Zd style connectors. All high speed connections are done via LVDS signalling levels. Four of the connectors are used for the four ADCs, which are 16 bit and run at 117 MHz. The fifth connector is used for configuration and status signals between the two boards.

Digital Signal Processing

The main signal processing element is the FPGA. It is here that all digital signal processing occurs. The FPGA that was chosen was the SX95T, which is rich in hard multipliers to allow for the complex filtering that is

needed. To implement the signal processing, the MATLAB/Simulink environment along with the Xilinx System Generator toolbox is used. This method allows for easy modeling and simulation of the system at a level higher then HDL code. The top level block diagram of the signal processing chain is shown below in Figure 12.

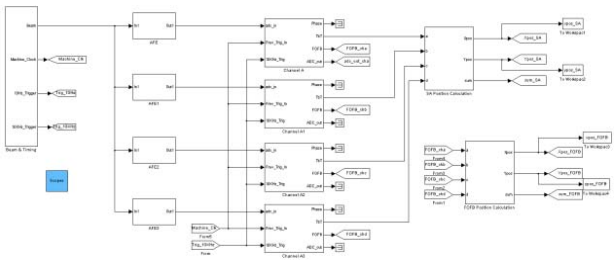

Figure 12: Simulink top-level system simulation model.

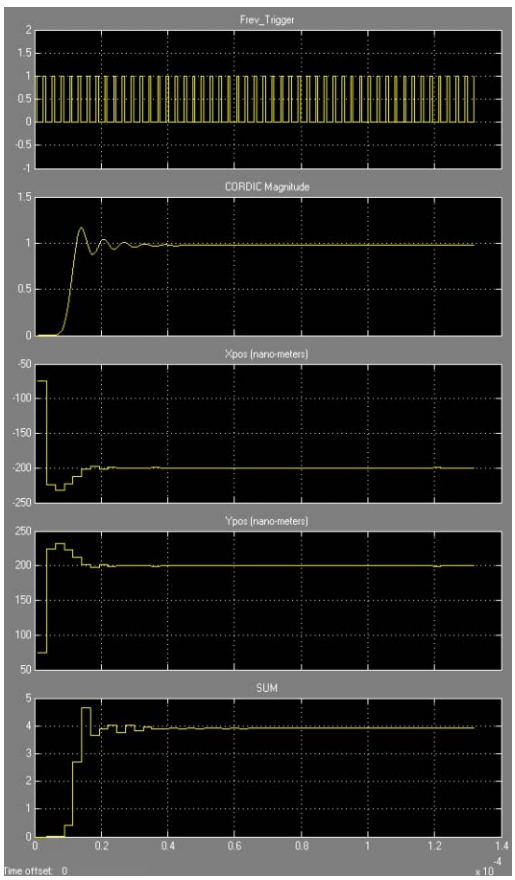

Figure 13: Slow Acquisition System impulse response.

RF BPM CALIBRATION TOOL

The RF BPM Calibration Tool is a Matlab-based program used to measure, and normalize the AFE systematic gains of the four channels prior to installation. Post calibration verification is also performed.

Systematic gain calibration will be performed in a laboratory setting on each BPM prior to installation using the "RF BPM Calibration Tool" (Figure 14). The Factory Calibration consists of a Rhode & Schwarz SMA 100A RF Signal Generator, general purpose computer running the calibration software, and the RF.

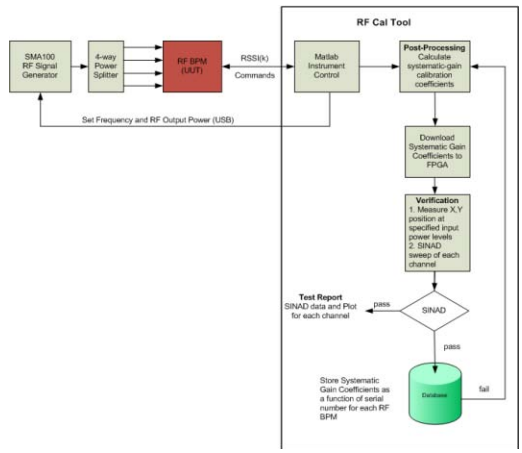

Figure 14: RF BPM calibration tool architecture.

STATUS

Two DFE units have been tested to be 100% functional. Six more DFE units have been received. Ten AFE boards have been received. Five AFE boards are currently being assembled for testing. Ten chassis have been fabricated. Five diplexers will be received in early May. System integration will commence at the end of April 2010. Performance measurements of the diplexer will be conducted on live beam in May. The first system objective is to quantify performance in terms of resolution and drift in the NSLS-II thermally stable racks in the late May-June timeframe. TbT and Single-Pass characterization will follow.

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