

THE LCLS UNDULATOR BEAM LOSS MONITOR READOUT SYSTEM*

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Abstract

The LCLS Undulator Beam Loss Monitor System is required to detect any loss radiation seen by the FEL undulators. The undulator segments consist of permanent magnets which are very sensitive to radiation damage. The operational goal is to keep demagnetization below 0.01% over the life of the LCLS. The BLM system is designed to help achieve this goal by detecting any loss radiation and indicating a fault condition if the radiation level exceeds a certain threshold. Upon reception of this fault signal, the LCLS Machine Protection System takes appropriate action by either halting or rate limiting the beam. The BLM detector consists of a PMT coupled to a Cherenkov radiator located near the upstream end of each undulator segment. There are 33 BLMs in the system, one per segment. The detectors are read out by a dedicated system that is integrated directly into the LCLS MPS. The BLM readout system provides monitoring of radiation levels, computation of integrated doses, detection of radiation excursions beyond set thresholds, fault reporting and control of BLM system functions. This paper describes the design, construction and operational performance of the BLM readout system.

INTRODUCTION

SLAC National Accelerator Laboratory's Linac Coherent Light Source (LCLS) is a Free Electron Laser which produces tuneable hard X-Rays in the 1.5 to 15 Angstrom range. The X-rays are produced by passing 4.6 to 13.6 GeV, 0.05 to 1.0 nC single bunches of electrons from the last third of the SLAC Linac through a newly constructed undulator line. The undulator line consists of 33, 3.42 meter long permanent magnet segments. Each segment contains 226 NdFeB magnets with vanadium permendur poles arranged with 30mm period [1]. These materials can be demagnetized by radiation induced by beam loss. The Beam Loss Monitor (BLM) system has been developed based on system requirements [2] to detect this loss before it reaches an appreciable level.

The BLM system was developed in collaboration with Argonne National Laboratory. ANL had the responsibility of developing the BLM detectors and detector signal conditioning electronics. SLAC had the responsibility for developing the readout electronics system, integration into the LCLS Machine Protection System, and system commissioning.

The system design requires 33 BLM detectors, one for each undulator segment. Due to initial budget limitations,

only five ANL BLM detectors and associated electronics were produced. As a interim solution, re-purposed PEP-II BLM detectors, available after the shutdown of the B-factory, were installed on the remaining 28 undulators plus some additional locations.

BEAM LOSS DETECTORS

The ANL BLM detectors consist of a fused silica Cherenkov radiator optically mated to a PMT [3]. The complex geometry of the radiator was chosen in order to cover the undulator magnets, while propagating the resultant output light to a single PMT. Signal conditioning, high voltage and a test signal are provided by a local BLM Interface Module (BLM-IM) on a per detector basis. The detectors are mounted at the upstream end of each undulator segment, with the companion BLM-IM mounted nearby on the undulator girder in the undulator hall tunnel. The BLM-IM contains an adjustable high-voltage power supply with a range of 0...-1KV, as well as a charge-sensitive preamp which converts the PMT charge pulse into a time-shaped ($\tau=50\mu\text{s}$) voltage signal with a maximum output voltage of -1.5V in 50 ohms. Additionally, the BLM-IM contains an LED pulse generator whose 600ns light signal is optically connected to the detector head. This allows the detector and electronics chain to be stimulated with a test pulse during non-beam time as a built-in self check.

The PEP-II detectors [4] are similar in their materials (quartz Cherenkov radiator mated to a PMT) but have a different geometry: cylindrical radiator mounted in a cylindrical housing. The housing contains a lead shield to attenuate the storage ring synchrotron radiation and enhance beam-loss showers, and also the dynode resistive divider chain. The PEP-II detectors are mounted near the original locations of the ANL units, but a 10cm away due to their incompatible geometry. High voltage is supplied to a string of PEP-II tubes from one of two supplies, serving approximately 15 tubes each. The raw charge pulse from the PMTs is sent directly, following a 1dB attenuator, to the readout system. Thus the readout system has to accommodate mixed-mode detector signals. Note that the PEP-II units have no provision for an LED test signal input. In addition to the undulator, additional PEP-II BLM detectors were installed near upstream collimators and the Undulator tune-up dump in the Linac-To-Undulator beamline.

SYSTEM OVERVIEW AND DESIGN

The original system design accommodated the ANL detector systems exclusively. This design was modified in

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order to include the PEP-II units. Figure 1 shows the system diagram with ANL detectors. The PEP-II installation differs in that there is no BLM-IB, and the PEP-II high voltage power supply is located upstairs. In both cases, the detectors are located in the undulator hall tunnel, along with the BLM-IM for the ANL units, and the readout systems are located in service buildings, which are located at the beginning and end of the undulator line.

The MPS BLM Link-Node

Readout and control of the BLM detectors and support electronics is accomplished by the LCLS Machine Protection System (MPS) BLM Link-Node (L-N) chassis. One BLM L-N can serve eight BLM detector channels. There are a total of six BLM L-Ns in the system: the original five serving the Undulator BLMs and an

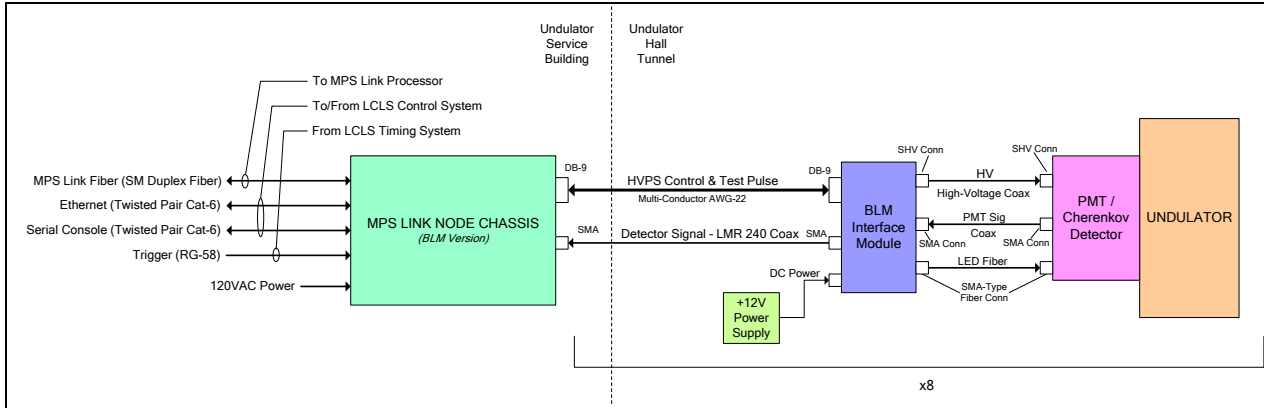


Figure 1: LCLS Undulator Beam Loss Monitor system block diagram – ANL detectors

A system design goal was to keep as much of the readout electronics out of the tunnel as possible. This is for serviceability as well as to avoid additional heat loads in the tunnel, which must be kept at +20 deg Celsius ±1deg C for the undulator magnets.

The longest cable run from tunnel to service building is approximately 100 meters. The detector signals are transmitted over high-quality LMR-240 coax cable, with SMA connectors at each end. The BLM-IM control signals are transmitted over a multiconductor cable consisting of four individually shielded (only three are used), AWG22 twisted pair cables with foil shield and drain wire, wrapped by an overall foil shield which is encased in a low-smoke non-halogenated jacket. This cable is terminated with DB-9 connectors at each end. The controls signals present are the analog HVPS set and readback, both driven differentially on the cable, and a digital RS-485 level test pulse that drives the test LED, also differential. Grounding and shielding of the differential pairs is handled carefully, with only one end of each individual shield connected to ground at the sending end. Local +12VDC power is supplied to each BML-IB by standard “wall-wart” power supply units that have been carefully chosen and evaluated.

The PEP-II HVPS voltage is carried down to the PMTs using Type-C high voltage coax. In the tunnel, this HV is daisy-chained to the string of PMTs, with standard SHV connectors on RG-59 cables. The PEP-II HVPS units receive power and control from the readout system. These power supply units are also re-purposed from PEP-II and have an added signal conditioning unit, designed to match the control and readback voltage levels of the ANL units. This allows direct connection to the readout system.

additional chassis installed to serve the added LTU BLMs. The L-N is a component of the LCLS MPS [5]. The MPS consists of an array of Link-Node chassis which connect to various status and mitigation devices. The L-Ns are connected to a central Link Processor via Gigabit Ethernet links in a star topology, over a private fiber optical network. A commodity GigE switch connects the Link-Nodes to the Link Processor. The Link-Processor, a VME CPU, runs the MPS algorithm, polling all L-Ns on the network for status at 360Hz. The LP is connected to the LCLS Timing Event system and receives a 360Hz interrupt from it. This invokes the message passing / status checking / fault mitigation operation between the LP and individual L-Ns. The MPS is capable of responding to a fault condition within 1/360th of a second by either halting or rate-limiting the beam.

A block diagram of the BLM Link-Node is shown in Figure 2. The MotherBoard (MB), common to every type of L-N, contains a Xilinx XC4VFX20, Virtex-4 FPGA. This FPGA implements the core MPS function of fault detection and reporting. The FPGA’s Multi-Gigabit Transceiver and MAC core implement the Ethernet interface to the LP. The FPGA contains a fault memory which is then read out over Ethernet. A USB 1.1 interface port is included on the MB as a local diagnostics and control port. When connected to a host system, the unit’s full fault memory, control, status and diagnostics functions are available. Additionally, an embedded ColdFire CPU (Arcturus Networks uC-528XF) has been integrated into the MB. This CPU is used for the EPICS interface and provides control, status, diagnostic and housekeeping functions between the L-N and the LCLS control system. It should be noted that the actual fault handling mechanism is separate and isolated from EPICS.

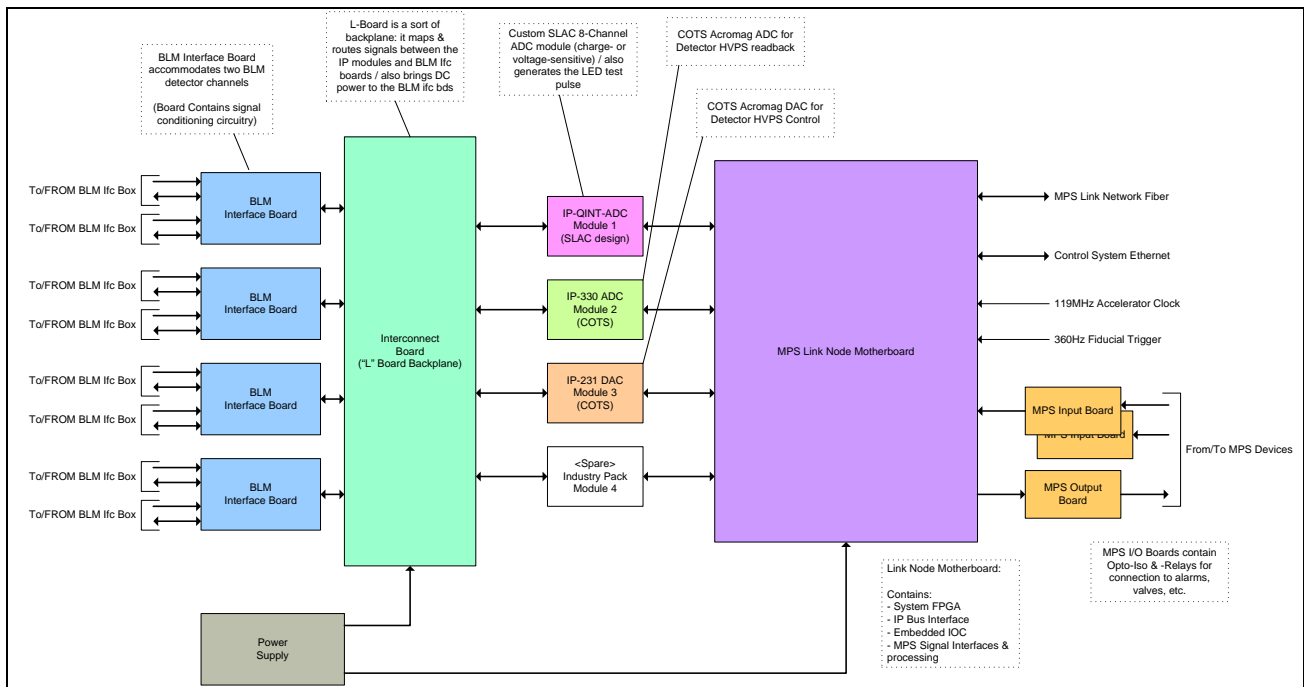


Figure 2: The BLM Link-Node Block Diagram

The BLM L-Ns serve standard digital MPS input and output devices. Inputs are connected to the motherboard by plug-in boards. MPS Input boards contain 16 optical isolators for interface with devices, typically at +24V levels. The MPS input signals are debounced digitally with a 100us minimum time constant. The MB has provision for six input boards, giving a total of 96 inputs. One MPS digital output board is also available to provide outputs to mitigation devices. Eight channels of optically isolated solid-state relays are provided.

The BLM version L-N adds some more hardware to the base L-N. The HW added to the Link-Node for the BLM version is shown in the left-hand side of Fig. 3. These items implement the data acquisition and control functions of the BLM system and interface with the BLM detectors and front-end electronics.

The MB was also designed with a general-purpose Industry Pack [6] interface, capable of supporting up to four IP modules. The IP interface logic is implemented in the FPGA. The BLM readout and control is handled by three individual Industry Pack (IP) modules inside the Link Node. One of these is custom (the IP-QINT-ADC) while the other two are commercial off the shelf (COTS). The two COTS modules consist of an Acromag IP-231 16-channel, 16-bit DAC and an IP-330A 16-channel, 16-bit ADC. These two modules are used to set and read back the system high voltage power supplies, respectively.

The signals from the IP modules are routed to the BLM Interface Boards by way of the Interconnect Board L-board (called L board because of its shape); the L-board also provides power the BLM Interface boards. This board is passive except for some buffer devices for the LED Test pulse.

The BLM interface boards contain interface and signal conditioning circuitry for the physical interface to the BLM detectors. This board contains an analog differential driver and receiver for the HVPS control and readback, and a differential RS-485 driver for the LED test pulse. The PMT signal is not processed or conditioned on this board (other than an input overvoltage protection circuit) and is passed directly to the IP-QINT-ADC module. Careful routing and shielding of the detector signals is done to minimize noise and crosstalk. This interface board serves two detector channels. Four are required for a complete BLM Link-Node.

Triggering and Data Acquisition

The BLM L-N also receives a 119Mhz clock with phase-modulated 360Hz fiducial from the LCLS Timing Reference Distribution system [7]. The motherboard processes this signal and extracts the 360Hz fiducial to form the BLM system trigger. The delay of this trigger is settable from EPICS. The system triggers at 360Hz, performing its BLM acquisition, signal processing and fault checking operations. Note that the maximum LCLS beam rate is 120Hz. Three measurements occur at each trigger: Beam, Test and Pedestal. A timing diagram is shown in Fig. 3. The Beam measurement interval acquires the actual BLM detector data. Timing is adjusted so that the detector signal arrives within the Beam gate. Approximately 900us later, the Test acquisition interval sends the LED test pulse to the detector and acquires the resultant detector signal. At 900us after this interval, during the system “quiet time”, the Pedestal measurement acquires any offset voltage present in the detector and front end electronics. In charge integrating mode, a 2.5us gate is opened at the start of each measurement interval.

Charge is collected for 2 μ s, and the resultant integrated voltage is sampled 500ns before the close of the gate.

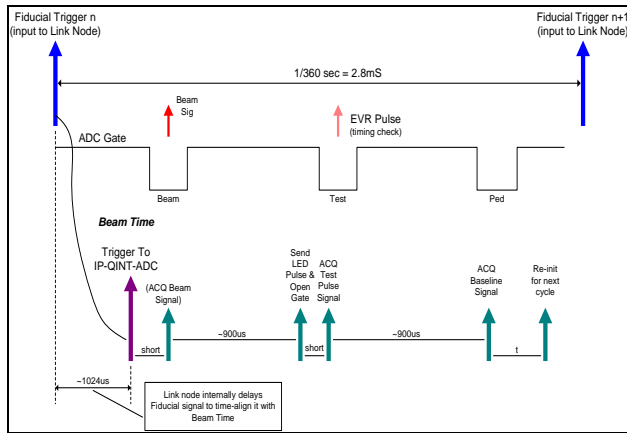


Figure 3: BLM System Data Acquisition Timing

For voltage-sensitive mode, the gate signals are still present and timing relationships are the same except that a voltage signal is sampled.

Since the various timing delays in the acquisition subsystem are SW programmable, there exists the possibility that a wrong setting could cause the beam signal to get missed, never indicating a fault. A separate fault checking mechanism was employed using the LCLS timing system Event Receiver to inject a 360Hz trigger pulse into the analog front end (via an RF directional coupler) during the Test acquisition interval of a non-ANL channel. This produces a signal that could be thresholded. If timing changes the level of this signal varies, exceeding the thresholds and indicating a fault.

IP-QINT-ADC

The IP-QINT-ADC is the functional core of the BLM readout system. This module (called the QADC) was custom-designed for MPS BLM and Protection Ion Chamber (PIC) applications. It consists of eight HW programmable charge-integrating or voltage-sensitive ADC channels and a signal processing and fault checking subsystem implemented in a local FPGA. The BLM version QADC also generates the LED test pulse for the ANL BLMs. The programming of input sensitivity type is set by four resistors per channel. All analog inputs are terminated into 50 ohms at the QADC. For each channel, the analog front end consists of a single opamp integrator with a 100pF integration capacitor. Integration is controlled by the gate signal, generated by the QADC FPGA. When the gate is closed, the integration capacitor is shorted. The integrator is followed by a shaping amplifier with a gain of +3.74 and a 1.24 μ s shaping time constant. The gain was chosen so that the maximum output of the ANL preamp (+1.5V) will present a near full-scale input to the ADC. For the integrator, the corresponding maximum charge input is 134pC. When in voltage mode, the integrator is bypassed and the input is connected directly to the shaping amplifier. In voltage sensitive mode, the maximum charge (via the charge-sensitive preamp in the BML-IM) that the system can

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read is 200pC per channel. The ADC is an Analog Devices AD7656 16-bit successive approximation device configured with a +/-5V bipolar input. All eight input channels are sampled simultaneously.

Special signal processing is done on the sampled data. The sampled pedestal data is summed for 360 samples and its average taken. The averaged pedestal is used to subtract of the offset present on the Beam and Test data samples. The pedestal-corrected most recent Beam and Test data samples are integrated over several different intervals to provide integrated dose measurements. The integration is performed digitally on a sample $x[n]$, according to the relation:

$$y[n] = y[n - 1] + x[n] - y[n - k]$$

The first two terms form the integration function, with the last being the leakage term; subtracting off the k^{th} sample in the array, limiting the integration to a fixed rate. These rates are 1Hz, 10Hz, 30Hz and 60Hz. These sums are also used for rate limiting and recovery. The most recent and integrated data are then presented to a fault checking block inside the same FPGA that compares them with a windowed threshold. If outside, a fault bit is set.

Fault Reporting

The L-N MB polls the QADC at 360Hz and stores this fault data in its local fault memory, which is then sent to the LP. A done/ready handshake is employed between the QADC and L-N MB FPGA state machine, ensuring that valid fault data is read. The BLM faults are copied into the L-N MB FPGA fault memory by that FPGA's state machine. The MB FPGA also applies window thresholds to the HVPS readback values on each channel. Any excursions outside the fault windows are indicated and sent to the LP, along with the BLM faults. Additionally, the most recent and accumulated data values are made available for read out over EPICS.

System Software

The control of the IP modules, setting of fault thresholds, trigger delays, and other housekeeping functions are controlled via EPICS with the embedded CPU running the RTEMS real-time operating system. A set of EPICS EDM GUIs have been created for system control, status and diagnostic functions. The fault reporting is handled by a separate set of MPS software, with faulted conditions being mirrored in the EDM GUIs. BLM faults are individually bypassable in the global MPS application.

OPERATIONAL EXPERIENCE AND PERFORMANCE

The BLM System was commissioned in the winter of 2009. Overall, the system has performed well in its primary MPS function. Many things were learned during

the commissioning process, which led to fixes and improvements in the system.

Several channels exhibited large noise signatures. After some effort, the noise sources were identified to be AC power in one case and signal transmission from a klystron modulator through a cable in the same tray as the BLM detectors in another. The noise sources were mitigated by shielding, grounding and isolation.

Studies were performed to determine the sensitivity of the detectors, both PEP-II and ANL. The results of these studies showed that the ANL units were more sensitive.

Another study was undertaken to understand the noise contributions of the electronics since it was noticed that the voltage-sensitive channels tended to be quieter than the charge-sensitive ones. The study showed that the analog integrator circuit was susceptible to noise pickup and crosstalk from clocks and other signals within the BLM Link-Node chassis. While able to perform its primary Machine Protection well, this noise has limited the ability to make meaningful radiation dosage measurements. Work continues in understanding the various radiation mechanisms seen by the detectors as well as the differences between measured versus expected loss levels.

Figure 4 plots the one-second sums of several BLM channels while a beam finder wire is inserted. The figure is an EPICS stripchart plot showing the loss signal induced when beam finder wire 26 was inserted. The beam is running at a rate of 10Hz and the gaps between peaks is due to the beam being toggled on and off with BYKIK, the upstream undulator beam kicker magnet. The largest loss signal seen is on the BLM on girder 33, as expected, because the loss radiation peaks approximately 10 girders beyond the inserted finder wire.

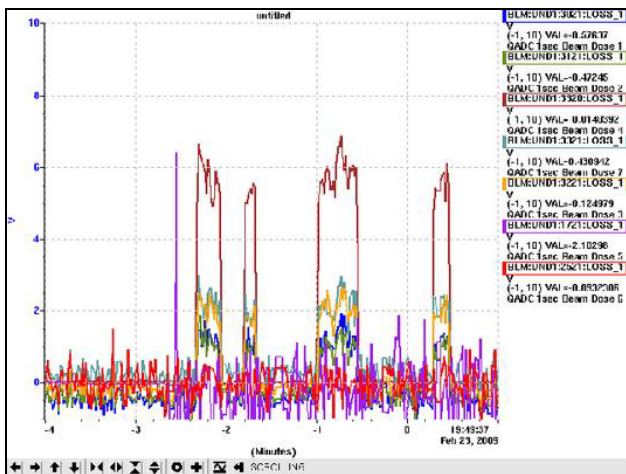


Figure 4: Measured Beam Loss from inserted BFW.

UPGRADES AND FUTURE PLANS

In its current configuration the system contains only five ANL BLM detectors. In late 2009, funding was secured to construct the remaining ANL-type BLM detectors and interface modules. These new units will

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replace the PEP-II units in all locations along the undulator. Construction is progressing and at the time of this writing, with full delivery of the ANL units is expected by summer 2010.

In anticipation of these units, the timing check mechanism for the BLM L-Ns was modified into a more permanent configuration: the directional coupler will not be usable when all channels are occupied with ANL units. Instead a hardware modification was made to the Link-Node's L-board that will allow the LED test pulse to be directly driven by an EVR trigger, instead of the QADC. The change was implemented during the 2009/2010 winter downtime, tested and shown to work. The checking mechanism is sensitive to within ± 200 ns.

Other feature enhancement upgrades to the MotherBoard and QADC FPGAs have been implemented, along with the supporting software and are currently in the integration testing phase. These improvements include added watchdog timers to guard against system failures, extended integrated sum readouts, extended threshold setting ranges and individual threshold settings on all accumulated sums and most recent data values. The latter is required for the MPS rate recovery feature, which is scheduled to be commissioned in 2010.

Longer term plans in implement Beam-Synchronous Acquisition (BSA) in the BLM system to allow recording of loss data coincident with beam events. This will be very useful for loss radiation studies.

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