THE DEVELOPMENT OF HIGH STABILITY MAGENT POWER SUPPLY*

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Abstract

This paper presents the magnet power supply (MPS) for the beam correction magnet. The required current to the magnet was ±20 A. The MPS has been implemented using the digital signal processing technology using the DSP, FPGA, ADCs and analogue and digital circuits. An embedded module was adapted for the Ethernet connection. The output current stability of the MPS showed about 10 ppm peak-to-peak in short term experiment. The long term stability was also ~10 ppm for eight hours. The other experimental results such as line regulation, and bandwidth were given in this paper.

INTRODUCTION

The Pohang Light Source(PAL) has been constructing the PAL-XFEL accelerator that needs many kinds of magnet power supply (MPS). The MPSs are nowadays developed by the digital technologies using digital signal processor (DSP), FPGA, ADC and so on. The DSP was primarily optimised for the various digital signal processing with the fast calculation time such as feedback control, digital filters, stand alone controller etc. And it includes many hardware functions to make it easy to interface the peripheral devices through the SPI, CAN, RS232C, I2C, ADCs etc. Thus the application areas of the DSP increased sharply in the various applications, especially in power conversion systems – high quality power supply, UPS, inverter, etc. [1].

The other trend in circuits design for the electronic system is that the FPGA gets popularity in the wide application area because it gives flexibility in circuits design to the designer. It can be made the complicated random logic simple. The FPGA makers also provide various useful IPs thus circuits design is very easy, furthermore it gives very high performance and density [2]. The high stable MPS circuits generally combined a DSP with FPGAs to get the fast calculation time. The digitally controlled MPS was at the many accelerator laboratories. The performance of MPS improved better but its size smaller by every year. The MPS was also required the embedded Ethernet connection for EPICS which was the general control architecture in accelerator machine [3].

In this paper, we present the various design schemes and experimental results of the high stabile MPS for corrector magnet of the PAL-XFEL.

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SYSTEM CONFIGURATION

The system configuration of the designed MPS is shown in the Fig. 1. The input stage is rectifier circuits with a damped low pass filter to get stable output stability. The bandwidth of the input filter should be less than 30 Hz with a small under damp. The out stage is H-bridge topology using the four FETs with cascaded low pass filters to make the output current smooth and remove the switching noise. The output stage was isolated to the control circuits in order to minimize the switching noise influence.

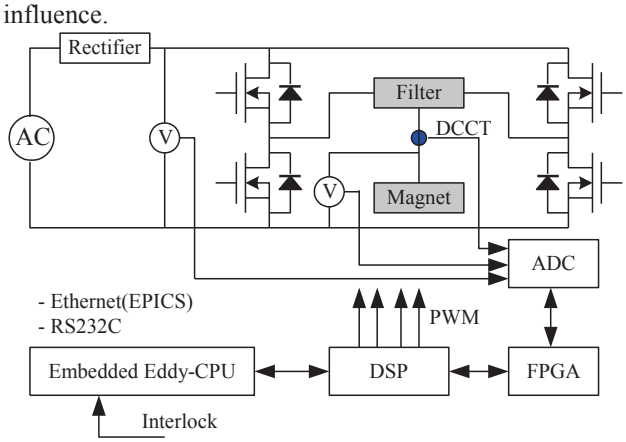

Figure 1: Block diagram of the magnet power supply.

The DSP TMS320F28335 from TI Co was adapted to control the overall power supply system. It has six high resolution PWM outputs with 150ps micro edge position which is the absolutely required function to archive the ~10 ppm output stability [4].

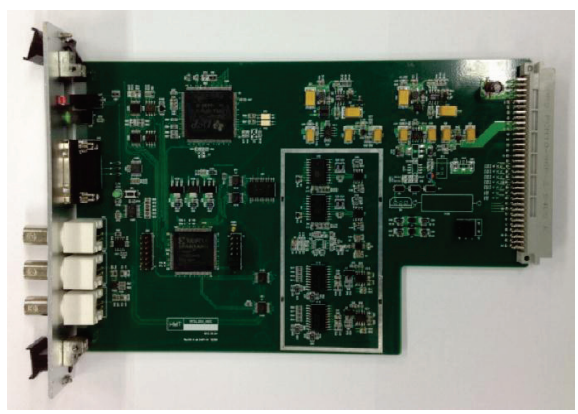

Figure 2: DSP Board that includes DSP, FPGA, ADCs and the other logics.

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An Eddy-CPU from Systembase Co. which is a high performance embedded CPU module with powerful ARM9 core processor is applied to the MPS for the Ethernet connection to the main control system and to interface the interlock signals. Four ADCs are assembled to get the value of the output current, output voltage and link voltage. The ADCs are interfaced by the XC3S400 FPGA from the Xilinx Co. The FPGA generated SPI control signals to the ADCs respectively, processed the transferred data and temporarily saved them in the registers until the DSP requested them. The output current was measured using DCCT MACC150 from HITEC which converted down the current of ratio from 1000 to 1. Its current output was translated to voltage by the burden resistor of 50 Ω which has small temperature coefficient.

The control loops for the designed MPS are given in Fig. 3. A cascaded current and voltage feedback loop was applied to the MPS compensator. The inner loop controls the output voltage, and the outer loop controls the output current. The pole of the PI compensator should be ~KHz to get better dynamic responses to the noise coming from input and output terminals.

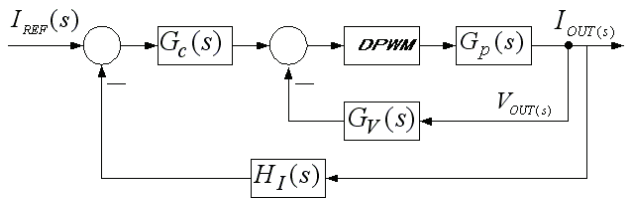

Figure 3: Block diagram of complete current loop system.

For the cascade control loop :

- The inner voltage loop used to reject the voltage fluctuation of the output stage.
- In cascade loop control, the inner voltage loop has a small time constant comparing to outer current loop.
- The inner voltage loop in a cascade control should be tuned before the outer current loop.
- After the inner voltage loop is tuned and closed, the outer current loop tuned using the responses of the inner loop.

The inner loop should have wider bandwidth to that of the outer loop thus it was shown as constant by the outer loop. The closed-loop transfer function of the MPS is given by:

$$H(s)=\frac{I_{out}(s)}{I_{ref}(s)}=\frac{G_c(s)G_{in}(s)S_I(s)}{1+G_c(s)G_{in}(s)S_I(s)}$$

Where $G_{in}(s)\equiv G_P(s)G_V(s)/(1+G_P(s)G_V(s))$ is the equivalent transfer function of the inner loop. The control loops were executed at every PWM switching frequency. The PI compensator was described as following:

$$u(t)=K_p e(t)+K_I\int_0^t e(t)dt$$

where, $e(t)$ is error coming from difference between reference and output signal, K_P and K_I are the proportional and integration gain, respectively.

The output filter was configured with two stages. The first is the major part influencing the system response directly, and second is to remove the switching noise. The cut-off frequency of the second stage is placed after half of the switching frequency. The output filter recommended to have the parallel damped type with condition of $C_2=4C_3$ [5].

The output filter with magnet load was simply modelled as Fig. 4, which has eliminated the second stage to make the equation simple. In Fig 4, the R1 and L1 were equivalent circuits for magnetic load, and C2, R2 and L3 for filter construction. The transfer function of the Fig. 4 was shown in the equation given by:

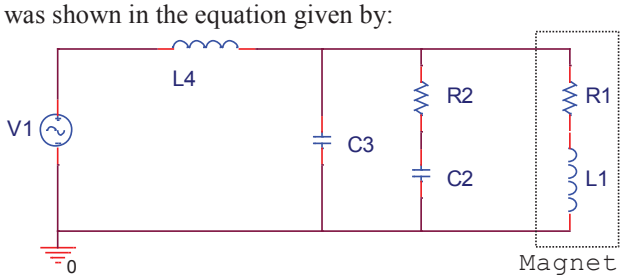

Figure 4: The modelling of output filter and load magnet.

$$\frac{I_{out}}{V_1}=\frac{1+sC_2R_2}{a_4s^4+a_3s^3+a_2s^2+a_1s+a_0}$$

Where,

$$a_4=L_1L_4R_1R_2C_3$$
$$a_3=L_1L_4C_2+L_4R_1R_2C_2C_3+L_1L_4C_3$$
$$a_2=C_2L_4R_2+C_2L_4R_1+L_4C_3R_1+C_2R_1R_2$$
$$a_1=R_1$$

The integrated model both switching and filter circuits were simulated using the PSIM and its result was shown in Fig. 5. The output current swing shows less than 2 ppm at the 40 kHz switching frequency.

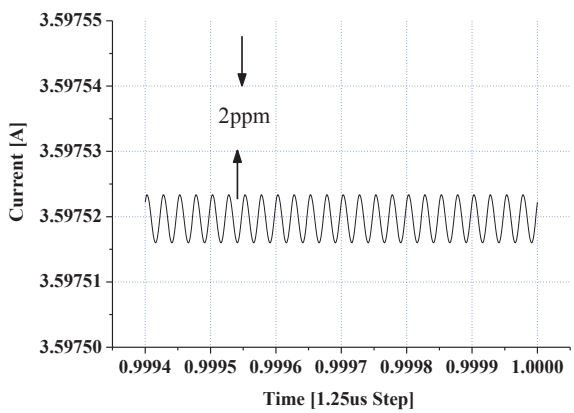

Figure 5: Current output signal simulated by the PSIM to the output filters and magnet load.

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EXPERIMENTAL RESULTS

Eight hours long term current stability was measured using the HP3458A digital voltmeter from Agilent Co, and the results are shown in Fig. 6. The current stability with load was less than 10 ppm at 20 A output current.

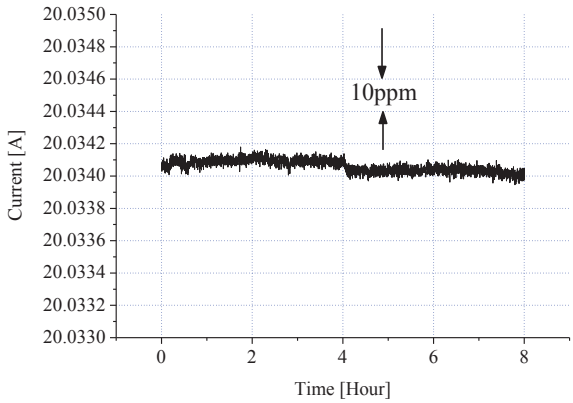

Figure 6: Long term stability test results.

The zero cross response of the MPS was also shown in Fig. 7. When 5 ppm step of the input current was increased from 0.001 A to -0,001 A, the MPS showed a good output responses.

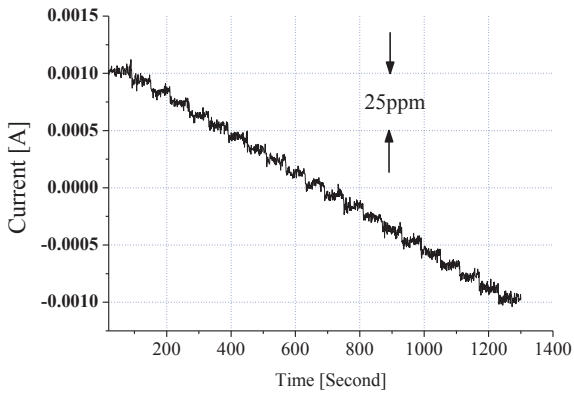

Figure 7: Test results of the zero cross responses.

The step responses of the MPS from 0 to 20 A maximum is shown in Fig. 8.

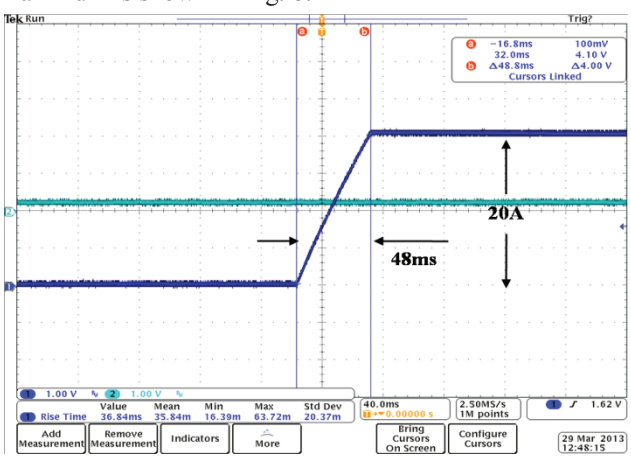

Figure 8: The response of step function from 0 to 20 A.

The band width is about 10 Hz where load inductance is 35 mH, link voltage is 24 V and the PWM duty is limited to the 80 % to the maximum.

Figure 9 shows that the short term stability is within 10 ppm for 3 minutes. The line regulations are also good responses when input AC line voltage is varied about 10 % from its normal voltage of AC 220 V.

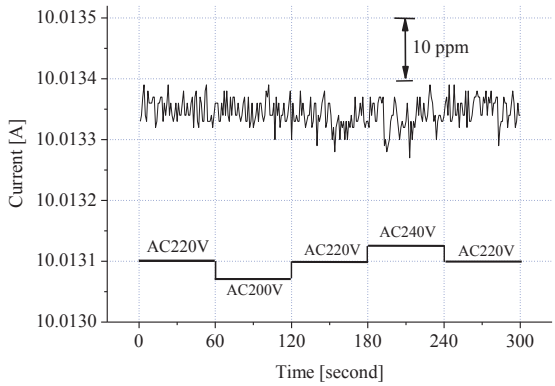

Figure 9: Short term stability and line regulation.

CONCLUSIONS

This paper described the DSP-controlled bipolar power supply for the corrector magnet. The designed digital controller includes DSP, FPGA, ADCs and the other analogue and digital circuits. The cascaded control loops for the load voltage and the current are designed. The two stages of output filters were designed and showed the simulated results. The experimental results with the assembled MPS showed the high stability. The short term stability is about 10ppm and long term stability for eight hours is about 10 ppm. The zero cross response of the MPS showed that there was no non-linearity when crossed the zero region. The band width of the MPS measured an oscilloscope when maximum step current was applied was about 10Hz under the safety duty margin of 20 %.

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