OVERVIEW OF THE BPM SYSTEM OF THE ESS-BILBAO

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Abstract

In this work is presented the design of the *Beam Position Monitors* (BPM) from ESS-Bilbao (ESSB), including the test bench, electronics and practical results. The test bench uses four capacitive buttons welded to the beam pipe. These are connected to an Analog Front-End (AFE) unit, based on logarithmic amplifiers and IQ demodulators, where the signals are conditioned and converted to baseband to meet the Digital Unit (DU) requirements. The DU (ADC and FPGA) includes a Δ/Σ algorithm, linearization and CORDIC blocks to sample the signals and calculate the position, amplitude and phase. To manage the FPGA a Java interface has been developed including the EPICS integration by means of JavaIOC and Archiver Instance. The measured resolution and accuracy are promising ($<10\,\mu$m for the position and $<1°$ for the phase) provided that the effect of errors such as temperature variations and nonlinearities are minimized through temperature regulation and system calibration.

INTRODUCTION

The new accelerator facility in Bilbao (ESSB [1]) has been conceived as a multipurpose machine which serve as a base for support of activities on accelerator physics and several applications carried out in the frame of different collaborations. Table 1 summarizes the main parameters of the beam and precision requirements of the Beam Position Monitors (BPM) electronics for such accelerator. The design of the BPM system for Bilbao linac has been developed by ESS-Bilbao in collaboration with the Electricity and Electronics Department of the UPV-EHU University.

The BPM electronics, the test bench and the control system designs are presented in the next sections. The control requires to integrate the BPM system into the *Experimental Physics and Industrial Controls System* (EPICS [2]) of the accelerator. The position and phase information which is sent to the control system should be updated at a rate of 2 Hz and recorded to the database with the same rate.

SYSTEM DESCRIPTION

For our BPM system we have been developed a teststand, the electronics and the control system. The electronics consists of two main parts (see Fig. 1):

- An Analog Front-End (AFE) where the signals will be filtered, conditioned and converted to base-band.
- A Digital Unit (DU) to sample the baseband signals and calculate the beam position, amplitude and phase.

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Table 1: Main Parameters of the Future ESS-Bilbao Proton Linac and Requirements of the BPM System

Beam Parameters	
Max. proton current	90 mA
Max. final energy	300MeV
Max. beam power	75 kW
Max. repetition rate	50 Hz
Pulse length	1.5 ms
Bunch frequency	352.2 MHz
Resolution and Precision Requirements	
Position resolution	10 μm
Position precision (absolute)	100 μm
Phase resolution	0.3°
Phase precision (absolute)	2°

The control system is based on a high performance FPGA, connected to a Host PC which works as an EPICS server. The communication between both parts is made by a register bank implemented in the FPGA, being accessible using a Compact PCI bus (cPCI). For the tests the host PC was replaced by a local PC connected to the FPGA to control the system in a MATLAB-Simulink environment.

Analog Front-End Unit

The Analog Front-End (AFE) unit is where the BPM signals will be filtered, conditioned and converted to baseband. The method used to convert RF signals into baseband is based on the ESSB *Low Level RF* (LLRF) system [3], due to its easy and versatile implementation.
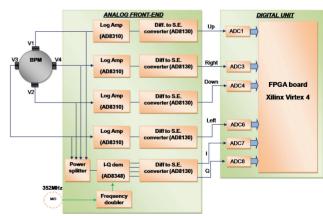

Figure 1: Electronics of the BPM system.

This solution is implemented using a logarithmic amplifier (log amp) for measuring the position and one IQ demodulator (AD8348) fed by the sum of the four button sig-

nals measuring the amplitude and phase of the beam. To measure the X and Y positions, a 4-channel log amp board was developed, where each channel is connected to one of the four BPM buttons. Each channel is based on a fast and high dynamic range log amp (95 dB), the AD8310, with a 50 Ω impedance at the input. Its bandwidth is from DC up to 440 MHz. Each signal is converted from differential to single-ended, using the AD8130 converter, and it is sent to the digital unit. A picture of the AFE is shown in Fig. 2-up.

Several tests have been done to check the requirements of this solution (resolution, accuracy, linearity and noise).

Digital Unit

The Digital Unit includes the FPGA and the Analog to Digital Converters (ADC) boards (VHS-ADC board from Lyrtech company [4] with an additional ADC card). This is a high performance cPCI digital board based on a Xilinx [5] Virtex-4 FPGA connected to an ADC (8 channels, 14 bits resolution sampling up to 105 MHz). The Xilinx System Generator has been chosen as this significantly shortens the programming time. The board includes 128 MB SDRAM for data buffering on the FPGA.

The outputs of the AFE will be sampled by the ADCs and sent to the FPGA for the signal processing. The FPGA includes the linearization (non-linear correction to measure properly non-centered beams) and calibration of the signals to compensate the effect of several errors which can degrade the precision of the measurements. These will include the offset compensation, gain adjustment, CORDIC block [6] to obtain the amplitude and beam phase (arctan(Q/I)) and an estimation of the beam current ($\sqrt{I^2 + Q^2}$) and a Δ/Σ algorithm [7] giving the position.

Test Bench

In order to test the performance of the BPM electronics, a test bench has been developed by ESSB using four ceramic feedthroughs as button pickups (Fig. 2-down), welded to the beam pipe. The relative position of the internal tube simulating the beam can be changed with respect to the outer tube within a range of 20 mm approximately for both X and Y axis with a positioning resolution less than 10 μm using the corresponding micrometer knobs. The test bench is connected to the AFE unit (Fig. 1) as well as the necessary RF equipments to simulate the beam.

BPM Control System

The BPM control is a multipurpose configurable system [8] based on a high performance FPGA for a fast control which ESSB has used also for related applications such as LLRF [3]. It is connected to a Host PC which works as an EPICS server using JavaIOC [9] for the networked control to allow a distributed control. The communication between both parts is made by a register bank implemented in the FPGA for storage of parameters and calculations. This register is accessible by the PC through a cPCI bus.
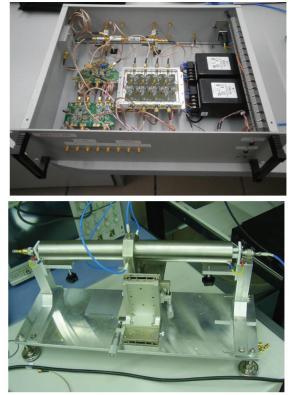

Figure 2: Up: Analog Front-End unit, with log amp and IQ demodulator boards. Down: ESSB BPM test bench.

The initialization values and the numeric representation of the digital signals are configured by XML files. A MySQL database is integrated in EPICS via RDBArchiver and Control System Studio (CSS) created by the Spallation Neutron Source (SNS), Oak Ridge, Tennessee [10].

PRACTICAL RESULTS

The ESSB BPM system has been tested using the described test-stand, AFE and DU. Several tests have been carried out to measure drift, noise and linearity of the system, monitoring the outputs of the FPGA using a local PC.

To simulate the beam a signal generator of 14 dBm and 175 and 352 MHz was used. Taking into account the components and test bench's impedance mismatches (S_{11}), the simulated beam intensity is 14.14 mA. The actual linac beam current can be several times larger than this value, so signal to noise ratio will improve in the real accelerator. The signals from the test-stand were connected to the log amp board and added as the input of the IQ demodulator with the reference provided by the Master Oscillator (MO). The system was tested continuously for several days in an unregulated temperature environment, showing some signal drifts as the result of these temperature variations.

As Table 2 shows, the obtained resolution and accuracy of the signals fulfill requirements. These results are similar at both frequencies, verifying the suitability of IQ demodulators for 4-quadrant beam phase measurements and showing an accuracy of 1°. The resolution and accuracy indicate that with this solution the effect of several errors such

Table 2: Resolution and Precision for Position and Phase

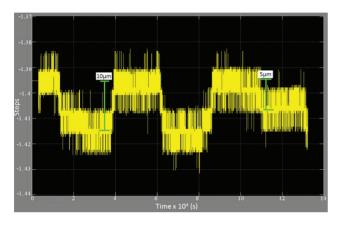| Parameter	Measure	Unit
X Position resolution	9.77	μm
Y Position resolution	9.14	μm
X Position precision (absolute)	48.84	μm
Y Position precision (absolute)	50.27	μm
Phase resolution	0.2	°
Phase precision absolute	1.3	°

Figure 3: Sensitivity of the BPM electronics.

as temperature variations and nonlinearities are minimized through temperature regulation and system calibration.

The accuracy and resolution values shown in Table 2 were obtained from measured steps of the FPGA taking into account the dynamic range of the test bench. These values were verified manually changing the position of the beam pipe relative to the simulated beam. Figure 3 shows that the electronics is sensitive to changes around 5 μm.

A linearity test have been done to characterize the system. The BPM mechanical center does not correspond to the electrical one, which is caused by mechanical distortions and impedance mismatch of the buttons. The BPM is more linear in the central area (box in Fig. 4). Due to its non perfect linearity a linearization block should be added to the FPGA (using MATLAB in this test). The horizontal (x) and vertical (y) beam positions are represented by the map functions up to a fouth-order polynomial [11]:

$$x_{real} = \Sigma_{i,j=0}^{4} a_{ij} \cdot X_{measured}^{i} \cdot Y_{measured}^{j} \qquad (1)$$

$$y_{real} = \Sigma_{i,j=0}^{4} b_{ij} \cdot X_{measured}^{i} \cdot Y_{measured}^{j} \qquad (2)$$

where a_{ij} and b_{ij} are the coefficients of the map functions, which are derived by fitting the map data to the map functions by using a leastsquares fitting procedure. After calculating the coefficients and adding the corresponding linearization block, a new test has been done to prove that the linearity of the BPM greatly improves (Fig. 4).
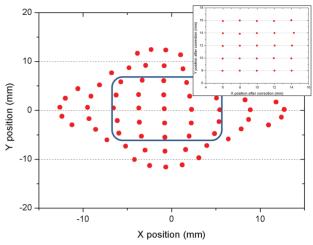

Figure 4: Positions before and after linearization (inset).

SUMMARY AND CONCLUSIONS

With the objective of developing the BPM system for the ESS-Bilbao linac, a test-stand and an analog front-end unit have been developed by ESSB in collaboration with the Electricity and Electronics Department of the UPV/EHU. The outputs of the AFE are sampled and fed into a Virtex-4 FPGA for the signal processing using a commercial digital unit controlledd by a PC. A control system based on EPICS has also been developed. Several tests were performed to measure drifts, noise and linearity leading to resolution and accuracy values fulfilling the ESSB requirements.

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