SEM-GRID PROTOTYPE ELECTRONICS USING CHARGE-FREQUENCY-CONVERTERS

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Abstract

A prototype system using an ASIC equipped with 8 Charge-to-Frequency Converters (CFC) was developed in collaboration between the Beam Diagnostics (BD) and Experiment Electronics (EE) department at GSI. The maximum sensitivity is 250 fC per output pulse. It will serve as an economic alternative for the readout electronics of Secondary Electron Monitor (SEM) profile grids or comparable beam diagnostic devices like Multi-Wire Proportional Chambers (MWPC). The goal of this contribution is to report on a detailed performance test under real beam conditions at GSI beam lines. A 32-channel electronics is connected to different beam profile SEM-grids at a LINAC beam line and tested with various beam conditions. Transversal beam profiles with a time resolution down to the microsecond range have been recorded successfully. Beam profiles recorded with the new CFC-board and the old standard trans-impedance amplifiers agreed well. Further measurements were done with a Multi-Wire Proportional Chamber. Therefore the prototype was extended to 64-input channels recently.

MOTIVATION

The present SEM-grid electronics for beam profile measurements is outdated and several components produce high purchasing costs and have long delivery times. For this reason BD department has launched efforts to look after a new low cost solution. The decision drawn on the CFC-ASICs developed by the EE department [1, 2]. The following description presents the past efforts and currently results.

FIRST TESTS

For first investigations a readout board for testing the CFC-ASIC was developed. Independent of these attempts the board could already be used for measurement tasks.

First Readout Board

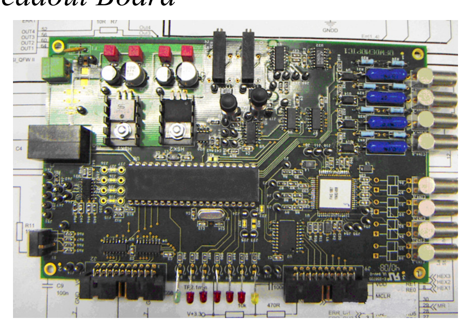

Figure 1: CFC readout test board, with PIC micro-controller, CFC-ASIC, current divider and LVDS-/LV-TTL-drivers.

The main parts of the board consist of the CFC-ASIC, a micro-controller and LVDS-/LV-TTL output drivers. A hex-switch allows changing the CFC charge range and its current polarity. The micro-controller transfers instructions to the CFC. For more information about the CFC see [2] and [3].

Investigations

Several tests were conducted with the measurement setup to characterise the ASIC. The following items give an overview of the investigations done with the CFC:

- Linearity in different ranges
- Range extension (current divider)
- Errors
- Gain synchronicity between channels
- Temperature drifts
- TID radiation hardness (with X-rays)

Results

The results showed that the CFC has advantages as a new electronic design for a beam profile measurement system. For example, the good temperature behaviour (deviation of only 0.7%, with respect to the 20°C reference) and the radiation hardness (functionality was checked up to 11 kGy total dose, irradiated with X-rays) show that the CFC is a promising candidate for the new readout electronics. For more detailed information see [3] and [4].

PROTOTYPE SETUP

Preliminaries

The main objective was to check the CFC-ASICs under real beam conditions at GSI beam lines and with different beam diagnostic devices. For this reason it was decided to look for existing components at GSI, e.g. at EE department different FPGA-I/O VME boards, CPU boards for Ethernet communication and data acquisition systems were already developed and available [5]. This procedure should save development time and yield faster results.

Hardware

For the new development existing parts of hardware were used. The new readout electronic consists of:

- One or two 32-channel motherboard with 8 CFCs
- VME crate
- RIO-2 (CPU and network connection) [8]
- VUPROM (FPGA, CFC-control unit) [9]
- TRIVA (Trigger module for MBS-DAC) [10]
- LEVCON (Level converter box) [11]
- Power Supply for CFC motherboard (+7V/6A)

Therefore it was only necessary to develop a new CFC-motherboard. It contains 8 CFC-ASICs, thus 32 current input channels were realized on each motherboard. The VUPROM board can communicate with one or two CFC-motherboards. This means measurements are possible with up to 64 profile wires.

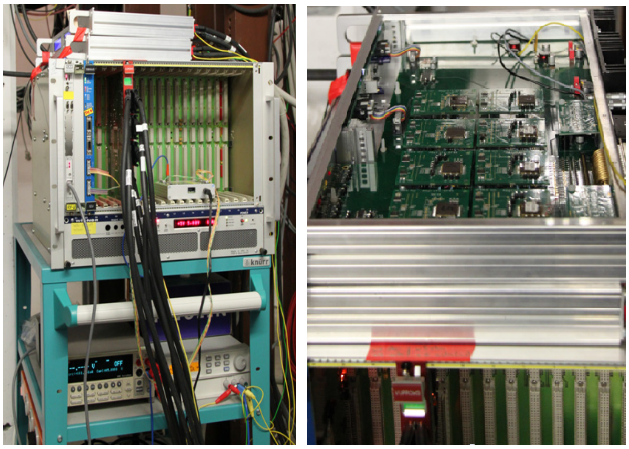

Figure 2: VME crate with hardware setup (left) at GSI beam line. Two prototype boards with 8 CFC-ASICs (right) each were connected with one MWPC.

Software

For data acquisition, viewing of measurement results and setup operation the following software tools were used:

- Go4 (program for data analysis, **G**SI **O**bjected **O**riented **O**n-line **O**ff-line system)[6]
- C-program on RIO-2 board (for CFC settings)
- MBS (DAQ – **M**ulti **B**ranch **S**ystem)[7]
- Terminal program (send CFC instructions to RIO-2)

These program tools like Go4 and MBS were also developed by the EE department. and readily available.

Principle of Function

The CFC-ASICs are controlled by a VUPROM board. Each CFC receives the same instruction from FPGA on the VUPROM board, e.g. current polarity and charge range. The VUPROM itself receives the parameters by a small C-program running on the RIO-2 CPU.

Scalers are implemented in the FPGA. Each scaler counts the output charge pulses of one of the possible 64 CFC output channels. For every time slice the scaler data of all channels are stored in the memory of the FPGA. With the end of data taking for the last time slice the data is sent to the MBS via the RIO-2.

With the present FPGA program version it is possible to handle up to 100 time slices with a time slice resolution between 100 ns and 86 s. The scaler values, which are presenting the beam profiles, are stored in lmd-files via MBS and can be monitored and analysed with the online analysis software Go4. The TRIVA and LEVCON modules manage the MBS trigger operation. The prototype is event driven. An external trigger to the VUPROM starts the measurement procedure. With the end of the measurement of the last time slice the system generates a trigger for the DAQ to signalize that the measurement has finished and the scaler values can be readout. During this time it has to be secured that no new external trigger for the VUPROM is generated.

Performance

The Go4 plots of beam profiles can be presented in different diagram styles. For example it is possible to present a 2D plot like the old existing software at GSI main control room. With the 3D plot Go4 can now present also the variation in time of the measured beam profile – also in different kind of diagram styles. Go4 provides special feature extraction of the measured data for beam analysis. The CFC-ASIC has a high dynamic input range from several pA up to 100 uA. In addition an external current divider is implemented on board to extend the measurement range up to 10 mA. The resolution of the prototype is 0.45 pC (±3σ).

MEASUREMENT RESULTS

The CFC motherboard was tested with two 2x16-wire SEM-grids and one 2x64-wire MWPC at GSI beam lines. In the following sections the measurement result at these beam diagnostic devices are shown. Additional measurements were done with Faraday-cups and ionisation chambers.

Results with SEM-GRIDs

In Figure 3 a horizontal and vertical $^{238}U^{28+}$ ion beam profile with 8.6 MeV/u is shown. The measurements were done at the experimental beam line UNILAC at GSI. Here the measurement values are presented as blocks.

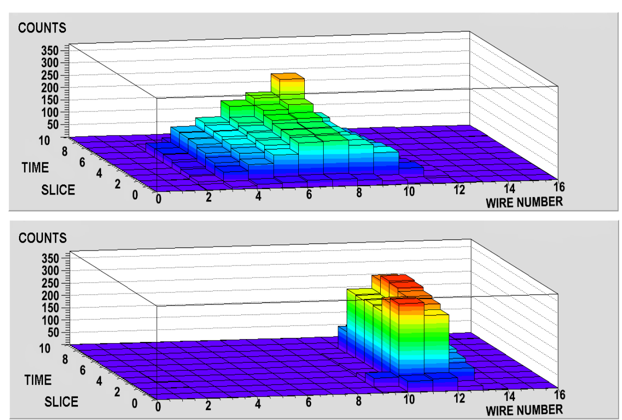

Figure 3: Time dependent horizontal (top) and vertical (bottom) beam profile. Each time slice has a record length of 15 µs with a beam pulse length of 100 µs.

The following diagram (Figure 4) shows now the sum of all charge counts of each SEM-grid wire. This presentation format corresponds to the measurement method of the old existing readout electronic, used in the main control room.

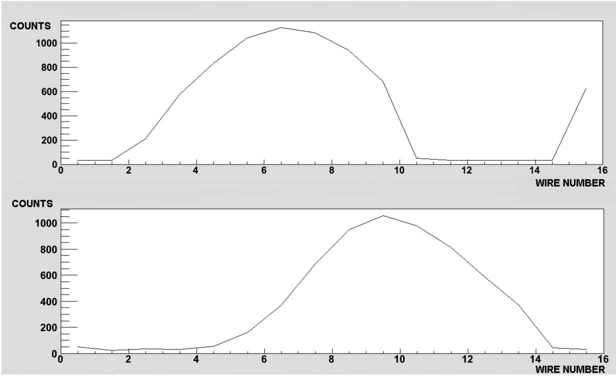

Figure 4: Profiles of a 8.6 MeV/u U^{39+} ion beam. For reference reason, wire number 16 of the x-plane (top) was connected to an external calibrated current source. The y-plane (bottom) of the SEM-Grid is shown also.

Go4 was operated at beam time in online mode. It is also possible to use Go4 "offline" for a detailed analysis of the stored MBS data.

Results with MWPC

Figure 5 and 6 show the beam profiles for a 300 MeV/u $^{40}Ar^{18+}$ ion beam. The measurements were done at the HEBT-section at GSI. 32 neighbouring wires of this MWPC device are connected together to reduce the total number of wires for each grid plane to 32.

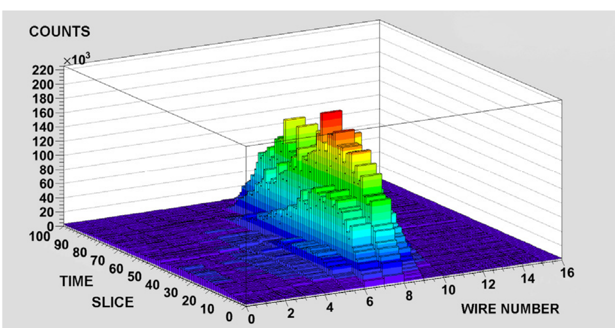

Figure 5: Time dependent horizontal beam profile (first half part of the MWPC x-plane, wire 1 to 16). The beam pulse length is around 1.8 ms, the time slice length is 20 ms.

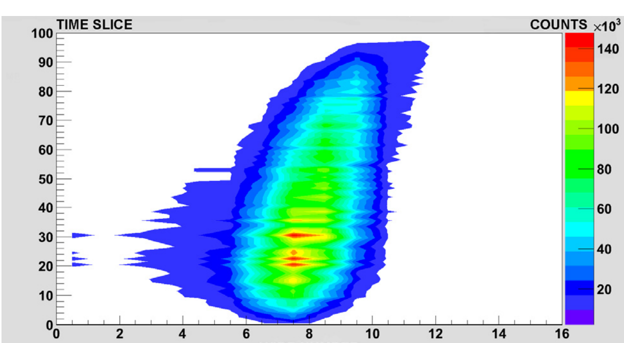

Figure 6: Another presentation format possibility of Go4. Beam pulse and parameter are similar to Figure 5. The colour correspond to the values of the charge counts.

CONCLUSION

The prototype shows successful beam profiles under different beam conditions. The beam profiles as measured with the existing and the new electronics are in very good agreement. The time-resolved beam profiles (3D-plots), which was not possible with the old existing electronic, is now very helpful for future accelerator operations. Also the readout system is flexible enough to be used with other diagnostic devices.

OUTLOOK

Hardware

After further beam tests with different SEM-Grids and a complete analysis of last measurement campaigns it is planned to develop a new prototype board, now with 64 input channels. The counting FPGA, automatic offset correction as well as the network communication will entirely be integrated on this new motherboard. So with this new system the use of VME crate and VME components are no more necessary. This can be a new economical solution for the read-out of SEM-grids, MWPCs and other beam devices (e.g. Faraday-cups, ionisation chambers) at GSI and future FAIR beam lines.

Software

The present software is developed for testing purpose. It will be trimmed in future for the requirements of the daily work of beam diagnostic operating, e.g. automatic offset calibration, automatic charge measurement ranges, calculation of the profiles centre-of-mass, etc.

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