AN FPGA-BASED BUNCH-BY-BUNCH POSITION AND ANGLE FEEDBACK SYSTEM AT ATF2

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Abstract

The FONT5 intra-train feedback system serves as a prototype for an interaction point beam-based feedback system for future electron-positron colliders, such as the International Linear Collider. The system has been tested on the KEK Accelerator Test Facility (ATF) and is deployed to stabilise the beam orbit at the ATF2. The goal of this system is to correct both position and angle jitter in the vertical plane, providing stability of ~1 micron at the entrance to the ATF2 final-focus system. The system comprises three stripline beam position monitors (BPMs) and two stripline kickers, custom low-latency analogue front-end BPM processors, a custom FPGA-based digital processing board with fast ADCs, and custom kicker-drive amplifiers. An overview of the hardware, and the latest results from beam tests at ATF2, will be presented. The total latency of the system with coupled position and angle feedback loops operating simultaneously was measured to be approximately 140 ns. The greatest degree of correction observed was down to a jitter of 0.4 microns at one of the feedback BPMs, a factor of six compared to the uncorrected beam jitter, for a very high degree of bunch-to-bunch correlation.

INTRODUCTION

A number of fast beam-based feedback systems are required at future electron-positron, such as the International Linear Collider (ILC) [1]. At the interaction point (IP) a very fast system, operating on nanosecond timescales within each bunch-train, is required to compensate for residual vibration-induced jitter on the final-focus magnets by steering the electron and positron beams into collision. A pulse-to-pulse feedback system is envisaged for optimising the luminosity on timescales corresponding to 5 Hz. Slower feedbacks, operating in the 0.1 – 1 Hz range, will control the beam orbit through the Linacs and Beam Delivery System.

The key components of each such system are beam position monitors (BPMs) for registering the beam orbit; fast signal processors to translate the raw BPM pickoff signals into a position output; feedback circuits, including delay loops, for applying gain and taking account of system latency; amplifiers to provide the required output drive signals; and kickers for applying the position (or angle) correction to the beam. A schematic of the IP intra-train feedback is shown in Fig. 1, for the case in which the beams cross with a small angle; the current ILC design incorporates a crossing angle of 14 mrad.
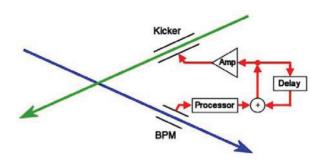
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Figure 1: Schematic of IP intra-train feedback system with a crossing angle. The deflection of the outgoing beam is registered in a BPM and a correcting kick applied to the incoming other beam.

Critical issues for the intra-train feedback performance include the latency of the system, as this affects the number of corrections that can be made within the duration of the bunch-train, and the feedback algorithm. Previously we have reported on all-analogue feedback system prototypes in which our aim was to reduce the latency to a few tens of nanoseconds, thereby demonstrating applicability for 'room temperature' Linear Collider designs with very short bunch-trains of order 100ns in length, such as NLC, GLC and CLIC [2]. We achieved total latencies (signal propagation delay + electronics latency) of 67ns (FONT1) [3], 54ns (FONT2) [4] and 23ns (FONT3) [5].

We report the latest results on the design, development and beam testing of an ILC prototype system that incorporates a digital feedback processor based on a state-of-the-art Field Programmable Gate Array (FPGA). The use of a digital processor allows for the implementation of more sophisticated algorithms which can be optimised for possible beam jitter scenarios at ILC. However, a penalty is paid in terms of a longer signal processing latency due to the time taken for digitisation and digital logic operations. This approach is now possible for ILC given the long, multi-bunch train, which includes parameter sets with c. 3000/6000 bunches separated by c. 300/150ns respectively.

SYSTEM DESIGN

A schematic of the FONT5 feedback system prototype and the experimental configuration in the upgraded ATF extraction beamline, ATF2, is shown in Fig. 2. The ATF can provide an extracted train that comprises 3 bunches

with an ILC-like bunch spacing, selectable in the range 140 - 154 ns. FONT5 has been designed as a bunch-by-bunch feedback with a latency goal of around 140ns, also meeting the minimum ILC specification of c. 150ns bunch spacing. This allows measurement of the first bunch position and correction of both the second and third ATF bunches.

The system is deployed at ATF2 to stabilise the position and angle of the beam in the vertical plane at the entrance to the final focus system to the one micron level. Two stripline BPMs (P2, P3) are used to provide vertical beam position inputs to the feedback. Two stripline kickers (K1, K2) [3,4] are used to provide fast vertical beam corrections. The third stripline BPM (P1) provides a witness of the incoming beam conditions and is used in the calculation of the BPM resolution. The two loops (P2-K1 and P3-K2) are nominally orthogonal in phase advance, in order to correct both position and angle. The system can be operated with the two loops uncoupled running either individually or simultaneously, or with both loops running together and taking into account coupling between them. In general, better results are obtained for the coupled system, as the phase advance between the pairs of kickers and BPMs is not exactly pi/2.

Each BPM signal is initially processed in a front-end analogue signal processor [6]. These outputs are then sampled, digitised and processed by the digital feedback board. Analogue output correction signals are sent to a fast amplifier that drives each kicker.
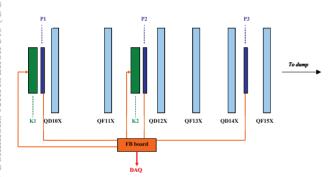

Figure 2: Schematic of FONT5 at the ATF2 extraction beamline showing the relative locations of the kickers, BPMs and the elements of the feedback system.

The design of the front-end BPM signal processor is described in [6]. The top and bottom (y) stripline BPM signals were added and subtracted using a hybrid, to form a sum and difference signal respectively. The resulting signals were band-pass filtered and down-mixed with a 714 MHz local oscillator signal which was phase-locked to the beam. The resulting baseband signals are low-pass filtered. The hybrid, filters and mixer were selected to have latencies of the order of a few nanoseconds, in an attempt to yield a total processor latency of 10ns.

The custom digital feedback processor board is shown in Fig. 3. There are 9 analogue signal input channels in which digitisation is performed using ADCs with a maximum conversion rate of 400 MS/s, and 2 analogue

output channels formed using DACs, which can be clocked at up to 210 MHz. The digital signal processing is based on a Xilinx Virtex5 FPGA. The FPGA is clocked with a 357 MHz source derived from the ATF master oscillator and hence locked to the beam. The ADCs are clocked at 357 MHz. The analogue BPM processor output signals are sampled at the peak to provide the input signal to the feedback. The gain stage is implemented via a lookup table stored in FPGA RAM, alongside the reciprocal of the BPM sum signal for beam charge normalisation. The delay loop is implemented as an accumulator in the FPGA. The output is converted back to analogue and used as input to the driver amplifier. A pre-beam trigger signal is used to enable the amplifier drive output from the digital board.
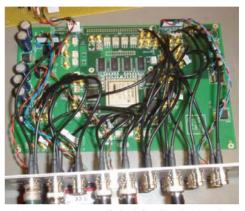

Figure 3: FONT5 digital feedback board.

The driver amplifier was manufactured by TMD Technologies [7], a UK-based RF company. The amplifier was specified to provide +-30A of drive current into the kicker. The risetime, starting at the time of the input signal, was specified as 35ns to reach 90% of peak output. The output pulse length was specified to be up to 10 microseconds. Although current operation is with only 3 bunches in a train of length c. 300ns, this design allows for future ATF2 operations with extracted trains of 20 or 60 bunches with similar bunch spacing.

BEAM TEST RESULTS

We report the results of beam tests of the system performed in 2010; some preliminary results were reported in [8]. We commissioned both the P2-K1 and P3-K2 loops, both individually and in coupled loop mode.

The latency was measured using a special mode of the firmware, where a constant DAC value is set, to provide a constant drive signal and hence a static deflection is given to the beam one complete latency period after the measurement of the first bunch. Provided the total latency is less than the bunch spacing, the effect of the kick will be present in the measured position of bunch 2 and the kick can be delayed in time until the effect on bunch 2 can no longer be seen, effectively mapping out the leading edge of the kicker pulse using the beam position. Data was recorded with interleaved kicked and un-kicked beam for each delay setting used, to mitigate against slow

position drifts, and averaged at each setting to reduce the effect of beam jitter on the measurement. Figure 4 shows the average difference between kicked and un-kicked position as a function of the additional delay applied, for P3-K1, the most critical path for coupled loop operation. The system latency is defined by the point where 90% of the full scale deflection is seen in the kicked beam. For P3-K1 this occurs at a delay setting of approximately 10 ns, which, for a bunch spacing of 151.2 ns, implies a latency of approximately 140 ns.
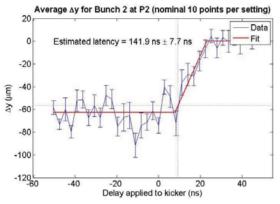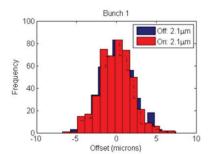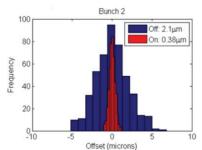

Figure 4: Average difference between kicked and un-kicked positions for bunch 2 at P2, as a function of additional delay applied to the constant amplifier drive. This data was for the coupled loop system and hence represents the latency in the longest path length in the system, P3-K1.

The most important figure of merit of the FONT5 feedback system at ATF2 is its performance on the reduction of the correlated beam jitter in the bunch-train. Position distributions for the three bunches at P2 for coupled loop operation are shown in Fig. 5, for interleaved data with and without the feedback system operating. In the case of bunch 1, the feedback system has no effect, and the jitter with and without the feedback operating is 2.1 μm. For bunch 2, however, the incoming beam jitter with the feedback on is reduced from 2.1 μm to below 0.4 μm. Similarly, for bunch 3, a reduction from 2.3 μm to 1.1 μm was observed. The measured value for the jitter of bunch 2 with the feedback operating implies that the resolution must be at most approximately 300 nm, at least for the BPM processor at P2. The difference between the scale of the correction between bunches 2 and 3 can be accounted for by the difference in measured bunch-to-bunch position correlation, which was 98% for bunch 1 to bunch 2, but only 89% for bunch 2 to bunch 3. The fact that bunch 3 has more random position jitter compared to bunches 1 and 2 is believed to be due to variations in the extraction kicker field at the edge of the c. 310 ns extraction pulse, as was also suggested by a different orbit observed for bunch in the extraction line compared to bunches 1 and 2.

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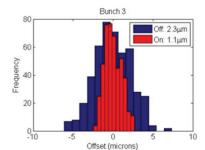[8] R. Apsimon et al, Proceedings IPAC10, Kyoto, Japan, p. 2788.

Figure 5: Position distributions for the three bunches at P2 showing the reduction in measured beam jitter with coupled feedback operation, with interleaved feedback off (blue) and feedback on (red). A rolling average is subtracted from each bunch position to remove the effects of position drift from the jitter distributions. The corrections observed for each bunch were as would be expected given the measured incoming jitter and bunch-to-bunch correlations observed.