OPTIONS FOR NEXT GENERATION DIGITAL ACQUISITION SYSTEMS

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Abstract

Digital acquisition system designers have an always increasing number of options in terms of bus standards and digital signal processing hardware among which to choose. This allows for high flexibility but also opens the door to a proliferation of different architectures, potentially limiting the reusability and the design synergies among the various instrumentation groups.

This contribution illustrates the design trends in some of the major institutes around the world with design examples including VME [1], PCI [2] and TCA [3] based modular systems using AMC [3] and/or FMC [4] mezzanines. Some examples of FPGA design practices aimed at increasing reusability of code will be mentioned together with some of the tools already available to designers to improve the information exchange and collaboration, like the Open Hardware Repository [5] project.

THE GENERAL ARCHITECTURE OF A DIGITAL ACQUISITION SYSTEM

The general architecture of a Digital Acquisition board/system (DAQ) (see Fig. 1), comprises the interface to the instrument Front-End (FE), a processing unit, usually implemented as a Field Programmable Gate Array (FPGA), some memory, a clock recovery and distribution system and the interface(s) to the system bus(es).

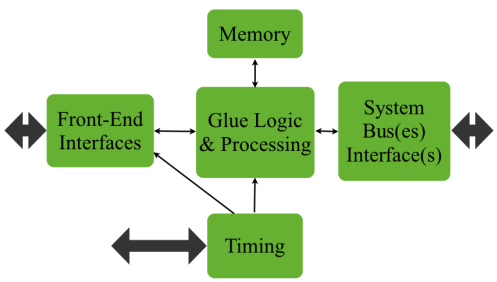

Figure 1: General architecture of a DAQ board/system.

It should be noted that there could be more than one system bus. It is indeed common in case of need for high data throughput to have a dedicated link on each board and leave the shared bus to serve as slow control and for configuration.

The Concept of Carrier and Mezzanine

For a given system bus the main difference between DAQs remains the FE interface and a modular approach can minimize the variations even in this respect. The logic required to implement such interfaces could be implemented as a separate module, a mezzanine, to be plugged on the main board, the carrier.

A modular approach reduces the risks and costs involved in new designs as the complexity of the PCB to be developed is reduced to the minimum. The software development is also speeded up by a modular approach as the system facilities' interfaces, like the clock management unit, remain the same from system to system. Moreover the use of a common carrier simplifies the spare management in an instrumentation group as several instruments can share the most complex and expensive part of their DAQs.

The use of standards for the mezzanines also allows using modules developed in other institutes or for different instruments whenever the requirements are similar, and this even if the system bus chosen for the DAQs is not the same.

There are 2 emerging standard for the mezzanines: the FPGA Mezzanine Card (FMC or VITA-57.x) and the Advanced Mezzanine Card (AMC or PICMG-AMC.x). While the first one results in very simple designs which assume all the processing and complex logic to be on the carrier, the second one requires the presence of a relatively complex FPGA and of some system management logic on the mezzanine itself. The AMC mezzanine will be detailed in the section dedicated to the options for carriers, as it is the basis for the uTCA standard and is mostly used in the high energy physics community in this form.

THE FPGA MEZZANINE CARD.

The FPGA Mezzanine Card (FMC) standard was defined to take full advantage of the great flexibility offered by modern FPGAs' IO blocks. The mezzanine is supposed to be directly connected to an FPGA and the function, direction and electrical standard of the pins is defined at configuration time. The standard foresees that the mezzanine plugged on the carrier could be identified using IPMI [6] (Intelligent Platform Management Interface) commands over a I2C (Inter-Integrated Circuit) bus. This would avoid the risk of loading incorrect firmware resulting in possible bus conflicts. The use of IPMI is a suggestion but not mandatory in VITA-57.

The FMC comes in several flavors. It is possible to have mezzanine with:

- Low Pin Count (LPC) or High Pin Count (HPC) connectors.
- Single width and double width (a double width mezzanine can have one or two connectors as in Fig. 2)

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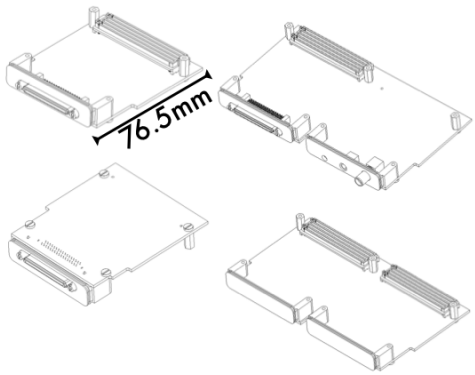

Figure 2: Single and double width FMCs.

The difference between the high and low pin count connector is in the number of pins available, 160 in the LPC and 400 on the HPC, but mechanically they are the the same, allowing a LPC mezzanine to work on a HPC carrier. Designers using LPC have up to 34 differential (68 single ended) user defined IO and 1 multi-gigabit data lane (2 differential pairs) available. The HPC version of the connector offers more user defined IO and 9 more multi-gigabit data pairs. The mezzanine receives 3.3V and 12.0V power supplies.

The FMC standard is rather flexible but offers limited real estate. A single width mezzanine is about 69mm by 76mm, but this is usually acceptable as it is not foreseen to have any complex logic on it. Another downside of the standard is the lack of dedicated carrier to mezzanine clock lines. The few available will most probably be removed in the next revision of the standard.

General purpose IO, ADC, DAC as well as TDC (time to digital converter) mezzanines are already available in FMC format..

OPTIONS FOR CARRIERS

Most of the DAQs in the high energy physics community have been based up to now on VME or PCI, but now a few other standards are being evaluated including xTCA (Advanced Telecommunications Computing Architecture and its derivatives) and VXS (VME switched serial).

The reason to look for new standard is not in the actual bandwidth of the old busses. Indeed in case of need for high throughput, having dedicated links on each DAQ board remains the best option to avoid the bottleneck at the concentrator/switch. Instead, it is driven by in the need to have high bandwidth communication between boards. A typical example of DAQs with such needs are the trigger systems of the experiments, where there is the need to recombine with low latency the information collected by several DAQ boards.

VME

VME, ANSI/VITA 1-1994, is very common standard in the high energy physics community. It was first developed in the late 1970s by Motorola. All the boards share the same bus, on which there is only one master at a time. The VME bus supports several transfer protocols that have been added later to the standard while keeping the same pinout. Boards supporting different transfer cycles can share the same crate. The maximum transfer speed on the VMEbus is achievable with a synchronous cycle called 2eSST and is of 320MB/s.

VME boards can have different form factors, but the most common is the 6U, on which it is possible to have up to 3 FMC mezzanine on the front panel.

The standard allows to have Rear Transition Modules (RTM) connected to the carrier using the user defined pins of the bottom connector (P2). The form factor of those RTMs is not defined in the standard and mostly depend on the crate geometry.

One of the main advantages of this standard is its maturity: over the years many modules have been developed and are now available as COTS (Commercial Off-The- Shelf).

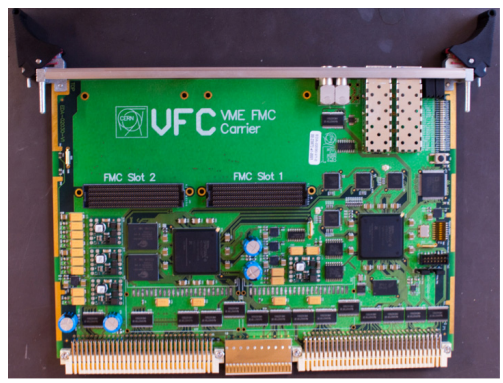

Figure 3: The VME FMC carrier developed at CERN.

Figure 3 shows the VME FMC Carrier (VFC), a board developed at CERN as part of a collaboration between the beam instrumentation and the controls groups. The VFC is a carrier for 2 FMC mezzanines and an RTM module. It has 2 small form-factor pluggable (SFP) transceivers on the front panel for clock/timing recovery and data transmission. Those modules are connected to the Gbit lines of the System FPGA (SFPGA).

All the interfaces, monitoring elements and configuration devices are managed by the SFPGA, while the Application FPGA has direct access to the FMCs and the RTM as well as to 2 SRAMs.

PCI

The PCI (Peripheral Component Interconnect) is a standard of PCI-SIG [2] (PCI Special Interest Group). PCI was originally developed at Intel in the 1990s. It went trough several revision and changes in the years. Its latest form is a serial link: PCIe (PCI Express).

PCIe is not a bus but a point to point link. The PCIe 1.0 can achieve a bandwidth of up to 250MB/s per lane, each lane consisting of two LVDS (Low Voltage Differential Swing) pairs, and each board can have up to 32 lanes.

PCIe is a very common standard for desktop computing and therefore many products can be found on the market as COTS in this format. PCIe boards can be plugged in standard and crate computers.

Figure 4: The PCIe FMC carrier developed at CERN.

Each PCIe board in a standard form factor can have up to 1 FMC available on the front panel.

Figure 4 is a picture of the PCIe FMC Carrier (PFC) developed at CERN in parallel to the VFC. It is a carrier for a FMC with an SFP for timing and data transfer on the front panel. It has 4 eSATA connectors on the back to implement custom board to board communication protocols.

The 2 carriers have been designed having in mind to share as much as possible in terms of architecture and components. This was done in order to give to the designers the possibility to have the seamless possible port of their application firmware from one carrier to the other.

VXS

VXS, VITA-41, is one of the answers of VITA (VMEbus International Trade Association) to the need of fast intercommunication between boards in the same crate.

The standard redefines the VME middle connector (P0) and assigns to it 16 differential pairs with a bandwidth of 10GHz. The protocol of those lines is defined in substandards with PCIe and Ethernet being the most common ones in commercial components. The standard foresees a system management based on IPMI, but this is just a recommendation.

A very strong point of the VXS standard is that old VME modules which do not use the P0, the most common option in COTS, can be plugged in VXS crates and work properly.

The network topology of the backplane is not defined in the standard and crates implementing it as star (Fig. 5) and mesh (Fig. 6) are both possible. The star topology, requiring a switch board, is the most common as the mesh requires too high densities of connections.

The standard has high potentiality but is not yet very popular in the high energy physics community. An FMC carrier for VXS crates is being developed by the radio frequency group of CERN, but is just one of a few designs.

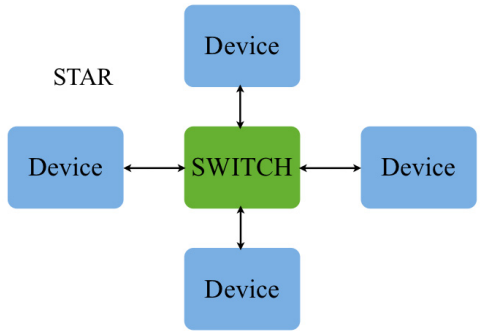

Figure 5: In a star configuration all the boards are connected to a switch board, usually plugged in the middle slot of the crate, via one or more lanes (couple of differential pairs). The switch than connects the boards that need to communicate between them in a dynamic way.

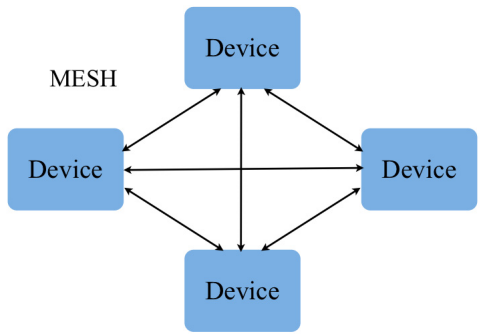

Figure 6: In a mesh configuration the boards are directly connected to each other. This reduces the latency but makes the backplane more complex. In some cases the boards could be connected in small groups to simplify the topology.

xTCA

xTCA is the collective name for ATCA (Advanced Telecommunication Computing Architecture), uTCA (Micro TCA) and MTCA.4 (Micro TCA for physics).

ATCA, PICMG 3.x, is a standard developed by the telecommunication industries for their specific needs: high backplane bandwidth and very high availability. The first target is reached thanks to the very high amount of Gbit lines each card could have: up to 200. The second with a very extensive use of system management based on IPMI for hot swap support and redundancy. Each board could use up to 200W, but available only from a -48V power supply, requiring DC/DC converters on board to obtain all the required voltages. Like in VXS neither the protocol of the differential pairs nor the backplane topology is defined in the standard. ATCA boards are in 8U format and can accept 8U rear transition modules (RTM).

The AMC (Advanced Mezzanine Card) was developed to increase the ATCA availability with the introduction of hot swappable mezzanines. The connector was specifically studied to allow an easy insertion and extraction from the

front of the crate without the need to unplug the carrier. As well as ATCA the AMC makes intensive use of the IPMI protocol. The mezzanines can self declare to the carrier at plug in time and inform the carrier when they are being removed. In this way all the required hardware and software steps to have a safe hot swap can be performed.

Figure 7: A uTCA board for a timing distribution system developed in a collaboration between the University of Stockholm and DESY.

An AMC mezzanine has 20 LVDS Gbit lanes (couple of differential pairs). The protocol of those lanes is not specified in the standard. Each AMC mezzanine is 180mm deep, but there are 6 form factors:

- Single (74mm) and double (149mm) width
- 13mm, 18mm or 28mm deep

The power in an AMC comes from a 12V supply. The allowed dissipation of a mezzanine depends on the form factor and can be at most 80W.

A single width AMC is about twice the size of an FMC, but is required to have a reasonably powerful FPGA on it as well as a few DC/DC converters, so that the real estate for the application specific logic is about the same.

The AMC mezzanines are also the basic element of the uTCA standard, in which the AMCs are directly plugged into a backplane. The standard doesn't specify the topology of the backplane, but the most common ones are the single and double star. Each crate require one, or two in case of double star topology, MCH (MicroTCA Controller and Hub), see Fig. 8. The MCH works as system manager and also as switch for the Gbit lanes between the boards. Users can connect to the MCH via ethernet and have access to the boards in this way.

Figure 8: A uTCA controller and HUB (MCH)

The uTCA standard is being evaluated at CERN by the xTCA interest group [7]. The interest group has reported some interoperability issues between boards from different manufacturers due to some interpretable part of the IPMI standard.

Figure 9: A uTCA crate. In the 1st slot there is the power supply, in the second the MCH and in the 3rd a crate PC.

The last standard that will be introduced in this paper is MTCA.4 (Micro TCA for physics). This standard is a derivate of uTCA that is still under ratification but has already been chosen for the XFEL control system at DESY.

MTCA.4 tries to reduce the freedom in the uTCA definitions to obtain a more standard product. In this optic it defines more strictly the connections assigning some as synchronization signals and strongly suggests to use PCIe as protocol for the Gbit lanes.

The MTCA.4 boards are defined as double width AMC and one more connector has been added on the top of the board to be used with a RTM (rear transition module).

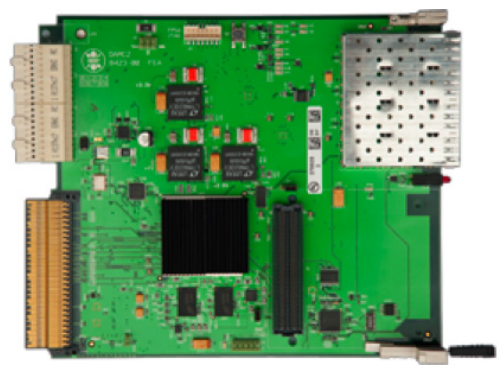

Figure 10: A MTCA .4 FMC carrier developed at DESY

An example of FMC carrier in MTCA.4 is shown in Fig. 10. This board is built around an FPGA that is connected to the LPC FMC, the rear transition module, a 128MB DDR2 memory and 4 SFPs accessible on the front panel. More details about the development ongoing at DESY for the XFEL control system are given in another paper from the same conference [8]

Table 1: Comparison Between the Various Standards

	VME	PCIe	VXS	uTCA	MTCA.4
FMC slots[1]	3	1	3	1-2	2
RTM	YES	NO	YES	NO	YES
System Bus speed	up to 320MB/s	-	up to 320MB/s	-	-
Gbit lanes	0	up to 32	8	20	20
Power available	108W	up to 75W	108W	up to 80W	80W
Hot-Swap	Partially implemented	NO	Partially implemented	YES	YES

[1]FMC mezzanines that could be placed on a carrier and be accessible on the front panel

LOOKING FOR REUSABILITY AND SYNERGIES

It is not possible to point to one standard as the optimal one. Which one suits best the system being developed depends on the specific needs but sometimes also on historical reasons: a group having invested in a specific technology will tend to reuse the same to have a common platform for its various systems. This doesn't mean that there cannot be synergies between groups: as the architecture of a DAQ is almost always the same it is possible that with minor changes the same board could be used by several institutes or groups. Sharing designs and opening them to external review and specification changes requests to fit a wider audience is exactly the purpose of the Open Hardware Repository (OHR) project, of which the VFC and PFC carrier are part.

The idea of OHR is that all the designs should be kept open and free to be used also by private companies. The OHR repository of a project is updated at each step, from specifications to production. Each developer willing to participate in the design or review phases can read and subscribe to the associated mailing lists giving inputs. The repository is also open to private companies willing to accept the terms of the OHR contract: each design shall be kept open and all the information made available. A private company can under the OHR contract, being prepared by the CERN legal office, produce and resell the boards in the repository.

Synergies and reusability can be improved not only at board level but also in FPGA firmware development. The use of a common internal bus, like the WishBone from OpenCores [9] as suggested in OHR, would allow to exchange FPGA blocks between designers, especially if the mezzanine standard used is the same.

ACKNOWLEDGEMENTS

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