REAL-TIME SAMPLING AND PROCESSING HARDWARE FOR BUNCH ARRIVAL TIME MONITORS AT FLASH AND XFEL

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Abstract

Bunch arrival time monitors installed in several locations at FLASH measure the arrival time of an electron bunch relative to an optical reference. The optical reference for the monitors is provided by the optical synchronization system based on a laser pulse train with a repetition rate of 216 MHz and a pulse duration of around 200 fs FWHM. This pulse train is distributed to the arrival time monitors by transit-time-stabilized fiber links with a stability better than 10 fs. The monitors encode the electron arrival time into an amplitude modulation of the laser pulse train. These laser pulse amplitudes need to be sampled and processed together with additional input parameters. Because the arrival time information is used in a feedback loop to adjust the accelerator fields, the signal processing, calibration and transmission of the bunch arrival time information via a low-latency, high-speed link to an accelerator RF control station is needed. The most challenging problems related to the signal processing are the synchronization of several clock domains, regeneration and conversion of optical laser pulses, online calibration, and exception handling.

INTRODUCTION

The principle of the bunch arrival time monitors (BAMs) used at FLASH is based on an electro-optical detection scheme, where the beam transient signal from a wide-bandwidth RF pick-up is used to modulate a laser pulse amplitude which is proportional to the arrival time deviation from its expected mean value. More details on the insights of the optical front-end of this monitor are discussed for example in [1].

Modulated and unmodulated laser pulses are sent via fibers to the sampling and processing hardware. An overview of the main functional blocks is shown in Fig. 1.

The following sections focus on major challenges involved in system design and commissioning of such a hardware and will give possible solutions and experiences.

OPTICAL TO ELECTRICAL SIGNAL CONVERSION

In order to process the encoded arrival time information coming from the optical front-end, the modulated optical pulses have to be converted into electrical signals. The common approach is to use a photo diode with additional components to interface the signals to the Analog to Digital Converter (ADC) input and the clock distribution unit.

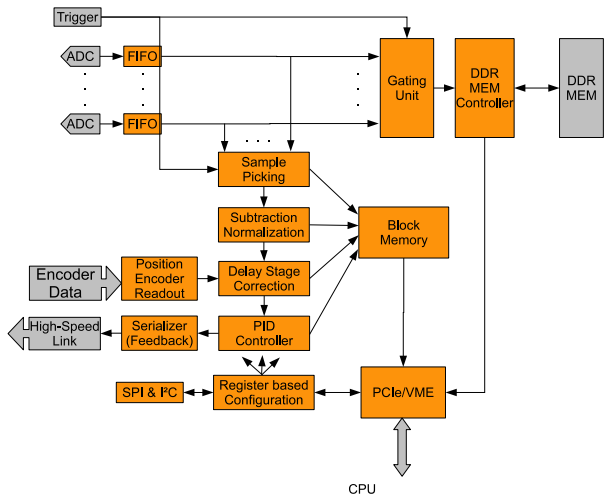

Figure 1: Block diagram of the internal processing and interfaces. The components shown in gray are hardware parts which are connected to the processing FPGA.

To calculate the arrival time, the baseline as well as the peak value of each modulated pulse is digitized. Due to limitations of the sampling rate of the ADCs, two channels are used, sample the baseline and peak separately. A splitter is, therefore, required to apply the same signal to two ADC inputs in parallel.

Due to the limited input bandwidth of the ADCs (700 MHz), low bandwidth photo diodes with a pig tailed fiber connector are used.

The first design included a gain block connected to the photo diode, a passive splitting of the signal and connection to the AC coupled input stage of the ADCs. However, the measurements showed, that the signal was distorted and differed completely in shape on the two ADC inputs. The most critical influencing factors turned out to be the connection between photo diode and gain block as well as the passive splitting and the transmission line to the ADC stage. Also the not optimally configured AC coupled ADC input influenced the signal on lower frequencies.

To improve the signals we changed the design in the following way:

- Reduction of the gain block influence on photo diode
- Decoupling of splitting and transmission line to ADCs with transistors
- Replacement of AC coupling ADC input stage (transformer) with capacitors

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The resulting ADC input signals measured with the ADCs by shifting the input clock step by step is shown in Fig. 2.

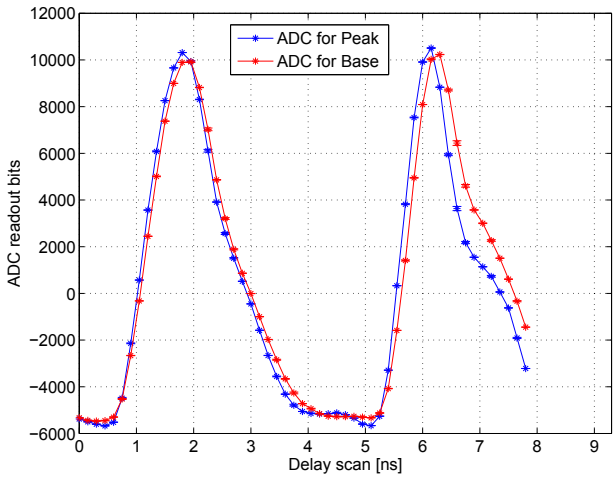

Figure 2: Measurement of the signal form at the ADC inputs. One ADC is used to sample the baseline and the other to sample the peak value.

Reducing the influence on the photo diode was achieved by reducing the energy transferred to the gain block and increasing the gain on the other side. After amplification the signal is split up and applied to a transistor stage to decouple the two paths and convert it to a differential signal. This is connected by a impedance matched transmission line and coupling capacitors to the input of the ADCs.

GENERATION AND DISTRIBUTION OF CLOCKS

The clock provided by the optical front-end has a repetition rate of 216 MHz. The maximum sampling frequency of the ADCs, however, is 130 MHz. Therefore it is only possible to sample every second pulse with one ADC while the baseline is sampled with the second ADC.

In order to provide the required ADC clock of 108 MHz a divider is used in the clock buffer chip available on the board. Dividing the clock introduces the uncertainty of two possible phases depending on the divider state in the beginning. This state, thus, defines which pulses are sampled and which are skipped, defining whether the correct pulses are sampled. Therefore the correct phase needs to be ensured by the system. This is achieved by synchronizing the divider with the trigger provided by the timing system and is discussed in more detail in the following section.

The most important drawback of this approach is, that the clock is not available for a short time during synchronization. This results into discontinuities in the processing in the FPGA and needs resynchronization also at that point.

Besides dividing the clock, also phase shifting of each ADC clock is important to sample the correct point of the signal form (peak or baseline (see also Fig. 2)). This is achieved by adjustable delay elements in the clock buffer chips. More details on this delay adjustment can be found in [2].

Finally the clocks are distributed to the four ADCs and the FPGA. It should be noted, that the FPGA clock is also divided to 108 MHz used for processing, but it is not affected by the synchronization of the divider and thus is available in the FPGA all the time.

ALIGNMENT OF CLOCKS AND TRIGGER

A major difficulty in the current setup of the system is the alignment of the clocks of the ADCs and FPGA to the trigger provided by the timing system.

The timing system produces a trigger synchronized to the machine on each macro pulse used to start sampling. A stable relationship of trigger, ADC and internal processing clocks ensures, that the sample point number always identifies the same modulated pulse. The other way round, if the alignment of both is changing, the sample point number is changing, which results in jumps of the waveform back and forth (i.e. left or right in the plot). This is critical, as the sample point number is used to define the modulated pulses in the memory for processing later on.

Unfortunately, the alignment is not fixed due to the system design. The clock for the ADCs and processing is provided by the synchronization system and shifted in phase in the optical BAM front-end. The trigger however, is generated based on the master oscillator and not shifted in phase. Additionally it has a timing jitter of about 1ns which is around 10% to 20% of the clock period. During operation it is always possible and also likely, that one clock edge passes the trigger edge, which results in undesired ambigiuties.

A complete solution for this problem has not been implemented by now. However, a promising approach is to detect the phase relationship between trigger and clock and shift the clock phases in the FPGA to establish the highest temporal distance between them. Additionally it has to be remembered, if an edge had been crossed, the whole sampling has to be delayed or sped up by one sample point. This would resolve instabilities due to jitter of the trigger around the clock edge within the FPGA.

To solve the trigger problem for the external clock divider, the only way is to generate a trigger shiftable in time in the FPGA. This is not an easy task, as no clock is available right now, which could be used for shifting the trigger.

MERGING OF DIFFERENT CLOCK DOMAINS

All four ADCs as well as the FPGA run with the same clock, but could have different phase relationships. To process the sampled data within the FPGA it needs to be merged to the same clock domain. This could be done by two approaches:

- Using FIFOs[1] with different input and the same output clocks
- Detecting and shifting the data in the right clock domain

Using a standard FIFO the sampled data could be clocked in with its own clock and taken out by the processing clock. Disadvantages for this solution is the need for four additional global clocks and most likely DCMs[2] within the FPGA as well as a latency introduced by the configuration of the FIFO. The second way is to follow a proposal given by the manufacturer of the used FPGA [3]. It uses just one DCM and detects the best clock phase to use to latch the sampled data into the FPGA for each ADC. Additionally it shifts the data to the correct phase of the processing clock and removes meta stabilities of flip flops. Main disadvantages are increased space and timing requirements.

INTRA BUNCH FEEDBACK PROCESSING

Besides the monitoring functionality and external pulse-to-pulse beam based feedbacks, an intra bunch-train feedback is implemented in the design as shown in the block diagram in Fig. 1.

The first step is to select the sample points of both the modulated pulses and one pulse before each modulated pulse.

Peak and baseline for each of those pulses are subtracted in order to calculate the real amplitude. Then the real amplitude of the modulated pulse is normalized to its preceding pulse to normalize the amplitude. This value is proportional to the bunch arrival time deviation from its expected mean value and could be used in principle for feedbacks.

However, before applying a feedback controller, the influence of the optical delay stage in the optical front-end must be removed. This is crucial to be independent of motor movements while measuring and processing data from the monitor. This also includes movements due to calibration (see also [2]).

To enable this an online and synchronized readout of the absolute position encoder attached to the optical delay stage is required, as well as additional external calibration parameters. This part is currently under development and will be included in the near future.

Finally, a common PID Controller[3] is used to control the output signal, which is then serialized and transmitted via a high speed serial link to the corresponding accelerator module controller. A more detailed description of the feedback structure could be found in [2] and [4].

HARDWARE PLATFORMS

The current implementation of the hardware for FLASH is a VME based digital carrier module with a Xilinx Virtex 2 Pro FPGA called Advanced Carrier Board (ACB). Connected to that board is a module with four 16 bit 130 MHz ADCs with optical to electrical signal conversion.

In the future and for XFEL a transition to μTCA[4] is currently under development. In this case the xTCA for Physics extensions will be used. It will consist of a front module (AMC[5]) providing processing and most likely analog to digital conversion and a rear transition module (RTM) implementing the optical to electrical signal conversion and conditioning.

CONCLUSION AND OUTLOOK

It has been shown, that a hardware to process information provided by the optical front-end of a bunch arrival time monitor faces different problems like clock generation and distribution, merging of clock domains and aligning with a trigger. Possible solutions and current implementations have been described and also intra bunch train feedback processing was discussed.

It should be emphasized, that this is not an easy task, which could be done with all standard ADC hardware available on the market. Instead it needs special hardware or hardware additions in order to allow precise measurement and real time processing.

ACKNOWLEDGMENTS

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REFERENCES

[1] M.K. Bock et al., “Recent Developments of the Bunch Arrival Time Monitor with Femtosecond Resolution at FLASH”, WEOCMH02, IPAC2010, Kyoto, Japan, May 2010

[2] P. Gessler et al., “Longitudinal Bunch Arrival Time Feedback at FLASH”, THPA04, FEL2010, Malmö, Sweden, August 2010

[3] Xilinx, Application Note 225, `http://www.xilinx.com/support/documentation/application_notes/xapp225.pdf`

[4] W. Koprek et al., “Intra-train Longitudinal Feedback for Beam Stabilization at FLASH”, THOAI2, FEL2010, Malmö, Sweden, August 2010

[1] First In First Out
[2] Digital Clock Managers
[3] Proportional, Integral and Differential Gain Controller
[4] Micro Telecom Computing Architecture
[5] Advanced Mezzanine Card