COMMISSIONING OF THE LOW-CHARGE RESONANT STRIPLINE BPM SYSTEM FOR THE SWISSFEL TEST INJECTOR

B. Keil, A. Citterio, M. Dehler, R. Ditter, V. Schlott, L. Schulz, D.M. Treyer
(PSI, Villigen, Switzerland)

Abstract

This paper introduces the architecture and first beam commissioning results of the standard BPM system for the SwissFEL test injector [1], a 250MeV linac that is progressively being commissioned in order to perform R&D for the "SwissFEL" 5.8GeV hard-X-ray FEL facility proposed at PSI [2]. Since the SwissFEL has a nominal bunch charge range of 10-200pC, the test injector is equipped with 500MHz resonant stripline BPMs that are optimized for high dynamic range and sensitivity, to support machine operation well below 10pC. Beam tests with a 5 GSa/s direct sampling electronics designed at PSI showed a single-bunch resolution of <20μm RMS at 2pC and typically 7μm RMS for charges >10pC. The BPMs also measure bunch charge, insensitively to dark current, with <30fC RMS resolution at 2pC.

INTRODUCTION

SwissFEL Test Injector

The SwissFEL test injector [1] has a length of ~60 m, with a laser-driven S-band RF gun and normally conducting S-band accelerating structures. The injector is presently being progressively installed and commissioned, using single bunches of 10-200 pC at 10 Hz repetition rate. The SwissFEL [2] will finally be operated at 100Hz, supporting a 2-bunch mode with ~50 ns bunch spacing, and parallel operation of a hard X-ray and a soft X-ray undulator beamline using a fast beam distribution system.

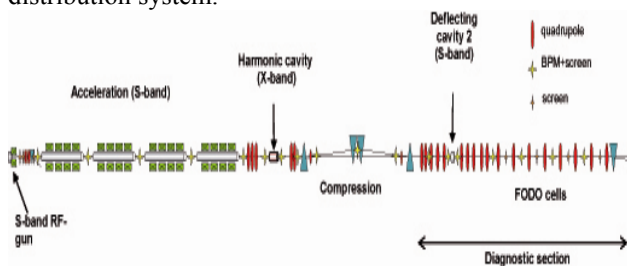Figure 1: SwissFEL test injector.

SwissFEL BPM Requirements

In the SwissFEL undulator intersections, with ~8mm inner beam pipe diameter, the baseline design presently foresees BPMs with ~1μm (σ/10) RMS resolution and drift at 10-200pC. These comparatively demanding specifications are driven by beam based alignment and trajectory stabilization requirements. The BPM and trajectory alignment requirements in the S-band injector (38mm inner beam pipe diameter) and C-band main linac (16mm inner pipe diameter) are more relaxed, due to larger beam size and uncritical orbit-related emittance

dilution tolerances [3]. Here the target single-bunch BPM resolution is <10μm RMS for the injector and <5μm RMS for the main linac at 10-200pC.

Technology Considerations

The SwissFEL baseline design foresees dual-resonator cavity BPMs with mode-suppressing couplers in the undulators [2]. They will be based on the European XFEL (E-XFEL) undulator BPMs that are presently being developed by a collaboration of PSI and DESY as in-kind contributions to the E-XFEL [4]. Since the cavity BPM mechanics and electronics are still under development, we decided to equip the SwissFEL test injector with a BPM system based on already existing PSI technology.

TEST INJECTOR BPM SYSTEM OVERVIEW

Modular System Architecture

The 500MHz resonant stripline BPM pickups used in the SwissFEL test injector [5] are an optimized version of a design that was developed for and installed in the SLS linac and transfer lines. The 500 MHz decaying sinusoidal signals of the test injector stripline pickups are amplified and filtered by a low-noise RF front-end (RFFE) board that was newly developed at PSI in a VME64x form factor to support beam charges down to 10 pC.
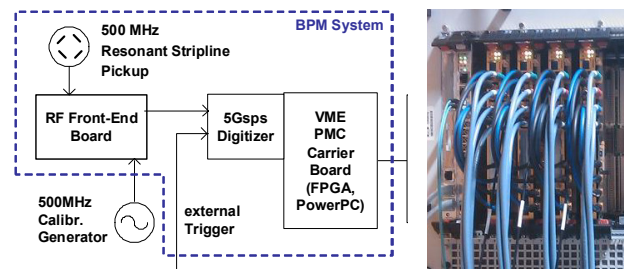

Figure 2: Left: BPM system block schematics. Right: VME crate with EPICS IOC, timing board, and four stripline BPM electronics.

The 500 MHz RFFE output signals are digitized by a PMC mezzanine module that uses a cost-efficient 5 GSa/s waveform digitizer chip (DRS4 domino ring sampler) also developed at PSI [6]. Tests with an early prototype PMC in 2008 using the predecessor of the DRS4 chip showed that a BPM system based on this digitizer type is feasible [7]. The digitizer waveforms are processed by an generic FPGA PMC carrier VME64x board ("VPC board") that has found widespread use at PSI, e.g. for digital proton BPMs [8]. The re-use of pickup concept,

electronics and FPGA firmware allowed a time, cost and man power efficient development of the SwissFEL injector BPM system.

RESONANT STRIPLINE PICKUPS

The pickups of the test injector consist of four λ/4 stripline resonators that are located parallel to the electron beam alongside the inner beam pipe wall, with 90° axial rotation symmetry. The resonators are excited at the gap at the open-circuit end, and the signal is extracted by direct tapping near the short-circuit end. The four beam-induced pickup signals consist of a superposition of decaying sinusoids, having frequencies around the fundamental resonance (500MHz) and odd order harmonics. The fundamental resonance that we use has four associated modes, each of them having its distinct electrode voltage pattern: A monopole mode (all voltages in-phase) with magnitude proportional to the bunch charge, two dipole modes (one mode per plane with voltages from opposite electrodes 180° out-of-phase) proportional to the horizontal (X) and vertical (Y) beam positions times the bunch charge, and a quadrupole mode. Depending on the mechanical design, the modes usually have a frequency separation up to a few percent.
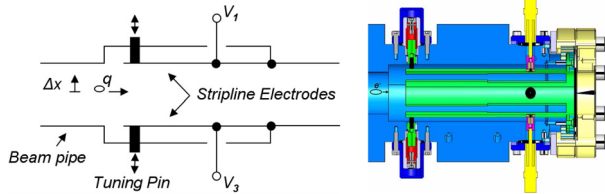

Figure 3: Resonant stripline pickup schematics (left) and construction drawing (right).

The pickup design for the SwissFEL is based on the SLS linac design, but was improved in several ways [5]. By changing the strip geometry (e.g. the width along the strip), the monopole and dipole mode frequencies were made nearly identical (500 MHz, with 0.4 MHz mode spacing), and the loaded Q for monopole and dipole is also very similar (6.2 and 7.6), which simplifies analog and digital signal processing. Furthermore, a ceramic tuning screw for each strip allows adjusting the radial positions of the open strip ends and thus the resonance frequency of each strip very precisely and efficiently. Each of the 25 manufactured pickups has been individually tuned using a network analyzer, prior to installation.

STRIPLINE BPM ELECTRONICS

RF Front-End

Each of the 4 symmetric input channels of the 500MHz resonant stripline RFFE consists of an input low-pass filter, followed by a programmable attenuator (31.5dB range, 0.5dB steps), a fixed gain amplifier, a 500MHz narrow band-pass filter in stripline PCB technology, an output amplifier, and a wide 500MHz output band-pass. Furthermore, an external reference input or the signal of

an on-board 500MHz oscillator can be multiplexed onto the four inputs for calibration purposes. To minimize the impact of digitizer jitter on the position resolution, the first band-pass filter stretches the 500MHz pickup signals. The 3-dB width of the envelope is stretched from 3 to 29 ns. This filter also suppresses the strong 1.5 GHz pickup harmonics.

5 GSa/s Digitizer Mezzanine

The four RFFE output signals are digitized by a PMC mezzanine module that is plugged onto the FPGA carrier board. Each of the four PMC input channels consists of a programmable attenuator (31.5dB range, 0.5dB steps), an amplifier, and a wide 500MHz band-pass (to suppress out-of-band noise). Each of the four input signals then passes a two-way splitter that is followed by two balancing transformers, and is fed to two independent DRS4 sampler chips. Processing each pickup signal by two independently operating samplers and digitizers allows improving the position resolution by about sqrt(2) at higher beam charges, where the resolution is dominated by sampling jitter of the DRS4.

The DRS4 chip consists of a cyclic analog waveform buffer with 1024 sample & hold (S&H) stages per channel. The S&H switches are activated by a so-called domino wave which is a pulse circulating on a cyclic chain of inverters (two per S&H cell), where the signal is tapped every two inverters to open/close the S&H switch of its adjacent sampling capacitor. By regulating the analog supply voltage of the inverter chain, the sampling rate for the DRS4 chip can be varied between 200 MSa/s and >5 GSa/s. The DRS chip allows to measure the DRS wave revolution frequency and thus the sample rate, which we digitally regulate to 5 GSa/s by a DAC connected to the FPGA on the VPC.

After storing of the analog waveforms in the S&H cells of the DRS4 chips, each of the 1024 cells per channel is read out by consecutively multiplexing the S&H capacitor voltage of every cell to a slow but accurate analog-to-digital converter. The read out rate is 33 MSa/s. The ADC has two channels (on per DRS chip), a resolution of 14 bits, and is also located on the PMC.

External Trigger Requirements

The sampling (i.e. the domino wave in the DRS4 chip) is started by an external trigger from the injector timing system and stopped by the FPGA. Due to the sampling window size of ~200ns, even some 10ns jitter of the external trigger (generated by the injector timing system) relative to the electron bunch are acceptable. Moreover, in contrast to other signal detection/processing schemes, no external reference clock is needed. Thanks to the very high oversampling rate, the signal amplitudes can be estimated reasonably accurate by digital post-processing.

DIGITAL SIGNAL PROCESSING

The ADC data is read by the FPGA on the VPC board that first performs an individual gain, offset, and sampling

interval correction for each single S&H stage in the DRS4 chips. The DRS4 chip samples at non-equidistant intervals, nominally 200ps, but with tens of picoseconds variations from cell to cell. These sampling interval variations are mainly reproducible [7], therefore they are measured in the lab along with the gain and offset errors by an automatic calibration system, and stored in an EEPROM on the PMC. An algorithm in the FPGA on the VPC board then converts the non-equidistantly sampled pickup signal waveforms to equidistantly sampled waveforms using a spline interpolation algorithm.

The resulting 500MHz waveform is digitally FIR-band-pass filtered in the FPGA. Then the signal envelope is calculated using a Hilbert transform FIR filter for complex signal reconstruction and Cartesian-to-polar-conversion, followed by another FIR filter to low-pass the amplitude waveforms and thus obtain the envelopes of the RFFE output signals. The FPGA then automatically chooses the part of the 1024-sample waveforms to be used for the calculation of the beam position (presently a window of 200 samples) by detecting the envelope peaks. The horizontal (X) and vertical (Y) beam positions are then calculated individually for each sample via

$$X = k \, ((B+C)-(A+D)) \, / \, (A+B+C+D)$$
$$Y = k \, ((A+B)-(C+D)) \, / \, (A+B+C+D)$$

with k=16.2mm (predicted theoretically and verified experimentally with beam) and averaged over the 200 values. A, B, C and D are the signal amplitudes of the top left/right and bottom right/left strips. The FPGA also supports an alternative position calculation mode where the amplitudes are integrated before calculating the position, with very similar position noise for both modes.

FIRST MEASUREMENT RESULTS

Position Resolution

The test injector presently has 17 resonant stripline BPMs installed that were recently commissioned with beam. The RMS position resolution of the stripline BPM system is dominated by electronics noise and was measured by two methods: a) by correlating the BPM data of three adjacent BPMs with only a drift section between them, assuming they have the same resolution, and b) by measuring the RMS noise of

$$Z = k \, ((A+C)-(B+D)) \, / \, (A+B+C+D)$$

Z is independent of the beam position (in first order, for a sufficiently centred beam) but should have the same electronics-induced noise as the beam positions X and Y, provided that the noise of the four BPM electronics channels is uncorrelated.

By using method a), we obtained 6.3μm RMS horizontal and 7.9μm RMS vertical single-bunch resolution for three adjacent BPMs (see Fig. 4, left plot), using BPM data taken at 10Hz during ~3 minutes while the beam charge was varying between 80 and 90pC.

Method b) gave 7.4μm RMS for the same BPM, with typical values for other BPMs around 7μm RMS ± 20%.
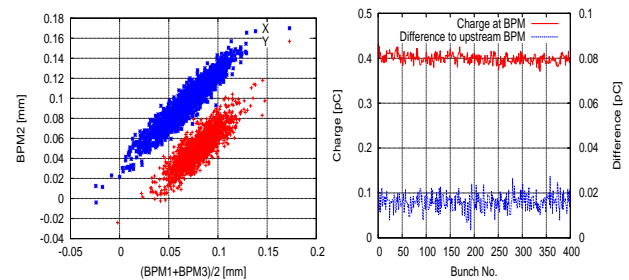

Figure 4: Left: Measured position at BPM2 vs. predicted position using linearly interpolated readings of adjacent BPMs. Right: Charge measurement at 0.4pC.

Measurements at other beam charges show that the resolution is ~7μm RMS for charges >10pC, independently of the bunch charge, where the attenuator settings were automatically adjusted to the respective charge by a digital feedback loop. The charge-independence of the resolution at higher beam charges is expected since the position noise in this charge range is dominated by the digitizer quantisation noise, i.e. by DRS4 chip sampling jitter.

At very low bunch charge <1pC, the BPM noise is dominated by thermal electronics noise, with the product of charge and single bunch RMS position noise being ~30μm • pC (e.g. 60μm RMS at 0.5pC), with less than 10% variation of this value over a larger number of BPMs used for this measurement.

Transverse Beam Jitter

Since the test injector and its BPM system were just recently put into operation, systematic studies of beam jitter sources still have to be performed. The smallest jitter was measured at the BPM downstream of the first S-band RF structure, with BPM readings of 9μm X RMS and 8.4μm Y RMS for data taken over three minutes at 85pC with ~10% charge variations. These RMS figures contain both BPM electronics noise and real beam motion. Provided they are uncorrelated, an assumed electronics noise of ~7μm would imply ~5μm real beam motion at this BPM. Other downstream BPMs showed larger beam movements above 10μm RMS. This is expected due to the larger beam size at these BPMs. Simultaneous measurements of beam size and position jitter via screen monitors that are integrated in the stripline BPM pickup bodies still have to be performed. Since many beam parameters and subsystems have not yet been tuned and corrected, and no active feedbacks are used so far in the test injector, the measured beam jitter values are promising for the first days of operation though not representative for the final SwissFEL performance.

Bunch Charge Measurement

The bunch charge at the injector BPMs is continuously calculated (and used e.g. for charge transmission optimization) using the sum of the measured strip signal amplitudes, with theoretical correction factors for the attenuator settings. The absolute charge is calibrated for all injector BPMs using a wall current monitor.

The BPMs integrate only over a period of 40ns and are only sensitive to the 500MHz spectral component of the beam. Since the dark current is bunched at the 3GHz main RF frequency, the BPMs are rather insensitive to dark current and thus well suited to measure the actual laser-induced bunch charge, even for very low charges. Down to charges of 2pC, the relative charge resolution is <1.5% RMS, with an absolute resolution limit of ~10fC for charges <<1pC (see Fig. 4, right plot, showing the charge difference measured between adjacent BPMs at ~0.4pC).

IMPROVEMENT OPTIONS

Use of 180° Hybrids

While we are presently digitizing the signal of each strip directly and calculate the difference-over-sum to determine the beam position digitally, we could also use an external 500 MHz 180° hybrid in front of the RFFE to generate the difference (proportional to beam position times charge) and sum (proportional to beam charge) signals of opposite strips. The RFFE and PMC gains can be programmed individually for each channel, thus sum and difference signals could have different gains G_Σ and G_Δ. For $G_\Delta > G_\Sigma$ the factor k would be reduced, resulting in improved position resolution. Ideally, the resolution improvement factor is G_Δ/G_Σ at higher beam charges, where the resolution is currently limited by sampling jitter. This comes at the expense of a reduction of the dynamic position range (now >20mm peak-to-peak) by the same factor, ideally with a fixed resolution-to-range ratio of presently ~0.035% for higher beam charges.

Since the resolution of stripline BPMs improves with decreasing beam pipe diameter, the use of hybrids should in principle allow for resonant stripline based BPMs that are capable of achieving sub-micron resolution.

DRS4 Chip Calibration

The gain and offset errors of the DRS4 chip S&H stages are presently measured using DC signals. Variations in the hold capacitor sizes that cause the gain for DC and 500 MHz AC signals to be different are thus ignored, which introduces additional noise on the sampled signal waveforms. This noise could be reduced by applying a suitable calibration of S&H gains. The 500 MHz calibration signal of the RFFE on-board oscillator could not only be used to determine the sampling time intervals, but also for AC gain error measurement and calibration of each S&H stage.

Temperature Drift Compensation

The RFFE on-board oscillator would also allow to measure and correct relative gain drifts of the four input signal channels of the BPM electronics, in order to reduce related drifts of the beam position readings. Such drifts could be corrected either by measuring the gains continuously in between bunches, or by measuring them once as a function of the electronics temperature and applying a feed-forward correction in the FPGA that can

read PMC and RFFE temperatures via on-board sensors with 0.03°C resolution.

SUMMARY AND OUTLOOK

The choice of resonant stripline BPMs allowed a cost and man power effective development and commissioning of the SwissFEL test injector BPM system. Over the nominal SwissFEL charge range of 10-200pC, a single-bunch position resolution of 7μm RMS was achieved, which is 0.018% of the beam pipe aperture and ~0.035% of the peak-to-peak position range of >20mm. At charges <<1pC, the position resolution is ~30μm · $(Q[pC])^{-1}$. The charge resolution is <1.5% at 2-200pC, with a resolution limit of ~10fC for very low bunch charges. The measured transverse beam motion is ~5μm RMS behind the first S-band accelerating structure and >10μm for the BPMs downstream.

In Q4 2010, four cavity BPMs will be installed in a BPM test section at the end of the SwissFEL test injector for SwissFEL / E-XFEL undulator BPM R&D, with two of the BPM pickups on motorized 2D movers. A recently developed corresponding BPM electronics achieved sub-micron resolution [4]. This BPM test section will also be perfectly suited to characterize the injector stripline BPMs in more detail, e.g. to measure and if necessary calibrate gain, offset and linearity for different attenuator settings and bunch charges, as well as to test the use of hybrids.

ACKNOWLEDGEMENTS

REFERENCES

[1] M. Pedrozzi at al, *"250 MeV Injector Concept Report. Accelerator Test Facility for SwissFEL"*, PSI Report 10-05.

[2] R. Ganter et al, *"SwissFEL Conceptual Design Report"*, PSI Report 10-04.

[3] M. Aiba et al., *"Study of Beam-Based Alignment and Feedback for SwissFEL"*, these proceedings.

[4] B. Keil et al., *"The European XFEL Beam Position Monitor System"*, Proc. IPAC'10, Kyoto, Japan, 2010.

[5] A. Citterio et al., *"Design of a Resonant Stripline Beam Position Pickup for the 250MeV PSI XFEL Test Injector"*, Proc. DIPAC'09, Basel, Switzerland, 2009.

[6] S. Ritt, *"The DRS chip: Cheap waveform digitizing in the GHz range"*, NIM A518 (2004): P. 470-471.

[7] B. Keil et al., *"Application of a 5 GSPS Analogue Ring Sampling Chip for Low-cost Single-shot BPM Systems"*, Proc. EPAC'08, Genoa, Italy, 2008.

[8] B. Keil et al., *"Commissioning of a New Digital BPM System for the PSI Proton Accelerators"*, Proc. EPAC'06, Edinburgh, UK, 2006.