A STRIPLINE KICKER DRIVER FOR THE NEXT GENERATION LIGHT SOURCE*

Fred Niell, Dr. Neal Butler, Dr. Marcel P.J. Gaudreau, PE, Michael Kempkes,
Diversified Technologies, Inc., Bedford, MA 01730, USA

Abstract

Diversified Technologies, Inc. (DTI) has designed, built, and demonstrated a prototype stripline kicker driver capable of less than 10 ns rise and fall time, ~40 ns pulse length, and peak power greater than 1.7 MW/pulse.

INTRODUCTION

Diversified Technologies, Inc. (DTI), under an SBIR grant from the U.S. Department of Energy, assembled a prototype pulse generator capable of meeting the original specifications for the Next Generation Light Source (NGLS) fast deflector. The ultimate NGLS kicker driver must drive a 50 © load (a 50 © terminated Transverse Electromagnetic (TEM) deflector blade) at 10 kV, with flat-topped pulses according to the NGLS pulsing protocol and a sustained repetition rate of 100 kHz. Additional requirements of the specification include a 2 ns rise time (10 to 90%), a highly repeatable flattop with pulse width from 5 – 40 ns, and a fall time (90% to .01%) less than 1 μs. The driver must also effectively absorb high-order mode signals emerging from the deflector itself.

STRIPLINE KICKER DRIVERS

The ultimate size, and hence cost, of any damping ring strongly depends on the speed of the kickers. It is envisioned that a scintilla of deflection will be imparted by a symmetric pair of shaped parallel deflection blades, pulsed in opposition at 10 kV. Within the guide, comprised of the two deflector blades and their environment, each TEM wave produced by the two pulse generators traverses the guide synchronously with the selected (relativistic) charge packet. Various system designs were explored for producing the desired pulse wave forms. The options included a direct series high voltage switch, solid-state Marx bank, inductive adder, or more conventional pulse transformers and transmission-line adders, several of which were considered in detail. The inductive adder was ultimately selected as the preferred development path for the remainder of the program.

The DTI team has designed and demonstrated the key elements of a solid-state kicker driver capable of meeting the NGLS requirements, with possible extension to a wide range of fast-pulse applications. The current iteration employs compensated-silicon MOSFETs with a charge-pump gate drive arrangement (Figure 1). Two of these transistor-gate driver modules are used to drive opposite ends of the primary winding of an inductive adder transformer in a Marx-derived topology, achieving 1 kV per stage with transistors rated for 650 V. The high voltage gate-drive technique speeds up switching by quickly charging the power transistor gate capacitance in spite of significant internal gate resistance and package inductance. This can be considered a Marx generator-type circuit because two capacitors are charged from the prime power in parallel and discharged in series.

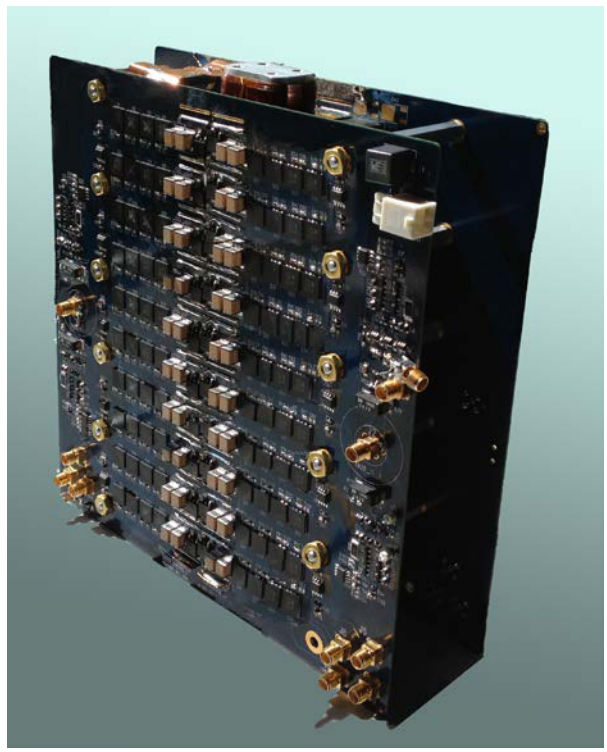

Figure 1: The dual-board pulser, displaying top and bottom boards with central output busbar.

HYBRID MARX-INDUCTIVE ADDER

The inductive adder functions by applying several separately-powered primary circuits, each with its own ferrite coupling transformer core, to a single shared secondary circuit. In this manner, the voltages of all the primaries add together, creating one large output pulse. The output pulse voltage is simply the applied voltage, minus any forward drop in the switching circuitry, across the "T" model of the output transformer. The current

*Work supported by U.S. Department of Energy SBIR Award DE-SC0004255

ISBN 978-3-95450-133-5

through the magnetizing inductance is chosen to be very small compared to the main pulse current, perhaps 1/100th of the main pulse current. This way, the clamp diodes across the primaries are not dissipating too much power on each pulse. The transformer leakage inductances then primarily set the rise and fall time of the system. Currently, no efforts have been made to optimize the primary-referred secondary inductances as 7-10 nH was achieved with simple methods.

In Figure 2, the green line shows the flow of current during the "charging" phase. The capacitors C1 - C n are charged through the resistors to the nominal 500 V bus voltage. The blue line shows the flow of current during the "on" state of the transistors. The various blocking inductances and snubber diodes are not shown in the interest of clarity.

RESULTS

The fully populated (dual-board) pulser with low inductance output structure is shown in Figure 1, while Figure 3 displays pulser performance. Note the arrangement of both sides to drive the common output busbar. The busbar was designed to fit snugly inside the core structure with enough clearance for 6 layers of 0.005" Kapton sheet as insulation. The bar was rounded on the edges to relieve electrical stress on the insulation, but the radius was simply 1/8" instead of an actual Rogowski profile. The output was terminated into 100 ohms (two Bourns 50-ohm RF terminator resistors), with two boards operating in bipolar mode (+/-2.5 kV). Future designs will incorporate some impedance control on the secondary winding.

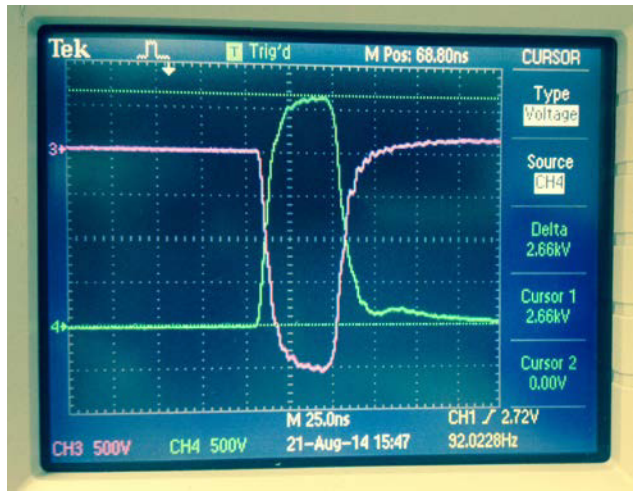

Figure 3: Output of two boards into 100 ohms operating in bipolar mode. 5 kV (+/- 2.5 kV), 5 ns 10 – 90% risetime, 25 ns pulsewidth.

FUTURE EFFORTS

Within the remainder of the project, effort level will remain high, as the initial challenge of circuit selection and demonstration is over. The hardware to test our theories has been built and proven to the 1 MW level. Testing of the hardware will continue, comparing the results with the initial PSPICE simulations and extending to 2 MW/pulse. Changes will be made to improve rise time and fall time by altering the physical form of the secondary windings and materials of the coupling transformers. Cooling options will be studied, and appropriate adjustments will be made to the design in order to complete a lab-bench prototype of the pulser that will support full voltage and current at the required PRF cooling.

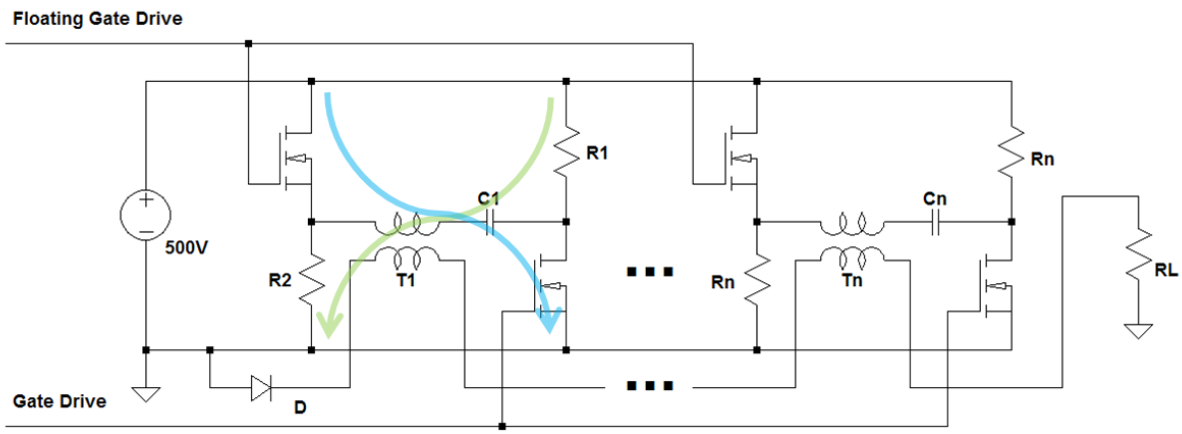

Figure 2: Electrical schematic of two stages showing main pulse current path in blue and charging current path in green. The floating gate drive is referenced to the source leads of the "flying" transistors. For clarity, snubbers and clamp diodes are not shown.

ISBN 978-3-95450-133-5