# THE DESIGN OF LOW NOISE MAGNET POWER SUPPLY*

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*Abstract*

The accelerator facility needs a high stable magnet power supply (MPS). The stability requirements of the some MPSs in accelerator facility were in the range of the ~10 ppm. There are many noise sources which affect the stability of the MPS. Thus the design of the MPS requests much attention on the noise reduction scheme from the design stage. The noise on the MPS divided into some sources such as the ripple voltage coming from rectifier on the DC link, switching noise from the high voltage switch, and so on. This paper dealt the ripple components analysis, oversampling converter and digital voltmeter for the high precision stability measurement.

## INTRODUCTION

The stability of the magnet power supply (MPS) was related to the noise components generated by MPS itself. The sources to give the poor output stability of the MPS were divided into two types as ripple components and switching noise. The ripple components came from rectifier which inevitably generated by the harmonic components of the line frequency such as 60Hz, 120Hz and so on. And the other noises were developed at inter PCBs or cables between modules due to parasitic inductance and capacitance on fast rising and falling time of the pulse when switching state. The proper signal processing in digital and analogue to increase signal to noise ratio was needed to the high stability MPS.

This paper describes some design schemes that was implemented into the MPS were described such as ripple voltage analysis, and oversampling converter for high resolution. And this paper shows the working process of the dual slop integrator for analogue to digital converter (ADC). And the aperture time of the DVM3458A affects the measurement precision in the ~ppm range.

## REDUCTION LINK VOLTAGE RIPPLE

The full wave rectifier of three-phase AC input of wye or delta-connection or both of them was composed for the DC link voltage of the MPS. The Fourier series expansion of the link voltage in the case of full wave rectifier of three phase AC line is given as the following equation

$$V_{link} = \frac{3\sqrt{3}}{\pi} V_m \left(1 - \sum_{k=1}^{\infty} \frac{2}{36k^2} \cos(6k\omega t)\right).$$

The spectrum of the $V_{link}$ contains sixth multipole components of the line frequency. It is corresponded to 360 Hz in the case of the 60 Hz AC input. The switching frequency of 25 KHz of the MPS was much higher than the multipole components of 360 Hz, thus it was acted as sampling frequency while it satisfied the Nyquist sampling theorem as the following equation [1].

$$F_s \geq 2F_c,$$

where $F_s$ is the sampling frequency and $F_c$ is the highest frequency in the signal.

The FETs worked as analogue switch devices in the sampling process. The cut-off frequency of the output filter of the MPS was located around ~KHz, thus the rectified ripple components passed without any attenuation. Figure 1 showed the simulation results of the PSPICE for a three phase full rectifier. The ripple components of the link voltage were appeared at the output stage with 0.5 $V_{pp}$, which affected to the output stability about 10 $mA_{pp}$ fluctuation with same frequency.

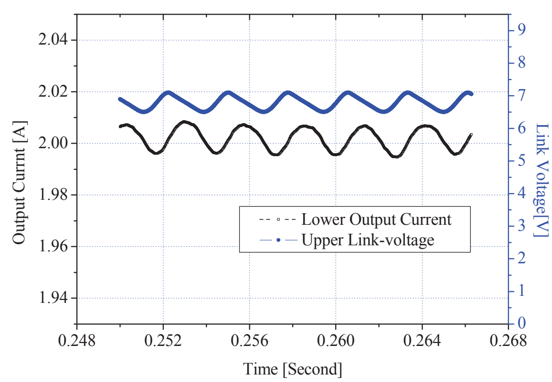


Figure 1: Ripple components on the output stage.

To reduce this effect of the ripple components, a proper low-pass filter should be configured into the input rectifier. The parallel damped filter was preferred to building the MPS as described in Ref. [2]. The cut-off frequency of the filter should be ranged ~10 Hz, that was dependent on the required stability.

## OVERSAMOLING CONVERSION

Oversampling method represents that the ADC converts analogue signal into digital with a higher sampling rate than the required bandwidth of interest. This method combined with suitable digital signal processing like average and decimation is able to improve signal-to-noise ratio (SNR). With the improved SNR the effective bit resolution of ADC will be increased [3].

The MPS is designed by the switching mode thus it cannot be avoided switching noise generated during the switch transition. Furthermore, there are many other noise

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sources in MPS introduced from DSP itself, induced noise voltage by the high current fluctuation, common mode noise from AC line, and etc.

All of these noises made the design of the high stable MPS difficult. Thus it was necessary to design hardware circuits in depth and to adapt suitable signal processing. The required current stability of the MPS was less than 10ppm. This means that the resolution of ADC for feedback control has to have higher than 17-bit.The switching frequency of the power converter of the MPS was 25 KHz. The ADC AD977 from the Analog Devices was adapted for the MPS which was specified 16-bit resolution, 200 KHz throughput, internal reference, etc. Two ADCs continuously sampled the output current with the same start of conversion clock of 200KHz.These sampled data were averaged and decimated in the field programmable gate array(FPGA) SPARTAN 3 comes from Xilinx Co. Whenever DSP requested the ADC data, FPGA sent them to DSP through SPI, which were calculated just before process. The DSP and FPGA were always synchronized by the time sharing access to the given clock period, thus there were no chance to loss the ADC data. Figure 2 showed the oversampling scheme applied into MPS.

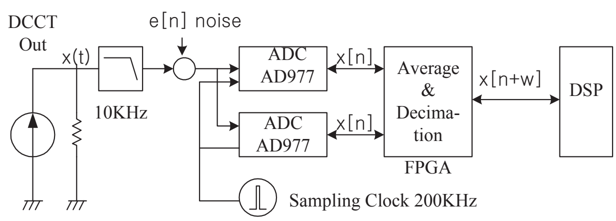


Figure 2: Oversampling and averaging to increase effective resolution.

In this case the oversampling factor *k* is 16. This will lead to improve SNR as following in Table 1.

Table 1: Oversampling Effectiveness

| Factor k | SNR in dB | Extra bits |
|---|---|---|
| 16 | 12 | 2.0 |

## HIGH STABILITY MEASUREMENT

The required current stability of the MPS was less than 10 ppm. The digital volt meter (DVM) to measure the stability of the MPS has to have the high resolution up to about 8-digit.

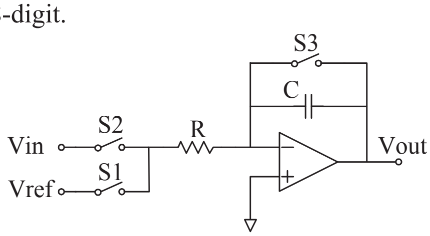


Figure 3: Dual-slop integrator circuits.

The DVM3458A from the Agilent was widely accepted for the stability measurement for the MPS. The DVM3458A uses basically the dual-slope AD converter to increase the resolution by the good noise rejection ratio [4]. Figure 3 showed a typical dual slope integrator which is the basic configuration of the dual-slope ADC. Its working process was described in Ref. [5]. Actual data conversion is accomplished in two phases: input signal integration and reference voltage de-integration. The first, the input voltage $V_{in}$ is applied to the integrator with a fixed length of time $t_u$ by closing the S2. Then output voltage was given as

$$V_{out}(t_u) = = -\frac{1}{RC} V_{in} t_u.$$

Next, $V_{ref}$ with polarity opposite to that of $V_{in}$ is connected by closing S1. Time counter was started at this time until the output of the integrator crosses through zero voltage. The typical waveform of the dual-slope was shown in Fig. 4.

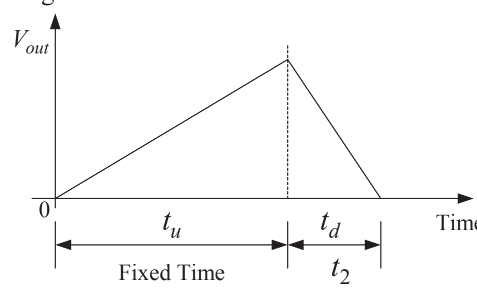


Figure 4: Dual-slope waveform.

This means that the counter contents are proportional to the unknown voltage $V_{in}$. The output voltage $V_{out}$ at the $t_2$ was given as

$$V_{out}(t_2) = V_{out}(t_u) - \frac{1}{RC} V_{ref}(t_d) = 0.$$

Then the unknown input voltage $V_{in}$ can be find by

$$V_{in} = -V_{ref}(t_d/t_u).$$

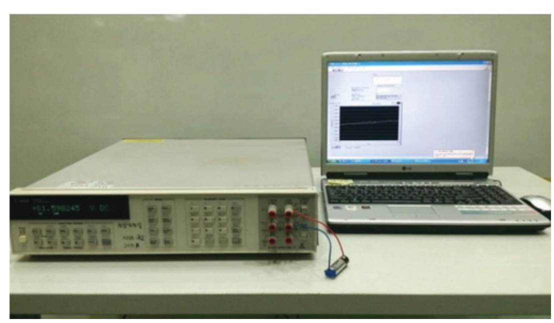

Figure 5: Test setup for the DVM with a battery input.

The DVM3458A has a function of choice for aperture time that is equal to the ADC integration time when direct current volt mode selected and it can be varied from 0.5 μs to 1 s. The default aperture time when power is on is 166.66 ms for 60 Hz AC line voltage. The DVM integrated the input signal thus input noise components averaged to be small during its aperture time. Figure 5

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shows the DVM3458A to test the precision depending on the aperture time with battery input.

The DC battery voltage was measured with various aperture time of the DVM 3458A in the range from 1 μs to 100 ms. With the same conditions, the measured voltages to the battery have the different stability with the different aperture time as following table 2. To measure the a few ppm stability the aperture time should be larger than 10 ms. Figure 6 showed the stability measurement results at the aperture time of 100 ms.

Table 2: Stability Comparison with Various Aperture Time at the Battery Input

| Aperture Time [ms] | 0.001 | 0.01 | 0.1 | 1 | 10 | 100 |
|---|---|---|---|---|---|---|
| Stability [ppm] | 1000 | 250 | 40 | 20 | 2.5 | 1 |

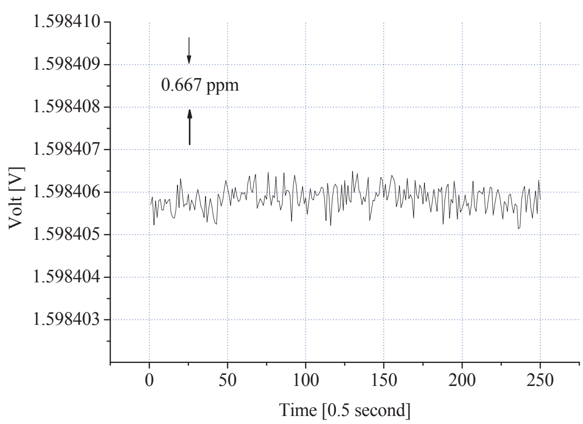


Figure 6: Stability test results at the aperture time of 100 ms.

## EXPERIMENTAL RESULTS

The short term stability of the MPS was examined. Its stability was less than 3 ppm peak-to peak for 15 minutes shown in Figure 7.

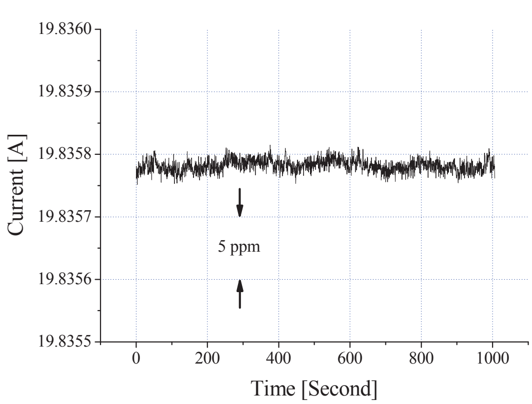


Figure 7: Short-term stability of the 20A bipolar power supply.

The stability variations as increase the output current were tested. The stabilities were become worse as output current increase as shown in Fig. 8.

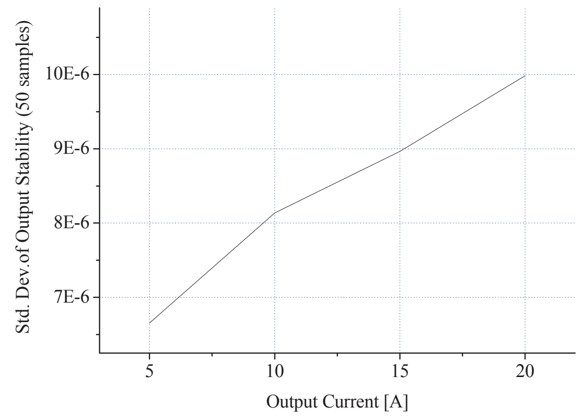


Figure 8: Stability variation on the output current.

## CONCLUSION

This paper described the MPSs which had high stability for the output current. The ripple components of the rectified link voltage were affected the stability according to the sampling theory. Thus the ripple voltage should be attenuated by the filter which was cut-off frequency of 30 Hz. The DVM 3458A from the Agilent showed different measurement results depending on the aperture time selection with the battery input. This means that aperture time should be longer than 100 ms for 1 ppm stability guarantee.

The short term stability showed less than 3 ppm. The stability variation by the output current increase was tested. It showed that the output stability was become worse as increase output current.

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