STATUS AND IMPLEMENTATION OF A WIDEBAND FEEDBACK SYSTEM FOR E-P INSTABILITIES IN THE SNS*

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Abstract

An analog wideband feedback system for damping e-p instabilities has been demonstrated at the PSR at Lansce. A mixed signal system is being developed and deployed at SNS. The status and expected performance of the system is discussed.

BACKGROUND

It has been demonstrated through a series of measurements that an e-p (electron-proton) instability exists in the SNS accumulator ring [1]. For example, see Fig. 1 to see a typical measurement of instability for 10 uC in the SNS ring.

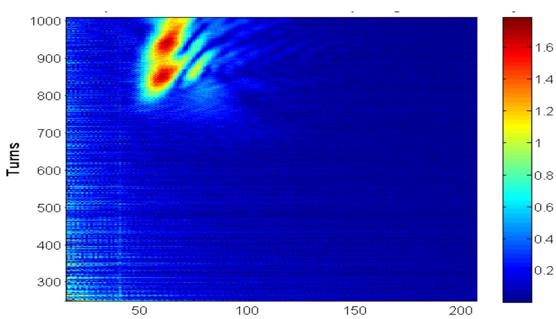

Figure 1: Time, or turns, is the vertical axis vs. Frequency (MHZ) on the horizontal axis. Intensity is depicted as a color. Picture courtesy of S. Cousineau.

To help ensure the steep power ramp up in power for the SNS accelerator, it has been requested, therefore, to design and build a wideband feedback damper system. The design is based on previous work on damping instabilities at the PSR[2].

HARDWARE DESIGN

A dual approach to the hardware is being designed and built. Currently, an analog system is being developed to benchmark the mixed signal design developed in collaboration with the Electrical and Computer Engineering Department at the University of Wisconsin Madison. Details of each system follow.

Stripline Electrodes

A new set of electrodes are being fabricated. These electrodes are tuned to have a peak sensitivity at 150 MHz, and have low coupling from electrode to electrode. This is accomplished with shielding placed between the striplines. This benefits the overall system because the pickup and kicker are then identical designs and a cost savings occurs. This design lowers the overall system phase dispersion and therefore provides a higher effective power delivered to the beam. Pictures of the Stripline electrode design are shown in Figs. 2 and 3.

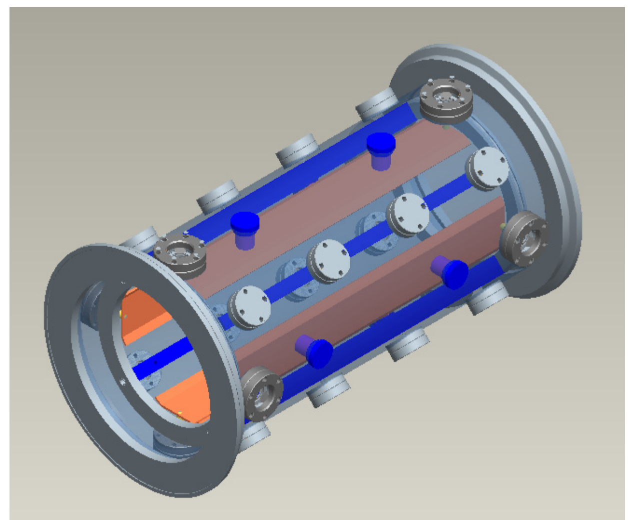

Figure 2: Mechanical design of pickup / kicker stripline electrodes. Striplines are shown in orange, shields between electrodes are shown in blue.

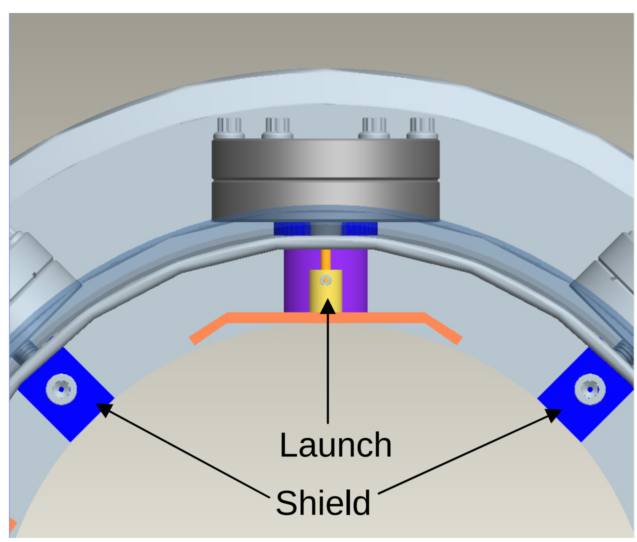

Figure 3: Launch is designed with fitting (in yellow) to reduce parasitic inductance of the feed-thru. Electrodes are designed with straight pieces for mechanical stability and cheaper manufacturing cost. Shields between electrodes reduce the coupling from electrode to electrode.

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- Signal from electrode launches to cable with better than -30 dB (calculated).
- Profile of electrode with angles simple to manufacture
- Better than -30 dB coupling from mode to mode.
- TiN coating program beginning with collaboration of SNS-NFDD and West Virginia University with Prof. Earl Scime.

Power Amplifiers

The requirement on power necessary for full intensity is 300 Watts per electrode [3]. Measurements have shown instabilities up to about 200 MHz. This requires, therefore a broadband phase flat amplifier. An amplifier was produced which exceeds these requirements.

- Complete solid state design.
- Gated to pulse the amplifier (reduces power requirement / heat load in racks).
- 4 stages of parallel 100 Watt amplifiers.
- Separate MPS (machine protection system) control on current drive + temp sensors to each SiC MESFET.
- Werlatone [4] power combiner on output.

A photo of the amplifier is shown in Figs. 4 and 5.

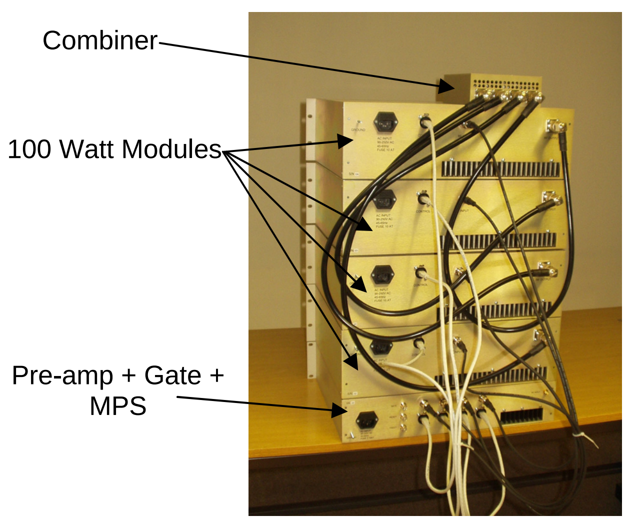

Figure 4: Back view of the amplifier. Pre-amp receives gate signal, which is then distributed to each 100 W stage. Combiner at the top. Photo courtesy of Intertronic Solutions [5] / Eltac Ltd [6].

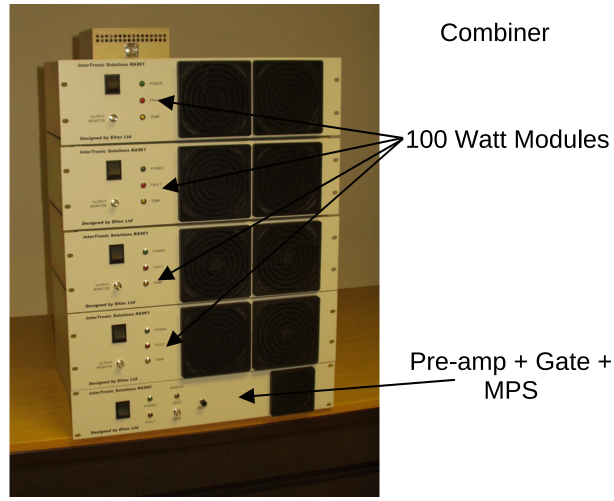

Figure 5: Fault indicators and switch to running unit in remote control and local mode are shown, Power monitoring ports are at the front of each stage for assessing overall health of unit. Photo courtesy of Intertronic Solutions / Eltac Ltd.

A measurement of the transfer function of the amplifier is shown in Fig. 6.

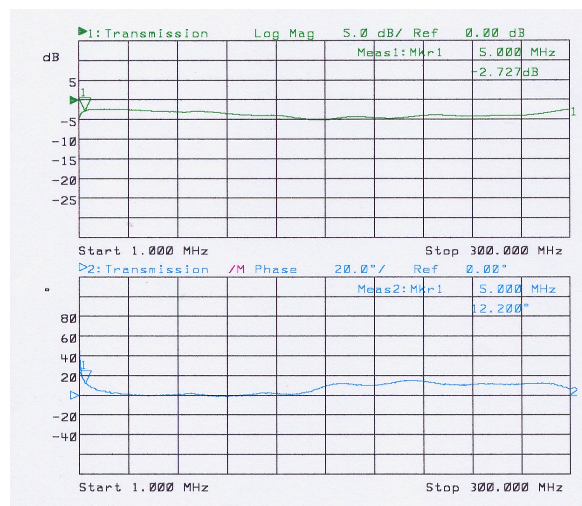

Figure 6: Gain and phase of amplifier are +/- 1 dB and +/- 10 degrees from 1 MHz to 300 MHz. Measurement courtesy of Intertronic Solutions / Eltac Ltd.

Mixed Signal System Design

The overall system is controlled the Triton card (ADC (analog to digital convertor) + FPGA (field programmable gate array) + DAC (digital to analog converter), designed by TEK Microsystems) [7]. A photo of the card is shown in Fig. 7.

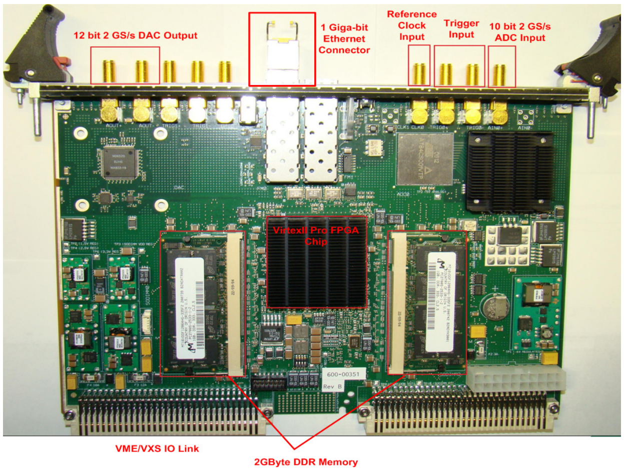

Figure 7: The Triton circuit card, designed by TEK Microsystems. On board 2 GB memory, 1 Gbit/sec UDP Ethernet, ADC + FPGA + DAC.

The system design is shown in Fig. 8. As shown, a PC running Labview will be controlling and monitoring the Triton card. Filter coefficients are downloaded to the Triton card using Labview, and data can be retrieved from the Triton card. The system permits users to have two separate modes of operation – namely, operational and research. In the research mode, four additional ADCs capture raw data from signals from the pickups and kickers, while capturing coherent data from the Triton card.

A schematic of the functionality of the mixed signal system is shown in Fig. 9.

Clearly in Fig. 9, the Triton system lies between the ADC and the DAC. It contains a programmable fixed digital gain stage, a programmable delay (FIFO) up to five microseconds, an FIR (Finite Impulse Response) filter, and two comb filters capable of notches at every one-half revolution.

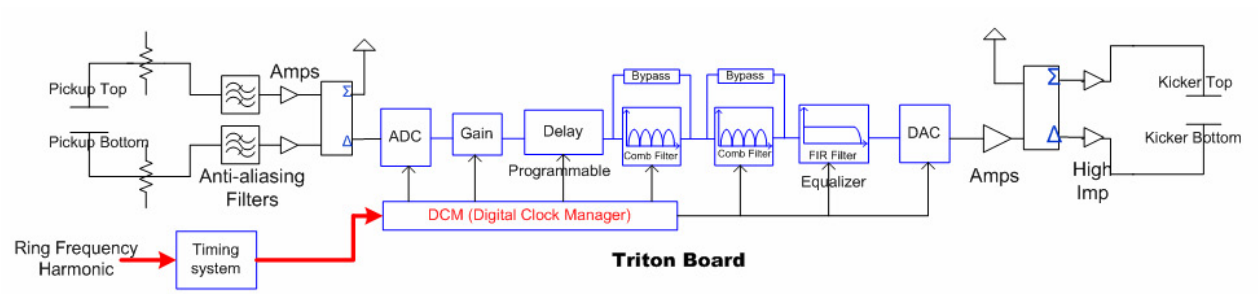

Figure 9: Schematic of the mixed signal FPGA based system. Critical to the system is the DCM to keep data synchronous. Digital gain, digital delay, and two comb filters can be used or bypassed before sending data out to the DAC.

The system is designed by having a synchronous clock of the master timing system. This is to say that the system will run at some multiple of the ring RF frequency, which is about 1.05 MHz currently. It is envisioned that a multiple of 1600 times the ring clock be used, which implies that the ADC and DAC run about 1.680 GHz.

The FIR filter is key to the flexibility and strength of the system, as it allows users of the system to equalize the system, thereby making gains and/or phases to any programmable levels. A schematic of the FIR filter is depicted in Fig. 10.

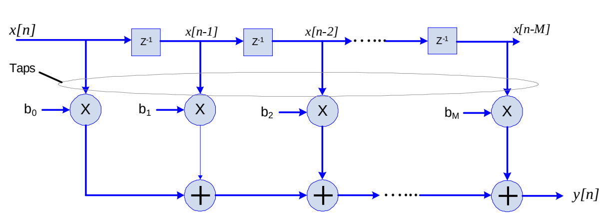

Figure 10. The FIR filter. The outgoing signal is convolved with a programmable predefined response signal.

To implement the FIR filter with 256 taps, a 16-channel parallel FIR filter which has a total of 256*(3/2)^4=1296 taps may be used. Computations such as the multiplications will be performed by simple lookup tables rather than use the limited FPGA resources.

A simple test of the functionality of the system's comb filters is depicted in Fig. 11. The test showed that notch depths of up to 40 dB are possible. By staging two comb filters in series one can achieve up to 80 dB of ring RF rejection. This is an important feature to the system, as the ring harmonics are simply offsets of the beam about the electrical axis of the pickup striplines. By filtering these out of the system, RF power of the power amplifiers is saved.

Figure 11: Measurement of sample comb filter. The system is capable of producing up to -40 dB notches.

CONCLUSION

It has been observed that the SNS ring has an e-p instability. To help meet the power ramp up, a wideband feedback system is being developed. The wideband feedback system will deploy tuned stripline electrodes, a mixed signal feedback system, as well as up to 600 Watts/plane of rf power. Parts are being manufactured for the stripline electrodes, a TiN coating program in collaboration with West Virginia University is being developed, the amplifiers have been designed and one has been delivered. Most of the FPGA code has been written and now needs time to be fine-tuned for timing accuracy.

REFERENCES

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[6] http://eltac.co.uk/.
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