THE DARMSTADT MULTI-FREQUENCY DIGITAL LOW LEVEL RF SYSTEM IN PULSED APPLICATION*

R. Eichhorn#, U. Bonnes, C. Burandt, M. Konrad, P. Nonn,
IKP, TU Darmstadt, Darmstadt, Germany
G. Schreiber, W. Vinzenz, GSI Darmstadt, Germany

Abstract

Triggered by the need to control the superconducting cavities of the S-DALINAC, the development of a digital low level RF control system was started several years ago. The chosen design proved to be very flexible since other frequencies than the original 3 GHz may be adapted easily: The system converts the RF signal coming from the cavity (e. g. 3 GHz) down to the base band using a hardware I/Q demodulator. The base band signals are digitized by ADCs and fed into a FPGA where the control algorithm is implemented. The resulting signals are I/Q modulated before they are sent back to the cavity. Meanwhile, this system has been successfully operated on 3 GHz, 6 GHz and 325 MHz cavities, on normal and superconducting cavities as well as in cw or pulsed mode. This contribution will focus on the 325 MHz version built to control a pulsed prototype test stand for the p-LINAC at FAIR and possible extensions to even lower frequencies. We will present the architecture of the RF control system as well as results obtained during operation.

INTRODUCTION

The S-DALINAC is an 130MeV recirculating electron linac that is operated in CW mode [1]. It uses superconducting niobium cavities at 2K with a loaded Q of $3 \cdot 10^7$ for acceleration. Their 20 cell design and the high operating frequency of 3GHz make them very susceptible for microphonics. Designing and improving the Low-Level RF System therefore was and is one major research activity [2,3].

In addition to the superconducting cavities, room-temperature chopper and buncher cavities are operated. As the new polarized electron injector has been assembled in the accelerator hall [4] the need for a harmonic system arose: Its bunching system consists of a chopper cavity and a 3 GHz as well as a 6 GHz harmonic buncher. Currently, our RF control system has to deal with different loaded quality factors (Q_L) ranging from some 5000 to $3 \cdot 10^7$ as well as with different operating frequencies. Due to its modular design, reflected in the hardware design as well as in the control algorithm (being programmed into an FPGA) the system was adapted to the needs of proton Linac currently under design ats GSI/FAIR [5]. This normal conducting drift tube linac comprises 12 crossed-bar H-mode cavities (CH cavities) that are operated at 325.224MHz in pulsed mode, requiring some major changes in the RF control, described lateron. The cavities are fed with RF pulses of 200 µs length at a maximum repetition rate of 4 Hz [6]. The beam pulse length is 36 µs, representing a significant beam load of approx. 80 %. Based on beam dynamics calculations, the field stability requirements were set to 0.1 % and .5°.

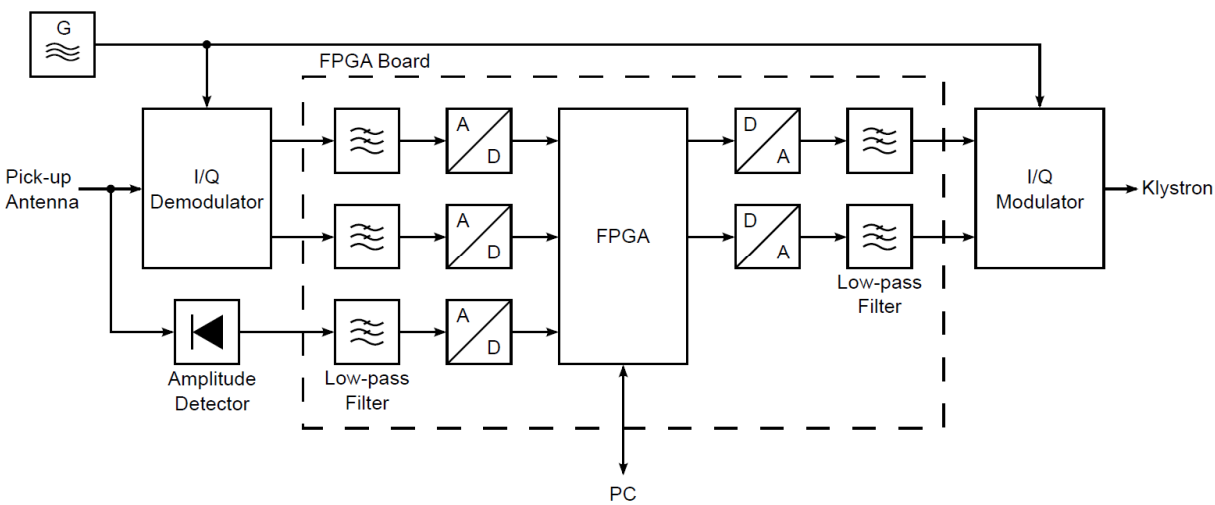

Figure 1: Overview of the hardware components of the rf control system. The (frequency dependant) modulator and demodulator are located on the rf board whereas the FPGA board only contains the signal processing hardware. The control algorithm itself is programmed into the FPGA, allowing SEL and GDS operation.

*Work supported by DFG through CRC 634 and by the BMBF under 06 DA 9024 I
eichhorn@ikp.tu-darmstadt.de, affiliation starting July 2012: Cornell University, Ithaca, NY, USA

SYSTEM ARCHITECTURE

The approach to control the RF chosen in Darmstadt was the base-band solution: All RF signals are down converted to the base band by mixing with the operation frequency, processed in the remaining low frequency domain and up converted later on by modulation, again using the master oscillator running at the operation frequency. This allows spliting the hardware into two parts: A frequency dependent RF board containing the I/Q (de)modulator and a frequency independent FPGA board processing the signals (see Fig. 1). All hardware components have been developed in-house. A separate power detector located on the RF board improves the accuracy of the magnitude measurement.

RF BOARD

The photo of the RF board, given in fig. 2, displays the principle of the layout: The incoming signal (right connector) is split and fed to the I/Q demodulator and the power detector. The low frequency signals then leave to the FPGA board (show later on in fig. 4) via the multipole connector. After the signal processing, the signals are I/Q modulated and leave by the left RF connector.

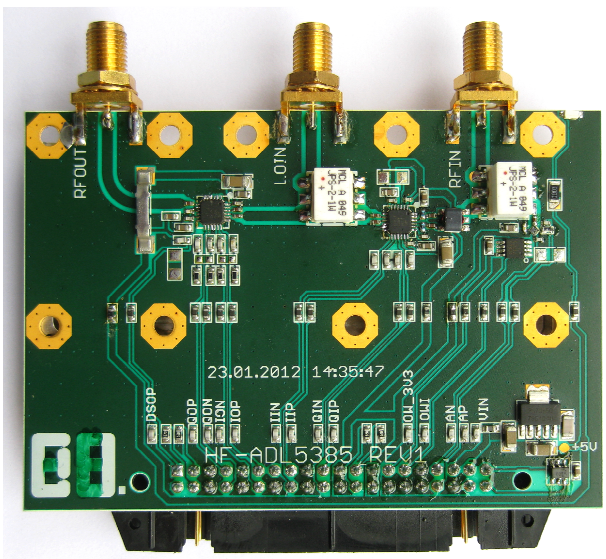

Figure 2: Photo of the (frequency dependent) RF control board. The signal from the cavity is connected to the right SMA connector; the left connector delivers the signal to the cavity while the Local Oscillator (LO) connects to the middle.

Depending on the operation frequency of the cavity, the splitters, modulator and demodulator as well as the power detector have to be chosen accordingly, being a minor modification. So far, we developed a 3 GHz, a 6 GHz, one 1.3 GHz, a 325 MHz and a 160 MHz version of the RF board, all of them where operating successfully. It should be noted that the low frequency versions (325 & 160 MHz) require a doubled LO frequency (650 and 320 MHz) for accuracy reasons.

Every board requires a careful calibration, the details of which have been described before [3]. However, not all errors of the (de)modulator can be compensated by calibration. An important figure of merit of the demodulator is the deviation of the measured input phase from the actual input phase, as shown in fig. 3. This has been measured by applying an rf input signal to the rf board with a frequency that is slightly shifted to the LO frequency (1 kHz away). The result is a rotating vector in the I/Q plane that is recorded over many periods. Figure 3 shows the deviation (for the 325 MHz board) of the phase calculated from I and Q and the input phase. The phase error is dominated by noise, produced by the two rf generators. With the resut of 0.2 ° rms gained after some major design changes[7], the deviation is smaller than the phase error of the 3 GHz boards now, currently used at the S-DALINAC. All together the described hardware errors are negligible, showing the substantial improvements compared to the boards used before.

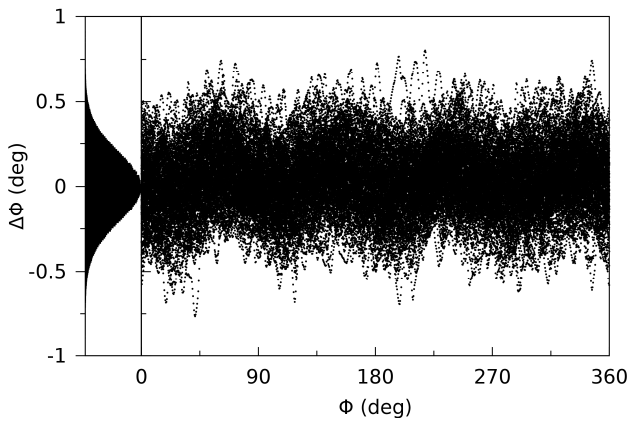

Figure 3: Characterization of the 325 MHz demodulator showing the typical deviation of the measured input phase from the actual input phase. The histogram on the left shows a projection to the y axis representing the phase deviation, being 0.2° rms.

FPGA BOARD

The FPGA board digitizes the analogue signals coming from the RF board and feeds them into its FPGA where the control algorithm is carried out. The resulting I and Q output signals are converted back to analogue before they are sent back.

The hardware of the FPGA board, shown in fig.3 is identical with the boards used at the S-DALINAC except for the filters: Low-pass filters in front of the ADCs ensure that frequencies above the Nyquist frequency are damped to avoid aliasing effects. Identical reconstruction filters at the output remove harmonics created by the DACs.

The filters have been designed for the S-DALINAC's RF control system which has to deal mainly with microphonics at frequencies below 10 kHz. High requirements with respect to accuracy together with

an adjacent mode of the cavity that is only 700 kHz away from the operating frequency led to third order filters with an cut off-frequency of 100 kHz. On the other hand the phase shift introduced by the filters decreases the gain margin of the controller. That is why the filters have been reduced to first order filters with the same cut off-frequency for the p-Linac RF control system. These filters still provide enough attenuation for the neighbouring modes.

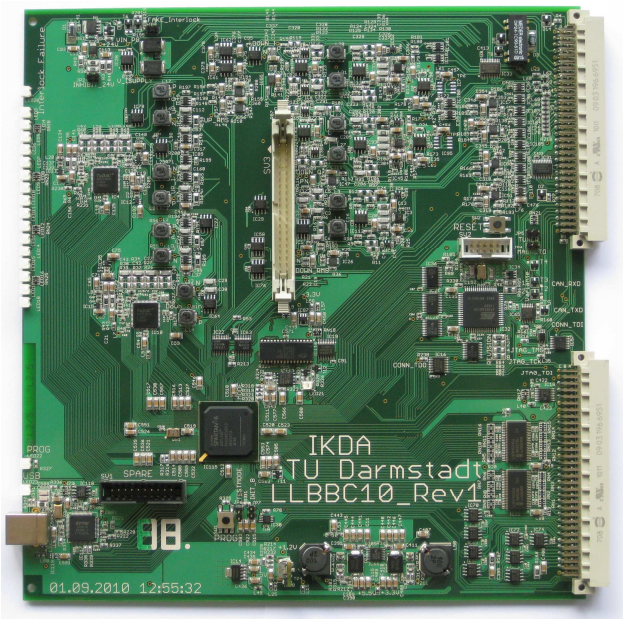

Figure 4: Photo of the FPGA control board, housing the filters, the ADCs/ DACs, the FPGA itself and some interfacing circuits. The signals from the RF board connect to the multi-pole connector in the middle of the board.

CONTROL ALGORITHM

Two different control algorithms have been implemented for the S-DALINAC: A generator-driven resonator control algorithm for normal-conducting cavities and a self-excited loop algorithm for superconducting cavities. Both algorithms are optimized for cw operation and cannot be used in pulsed mode with the p-Linac as they completely rely on static settings.

For pulsed operation, the programming of the FPGA had to undergo a major extension to allow time-dependant settings. In addition, a pulse shape generator has been implemented in the FPGA code. It consists of a memory storing 2048 set values that constitute a pulse shape of up to 2 ms in length. Up to now, the trigger signal for the pulse generator is generated periodically inside the FPGA. At the p-Linac test stand an external trigger signal will be used.

The control algorithm for the p-Linac is an enhanced version of the generator-driven algorithm for the S-DALINAC. A first revision of the p-Linac control algorithm is shown in fig. 5 with separated phase and amplitude controllers. The input phase is calculated from I and Q (provided by the RF board) using the CORDIC [8] algorithm, while the amplitude is measured directly with the power detector on the RF board. The amplitude as well as the phase controller use integral controllers in addition to the proportional controllers to eliminate steady-state offsets that remain after applying proportional control. A differential controller has been foreseen, but is finally used with zero gain as it turned out to amplify the noise solely without contributing to the control accuracy.

Between pulses the input signal vanishes, and thus the input phase has no meaningful value. To ensure that this does not affect the integral phase controller, its accumulator is set to hold between pulses.

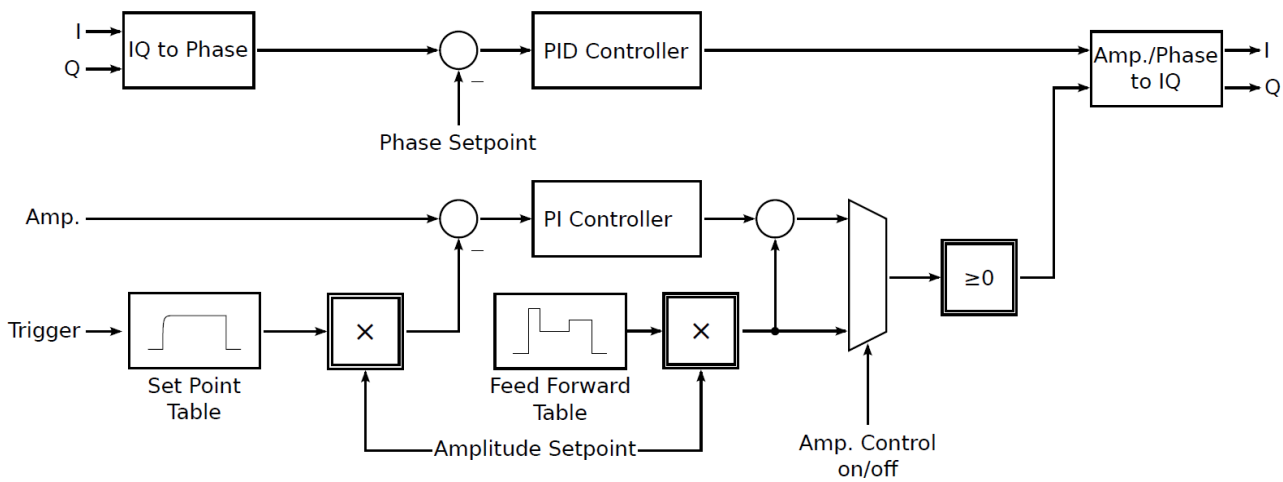

Figure 5: Algorithm flow chart: The I/Q signals from the RF board are converted to a phase signal which is controlled via a PID controller. The amplitude controller uses the signal from the power detector being compared to the time dependant set point table value. In a recent modification, an additional feed forward table was implemented to allow fast beam load compensation.

RESULTS

The performance of this control algorithm has been tested by measuring the amplitude and phase errors using a dummy cavity with a loaded quality factor around 1000. Figure 6 shows the step response of the closed loop whereas fig. 7 shows the rms errors over the time relative to the beginning of the pulse. The rms errors have been calculated from the corresponding errors at the same relative time over a set of 1000 pulses. It takes about 50 µs to stabilize amplitude and phase to the target specification.

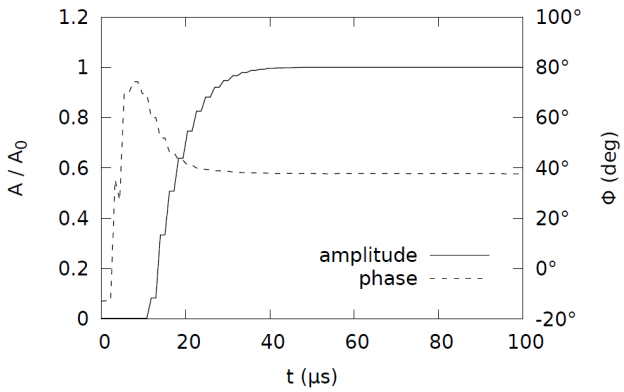

Figure 6: Step response of the the closed control loop measured using a test cavity with $Q_L \sim 1000$.

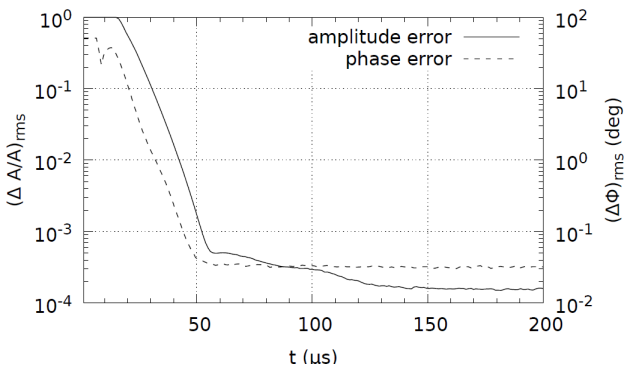

Figure 7: Amplitude and phase error during a 200 µs pulse. The pulse starts at 0 µs when the set value jumps from 0 to the set value.

To achieve a faster response the control algorithm has to provide a feed forward signal which was implemented recently, the need of which can clearly be seen in fig. 7: As the beam pulse planned for the pLinac has a length of 36 µs, a close loop time constant of 50 µs to reach a control accuracy better 10^{-3} is not acceptable. First optimization steps using this feed forward system have been performed and will continue by making use of a cavity simulator developed in house that allows implementation of different beam loading scenarios.

CONCLUSION

The rf control hardware initially designed for the S-DALINAC has been successfully adapted for the FAIR p-Linac. A newly designed RF board allows operation at 325 MHz, whereas redesigned filters provide a much faster response of the controller. Until the first cavity arrives at the test stand at GSI, tests of the RF control system are done with an FPGA-based cavity simulator that is currently under development [9].

During the course of this project, the potential of the base band approach was clearly visible: Within minor redesign steps, the adaption of other frequencies than the original 3 GHz is possible. Currently, first tests with a 160 MHz version to control a quarter wave resonator at ALPI, Legnaro are performed, results of which will be presented soon.

The extension of the operation mode of the system from cw to pulsed was realized within the project. This opens up the perspective for further improvements: Multi-pulse operations with different pulse shapes as well as ramped operation are now easy to realize. Together with the freedom of the algorithm programming this finally let us conclude that the Low Level RF system developed at TU Darmstadt has a great flexibility which seems to be unique.

REFERENCES

[1] A. Richter, “Operational experience at the S-DALINAC”, EPAC’96, Sitges (1996) 110.

[2] J. Auerhammer et. al., “Progress and Status of the S-DALINAC” Proc. 1993 RF Superc. Workshop, Newport News, pp. 1203.

[3] M. Konrad, et. al., “Digital base-band rf control system for the superconducting Darmstadt electron linear accelerator”, Phys. Rev. ST Accel. Beams 15 (2012) 052802.

[4] C. Eckardt et al., “The S-DALINAC Polarized Injector SPIN – Performance and Results”, Proceedings of PAC 2011, New York, USA.

[5] L. Groening et. al., “The 70 MeV proton linac for the Facility for Antiproton and Ion Research FAIR”. Proceedings of LINAC 2006, Knoxville, USA, pp. 186–188.

[6] W. Vinzenz et. al., “High power rf supplies for the FAIR injector linacs”, Proceedings of LINAC 2008, Victoria, Canada, pp. 975–977.

[7] A. Araz et al., “A Digital Baseband Low Level RF Control for the p-LINAC Test Stand at GSI”, Proceedings of IPAC, 2010, Kyoto, Japan, p. 1413.

[8] Xilinx Inc., ‘‘LogiCORE IP CORDIC v4.0—product specification’’, http://www.xilinx.com/support/documentation/ ip_documentation/cordic_ds249.pdf.

[9] T. Bahlo et, al., Proceedings of ICAP, 2012, Rostock, Germany, in preparation.