DEVELOPMENT OF THE NEW ELECTRONIC INSTRUMENTATION FOR THE LIPAc/IFMIF BEAM POSITION MONITORS*

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Abstract

Among all the LIPAc/IFMIF accelerator diagnostics instrumentation, the Beam Position Monitors (BPM's) are a cornerstone for its operation. A new approach for the LIPAc/IFMIF beam position monitors acquisition electronics is proposed for the twenty BPM stations distributed along the accelerator. The new system under development is a fully digital instrumentation which incorporates automatic calibration of the monitors' signals and allows monitoring of both fundamental and second signal harmonics. The current state of the development and first experimental results of the system on the test bench will be presented.

INTRODUCTION

The International Fusion Materials Irradiation Facility (IFMIF), within the framework of the Engineering Validation and Engineering Design Activities (EVEDA), prepares the design and construction of the Linear Prototype Accelerator (LIPAc) to be commissioned in Rokkasho, Japan, along the year 2014.

An important diagnostic for the machine operation is provided by the BPM system, for both beam commissioning and accelerator tuning and operation. It provides to the Central Control System (CCS) the variation of the beam centroid in the transverse plane (position) and the longitudinal plane (phase).

The BPM's are to be distributed along the transport lines –Medium Energy Beam Transport line (MEBT)- and High Energy Beam Transport line (HEBT)-, together to the superconducting accelerating sections (SRF linac) and those other locations required by the beam dynamics team to give a good feedback for steering and transporting the beam from the RFQ to the Beam Dump.

In addition to this, the BPM's located at the Diagnostics Plate will be committed to carrying out energy measurements, as such information is crucial for the tuning of the cavities and a proper validation and characterization of the output beam in each beam commissioning stage.

In the previous years a series of evaluation on commercial options and a prototype for the electronics based on analog processing were evaluated [1].

BPM STATION ELECTRONICS

The electronic system design for the BPM's is based on CompactPCI. This architecture was selected because the same digitizers are also the key to the Low-Level RadioFrequency (LLRF) system developed at CIEMAT [2] for IFMIF/LIPAc.

The BPM system is to be integrated into the EPICS control system of the accelerator facility via Ethernet and the EPICS Channel Access, and the position and phase information is sent to the CCS updated at a rate of 2 Hz approximately. Likewise, it is required to make a database system based on EPICS Channel Access in order to save the most recent position and phase information at a rate of 0.5 Hz [3].

General Layout

The full system comprises of two cPCI racks hosting, as depicted in figure 1:

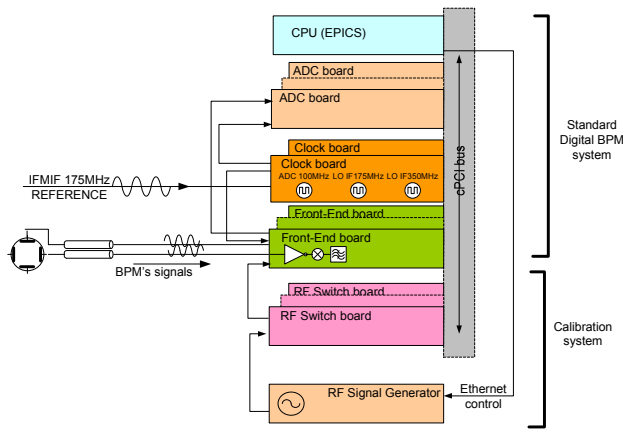

Figure 1: General layout of the BPM electronics.

- A Central Processing Unit (CPU) running Red Hat Linux 5.3 Operating System (OS) with kernel 2.6 and integrated into the IFMIF control system via EPICS.
- Several RF Digitizers, in particular the VHS-ADC CompactPCI (cPCI) board from Nutaq (formerly Lyrtech) [4], equipped with 16 ADC channels of 14b with a sampling rate of 100 MHz and an on-board virtex-4SX Field Programmable Gate Array (FPGA)
- The Analog Front-End boards, custom designed, performing basic filtering and a direct conversion to a low-frequency intermediate frequency (IF) stage, in the analog domain. This board can also reroute RF signals for self-diagnostics.
- Two Clock distribution boards, the ADAC-SYNC cPCI also from Nutaq [4], for distributing the sampling ADC master clock to all the digitizers and the different local oscillator (LO) frequencies for down-conversion to the Front-End cards.

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- Four RF Switch boards for distribution of the self-monitoring and calibration signals to all channels, from the diagnostics generator.
- One Timing card, which buffers the Trigger and Gate signals from the IFMIF Timing Distribution system and generates the gating and timing marks for calibration purposes along with the analog envelope for measurement of the cable health.
- Finally, a commercial RF signal generator with a high power module for exciting the calibration ports at their maximum nominal power of 23dBm.

Table 1 summarizes the main parameters of the beam, precision requirements and signal levels at the entrance of the BPM front-end electronics [3].

Table 1: Main LIPAc BPM Parameters

Parameter		Value
Beam Parameters		
	Beam energy	5..9MeV
	Beam current	90..126mA
	RF pulse width	200 μs..CW
	Duty cycle	0.1..100%
Resolution and precision requirements		
	Position resolution	10 μm
	Position accuracy (ABS)	100 μm
	Phase resolution	0.3 deg
	Phase precision (ABS)	2 deg
Signal levels at the Front-End electronics input		
	Max. input power	+22 dBm
	Required Input dynamic range	50 dB

Analog Front-End Electronics

The high sensitivity of the measurement and the need to obtain a precise readout of the beam position has weighted on the decision to introduce an analog front-end prior to the signal digitizer, to balance digitizer bandwidth and precision

However there are other considerations that pointed in that direction.

First, the VHS-ADC board has an analog bandwidth of 250 MHz@-3dB, making risky to measure beyond that frequency. The 350 MHz band, the beam's second harmonic, would be likely to provide a noisy measurement even using band-pass sampling.

Secondly, the 14b ADC has its maximum ENOB of 13.6 bit c.a. 30 MHz, and obtaining the maximum precision was paramount.

A third reason is the minimum band filtering needed prior to the input stages, and provide for a DC path necessary for the discharge of the capacitive captors of some BPM stations.

These two unavoidable reasons, along with the goal to include a self-diagnostics capability within the system precluded the inclusion of an intermediate board before the digitizer.

Down-converting the two frequency bands, 175 MHz and 350 MHz down to the 20 MHz intermediate frequency (IF) was therefore a sensible solution to accommodate all four requirements. A non-zero IF was selected to avoid problems related to quadrature DC offset.

This card is controlled by an FPGA which interfaces to the CCS via the EPICS subsystem.

Each of the analog channels can be individually adjusted in gain and attenuation, and the measurement frequency band (175 MHz, 350 MHz) selected via software.

Timing Distribution Board

The IFMIF timing system is based on a Trigger and a Gate signals, and this board basically acts as a fan-out device, yet controlled through the cPCI with an FPGA, which serves for timing monitoring and also to interstice calibration signals when the self-diagnostics is being performed with the beam on-line.

The card also modulates the RF calibration pulse in amplitude, to obtain the most of the limited capabilities of the cable check algorithm.

RF Distribution Board

The calibration signal coming from the commercial generator is distributed to every each of the 80 input channels through these boards.

They are switch stages controlled by the cPCI interface, and synchronized to the Timing Board for a precise signal injection

Clock Board

The clock board is in charge of generate the different frequencies needed in the signal stages for the mixers, translating the 175MHz and 350MHz bands down to the 20MHz IF.

The card generates as well the ADC clocks for the five digitizers. The main IFMIF RF clock is used as time base.

Digitizer

This commercial board from Nutaq is equipped with 16 ADC channels feeding data to an on-board processing device, a Xilinx Virtex-4SX.

Each one of the 16 channels is processed in parallel, with standard digital receiver architecture. Filtering followed by a digital down-conversion take the signals down to baseband, where they are decimated and through the use of the CORDIC algorithm [5] the amplitude and phase of each signal is extracted (as a matter of fact

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CORDIC is also used for the numerical oscillator of the digital IF).

This generates far more data than needed by the CCS, but detailed post-mortem information is a requirement of the system, so the CCS only receives an averaging of the measurements.

SELF-CALIBRATION AND IN-SITU CABLING DIAGNOSTICS CAPABILITY

The cabling between the acquisition electronics in the electronics room and the BPM sensors at the accelerator vault will be split in three parts. From the sensors up to a patch panel in the mechanical frame a rigid coaxial cable is to be used with mating SMA connectors. From that point up to the acquisition electronics, between 40 and 70 m depending on the location of the BPM station, a flexible low losses coaxial cable connects the stations to the electronics rack. For further detail refer to [6].

Nevertheless there is a concern about checking the health of both cables and measurements, due to the high relevance of the measurements gathered by the system.

Therefore a very particular protocol of self-calibration inspired on previous work from reference [7], and cable failure detection systems derived from applications on avionics [8, 9], taking advantage of the front-end board presence.

This board serves not only for performing a down-conversion but to inject well-defined and characterised excitations into the cables and the electronics, coming from a commercial RF generator.

Such signal injection serves as checks which can be performed with the beam operating, with the obvious limitations, whether when no beam is present or by just disconnecting the measurement channel for the test cycle, as the high number of BPM station allows for marginal operation of one station with only three of the four channels for a limited time.

Also, thanks to the application of reflectometry techniques, a testing of the cabling is performed. Mind that it is not desired to measure the value of the impedance discontinuities (failures) in the cables, but to detect them when comparing the measurements against a golden reference.

Summarizing, there are three differentiated modes of self-diagnostics, which are presented hereafter.

RF Electronics Chain Calibration

In this mode the well-defined RF signal excites the front-end and digitizer boards, disconnecting the actual BPM output meanwhile (figure 2)

This mode allows for the calibration of the electronics and the failure detection in any of the readout stages, as the RF generator is a signal reference of high quality and all the RF paths are characterised.

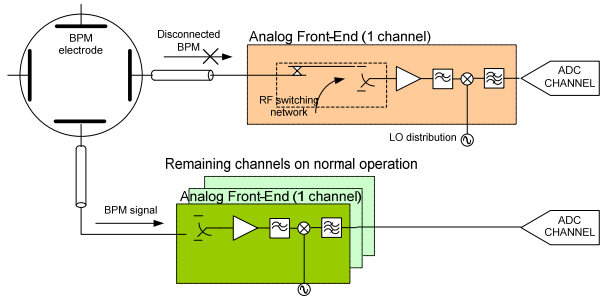

Figure 2: Calibration of the RF electronics.

BPM Coupling-Factor Calibration

Here the calibration signal is routed from the front-End board to the BPM button and from there it is coupled to the other three buttons. This measurement is crucial for characterising the BPM station (figure 3).

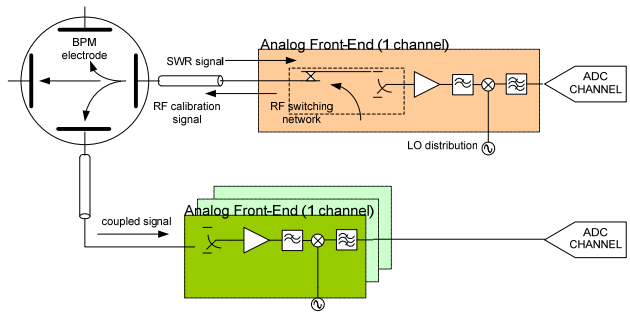

Figure 3: Measurement of BPM button coupling and SWR.

The reference signal is injected into the BPM captor and the coupling of the signal into the other buttons is measured, to check inter-channel coupling (although the opposite captor is far away enough to pick-up any signal at all)

On the other hand the channel which is injecting the signal to its BPM button is disabled. It would be a pity not to take advantage of its digitizer channel to study the transmission line itself.

Cable Diagnostics

It is well known that for measuring or detecting faults in cabling several methods are used, namely Time-Domain Reflectometry (TDR), Frequency-Domain Reflectometry (FDR) among the most well-known, and a combination of both referred as Time-Frequency-Domain Reflectometry with will be tested in the proposed system for accelerator applications [8]. FDR type techniques may also be classified as frequency-modulated continuous wave (FMCW), phase-detection FDR and standing wave reflectometry (SWR), where it is measured the standing wave voltage at the source point. This measurement has less accuracy but it has the advantage of being relatively simple to implement in hardware.

TDR methods are not possible to implement due to the severe bandwidth and signal routing limitations of the Front-End board.

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However, FDR is appropriate in spite of the limited bandwidth for fault detection, and the calibration system is flexible enough to allow the three techniques afore mentioned: PDFDR, SWR and standard FDR.

So in the cable diagnostics mode (figure 3), at the same time that the RF calibration signal is injected down the transmission line to the BPM button, the reflected wave coming from the excited captor is measured by the digitizer via a directional coupler, providing a measurement of the standing voltage at the reference point. This information helps to detect irregularities as they deviate from an initial nominal state, previously recorded at installation time after the cabling is lay out. On the other hand, by using standard FDR techniques, the reference signal is driven into the BPM terminal and its response measured.

The particular figures for this system allow a bandwidth of the front-end of 300 MHz, hence the actual resolution would be [9],

$$\text{Resolution (m)} = \frac{1}{2} v_p \cdot c \frac{k}{\Delta f} = \frac{1}{2} \frac{0.78 \cdot 3 \cdot 10^8 \cdot 1.95}{300 \cdot 10^6} = 0.76\,m \qquad (1)$$

Where v_p is the relative propagation speed of the cable and c is the speed of light.

So exciting the cabling with a RF chirp with a linear frequency modulation of 300 MHz, with steps of 1 MHz, would suffice to detect problem within c.a. 80 cm.

This figure stands valid for our application, as the range of detection results as

$$\text{Range (m)} = \text{Resolution (m)} \cdot (\text{N} - 1) \approx 0.76 \cdot 300 = 228\,m \qquad (2)$$

Where N is the number of frequency points, or the number of frequencies exciting the wiring. For this case, the system needs to inject either a chirp or perform independent measurement for each frequency driven by the RF signal generator.

To better refine the measurement, the Timing board not only generates the Trigger pulse for the RF generator to send the signal pulse, but also is able to modulate the envelope of the RF chirp with a given shape, aiming to make extensive use of time-frequency analysis [10]. The configuration of the system for doing so is depicted on figure 4.

It must be said that in any case, the cable diagnostics rely on the preliminary cable mapping at the installation phase of the wiring, obtaining the frequency signature of all the 80 lines from their BPM buttons up to the RF patch panel at the BPM electronics rack.

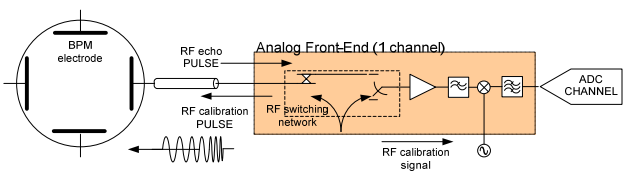

Figure 4: Measurement of fault in cabling, using time-frequency analysis.

CONCLUSIONS

The new BPM's electronics architecture for the IFMIF/LIPAC accelerator has been presented and discussed, with a calibration subsystem which will allow to smoothly check on-line the stability and operation of the electronics and the BPM's pick-ups.

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