# A NEW HIGH-DYNAMIC RANGE BPM FOR ELBE WITH INTEGRATED DIFFERENTIAL CURRENT MONITOR (DCM)

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*Abstract*

ELBE is a LINAC electron accelerator for small energies (12 to 50 MeV) [1]. It serves as a beam source for many quite different experiments. The recent ELBE upgrade allows electron beams with bunches in the area of single electrons to 1 nC. The maximum beam current is 1.6 mA CW and the repetition rates covering the range from one shot single bunch pulses to 26 MHz CW.

The existing BPMs and especially the DCMs which are used for the Machine Protection System cannot handle this newer, wide parameter range. To improve this situation the development of new BPMs / DCMs was necessary. The DCMs measure the difference of the beam current between two stripline sensors and produce an interlock for differences greater 10 µA. The new BPM electronics system has been designed including the DCM functionality because both BPMs and DCMs use the same stripline sensor signals at 1.3 GHz.

## EXISTING BPMS AND DCMS AT ELBE

Stripline sensors with λ/4 length for 1.3 GHz are used as beam position sensors. Beam position monitoring was done by analogue BPMs. Analogue logarithmic RF level detectors with a linear dynamic range of roughly 50 dB were used [2]. Because of the low beam energies of 12 … 50 MeV the beam size is not very small and no high position accuracy is needed.

The Machine Protection System used separate Differential Current Monitors (DCMs) based on the same sensors. Two types are used: RF-RF-DCMs watch the beam current difference between two stripline sensors and RF-LF-DCMs watch the beam current difference between a stripline sensor and a beam dump. A beam loss of greater than 10 µA produces an interlock. The integration time in the electronics is 100 ms. The maximum beam loss energy is therefore 50 Ws which does not yet damage the machine. A higher beam loss creates a shorter reaction time. The RF part of the DCMs detects the beam current by analogue RF summing of the RF signals of the 4 stripline sensor electrodes and level detection. Linear analogue RF level detectors based on Schottky diode peak detectors with a dynamic range of roughly 46 dB were used.

The DCMs are not the only system for beam loss detection. A radiation based cable ionization chamber system complements the DCM system [3].

## ELBE UPGRADE

The ELBE accelerator is in operation since 2001. The accelerator was designed for bunch charges till 77 pC or 1 mA beam current in CW delivered by a thermionic gun. The main foreseen operation mode was 13 MHz bunch repetition rate in CW but different repetition rates are possible [1].

Today ELBE has a great variety of beam modes:

- The bunch repetition frequency may be 26 MHz divided by 1:1 … 1:256, e.g. 26 MHz … 102 kHz or also 260 MHz.
- A macro pulse with a length between 100 µs and 36 ms and repetition time between 40 ms and 1 s may be used.
- 1 … $2^{31}$ single bunches with a repetition time between 100 µs and 1000 s may be used.
- The new superconducting RF gun (SRF gun) can be used instead of the thermionic gun with bunch repetition frequencies of 13 MHz, 500 kHz, 250 kHz and 100 kHz [4].
- The SRF gun macro pulse with a length between 100 µs and 20 ms and repetition time between 20 ms and 10 s may be used.

Because ELBE is a user facility with a lot of quite different experiments all these modes and combinations of them will be used.

But not only the timing is very flexible: also the bunch charge and the beam current have a huge range. Some experiments use only single electrons, whereas the SRF gun will allow bunch charges till 1 nC which is 13 times the maximum bunch charge of the thermionic gun. The ELBE RF power upgrade increased the maximum beam current to 1.6 mA CW [5].

The existing BPMs and especially the DCMs cannot handle this wide parameter range. The dynamic ranges are too small and the linearity is not sufficient. BPM result synchronization was difficult. The different type of current measurements in the RF-LF-DCMs (stripline sensors against a beam dump) caused problems which could not be fixed in the actual system. To improve this situation the development of new BPMs / DCMs was necessary.

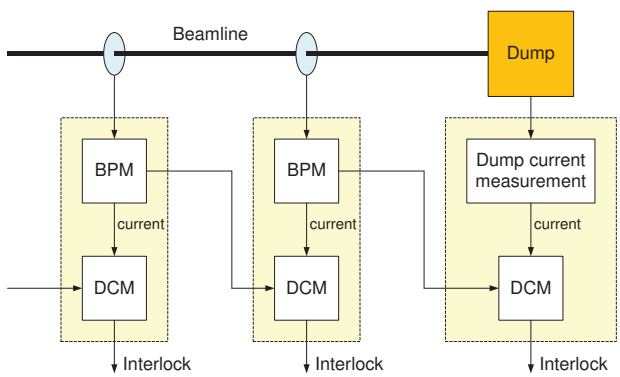


Figure 1: DCM working principle.



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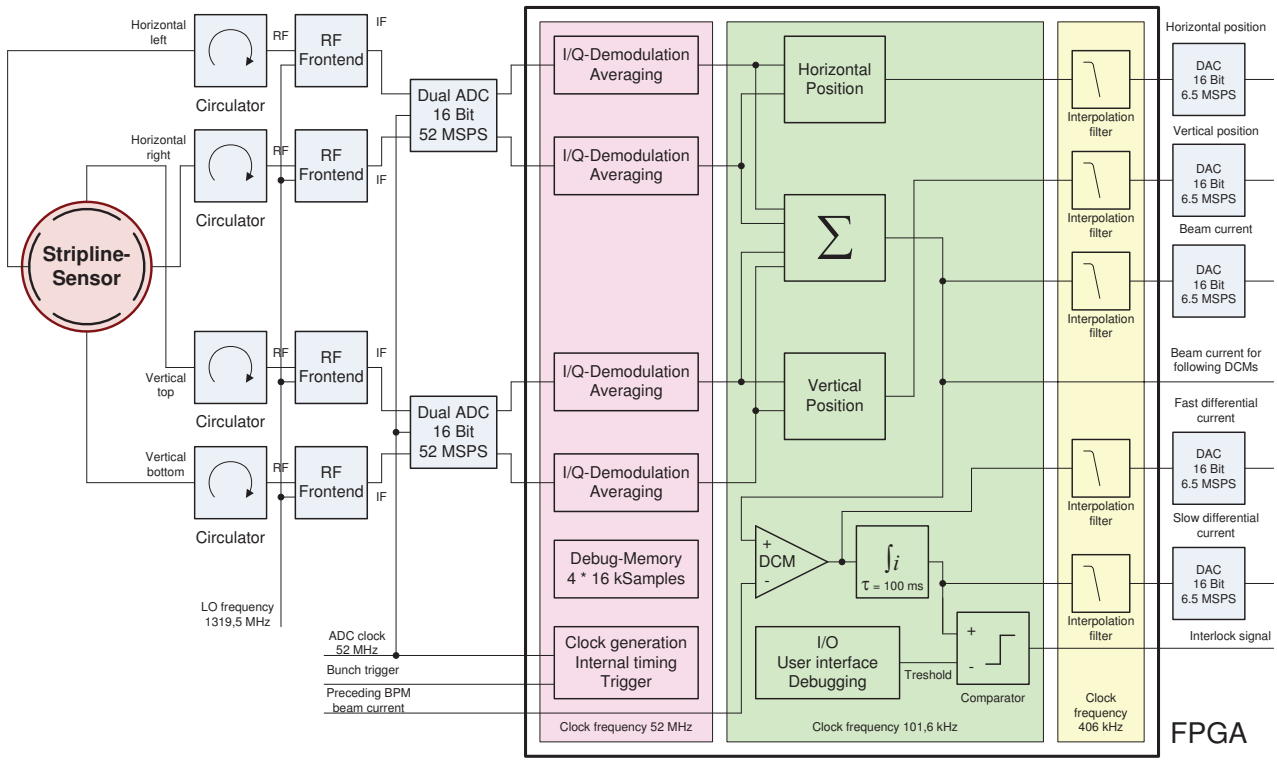


Figure 2: Overview of the new BPM/DCM electronics.

## NEW DCM

The new DCM scheme is shown in Fig. 1. The old RF-RF-DCM functionality is included in the new BPMs. The old RF-LF-DCMs will also be replaced. A new RF-LF-DCM with a new dump current measurement is yet under development and will not be further considered in this paper. This DCM will use many parts from the BPMs.

## NEW BPM

The new BPMs are based on digital signal processing. This processing is completely synchronized with ELBE. The analogue signals at 1.3 GHz are filtered, amplified and down converted to an IF of 19.5 MHz. The IF signals are digitized with 16 Bit resolution and 52 MSPS. These data are processed in a FPGA. In the FPGA an I/Q-demodulation is done. The I/Q-signals are averaged over 512 values according to a measurement window of 9.85 µs. This corresponds to the lowest thermionic gun bunch repetition frequency of 102 kHz. This synchronous operation combined with the true RMS calculation in the FPGA gives complete result independence from the bunch repetition frequency – a major improvement compared to the existing system. The result frequency of 102 kHz helps the ELBE operators to do time resolved measurements in the machine. After amplitude calculation the beam positions and the beam current are determined. These data may be polled by the visualization system. For compatibility reasons the results are interpolated and converted to analogue signals with 16 Bit resolution.

### *RF Frontend*

The goal of the RF frontend design was to maximize the dynamic range with low power consumption. The big variety in bunch modes gives different analogue signals in the RF Frontend: For high bunch repetition frequencies the input signal is after bandpass filtering practically a CW sin wave, whereas low bunch repetition frequencies or single bunch modes give signals like RF bursts. Intermediate signal shapes result between these two cases. The filter attenuation is different for these signal types.

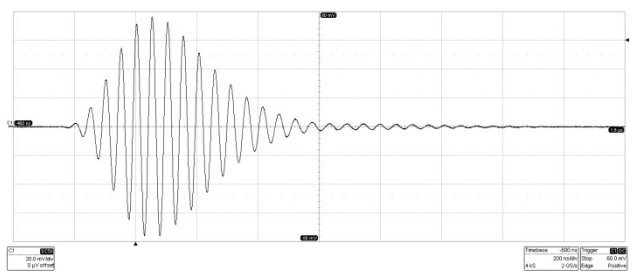

Figure 3: RF burst signal for a single bunch at IF output.



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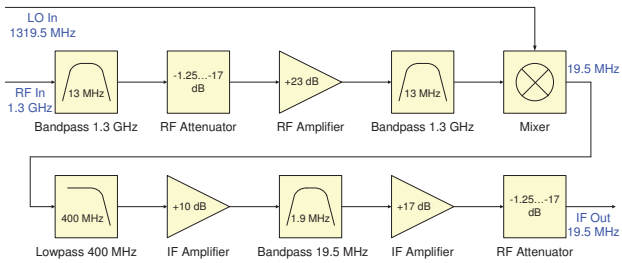


Figure 4: RF Frontend block diagram.

The block diagram itself shows the usual RF radio design. With two programmable attenuators the gain may be adjusted by more than 30 dB in 0.25 dB steps to get optimum ADC signal range usage. The overall RF bandwidth is 1.8 MHz and the RF image rejection at 1339 MHz is greater than 70 dB. The sampling frequency image at 1287 MHz (32.5 MHz in the IF) is suppressed by more than 85 dB. The noise figure of the RF frontend is 8 dB (dominated by the insertion losses before the first RF amplifier) and the dynamic range is roughly 110 dB.

Because of the synchronized operation shielding is very important. The BPMs will be used in the same room where the 10 RF power amplifiers (each of them with an output power of 10 kW CW at 1.3 GHz) are located. The RF frontend is built in a completely closed, shielded box.

### *ADC*

Two dual ADCs digitize the 4 IF signals. Sampling is done with 16 Bit resolution at 52 MSPS. Low power dual ADCs were chosen. The use of dual ADCs with serial LVDS output reduces the needed FPGA pin count. The BPM design is based on an IF frequency of 3/8 the sampling rate of the ADC. This way the I/Q-demodulation in the FPGA is easy and acts like a bandpass filter with notches for the ADC harmonics. The seventh and the ninth harmonics are the first harmonics which are not suppressed.

### *Signal Processing in the FPGA*

The I/Q-demodulated signals are averaged over 512 values. This gives a resulting system bandwidth of 95 kHz which is the basis for achieving a high dynamic range. After averaging the noise is below one ADC-LSB and the signal processing rate is reduced to 102 kHz. An external bunch trigger signal is used for synchronization with single bunches. The horizontal and the vertical beam position are determined by the difference over the sum of the corresponding signals. Beam current is simply the sum of the 4 electrode signals. With this sum the beam current difference to a preceding BPM is calculated. After integration the beam current difference is compared with a threshold which gives the DCM functionality.

### *FPGA Design*

A Spartan-6 FPGA from Xilinx is used for the digital part. The FPGA is mounted on a small PCB by Trenz electronic [6].

This FPGA module has more than 100 I/O pins available for the user. This allows to build a system without designing a multilayer PCB and it is available with FPGA's of different size.

The FPGA design is completely written in VHDL and has two main parts, the central signal processing and a System-On-Chip (SoC). The SoC is used for status readout, system control, debugging and maintenance.

The design functionality is checked with two methods. Every design module in the FPGA was simulated and stimulated by a test bench and the results were checked with the design requirements. Selected modules are tested direct on the FPGA. Direct testing is done by loading stimuli data into the internal RAM, processing this data and reading the results back to the host PC (Hardware in the loop simulation). The results are checked with different tools like Python or MathCad.

The SoC manages the communication between a lot of interfaces. As common interfaces were used UART, SPI, I²C and GPIO known from microcontrollers. Debug memory, the debug system controller and the error trace memory have special interfaces. Of course functional interfaces to the BPM and DCM signal processing also exist.

External interfaces with very different speed and protocol requirements are:

- The direct user interface with a display and push buttons
- The connection to the machine interlock system
- Beam difference current transmission for DCM functionality
- SCADA (ProfiNET)
- A high speed interface for fast control loops (like beam position stabilization)
- USB to a host PC (only for maintenance)

An elegant solution was developed for the beam current transmission. Plastic optic fibre (POF) transmitters give a cheap, isolated connection. As reliable transmission protocol an 8b/10b code with 10 Mbit/s is used. This coding is easily done in FPGA hardware. Other interfaces and tasks are realized in software.

The software runs on a 32 Bit Zylin soft CPU (ZPU) with GNU Compiler Collection support [7]. The ZPU is not known for fast data transfer or as number cruncher, but it is very small, device independent and does the job very well. The development and adaption of algorithms is easy and fast because the ZPU is programmable with standard C. On the ZPU runs a scheduler, which calls necessary tasks like SCADA communication and processes all other user interaction with the system.

All internal modules are connected by a bus system. This simplifies the design of modules and their integration into the system. The software accesses the modules by memory mapped I/O. On system startup all modules are initialized and checked for integrity.



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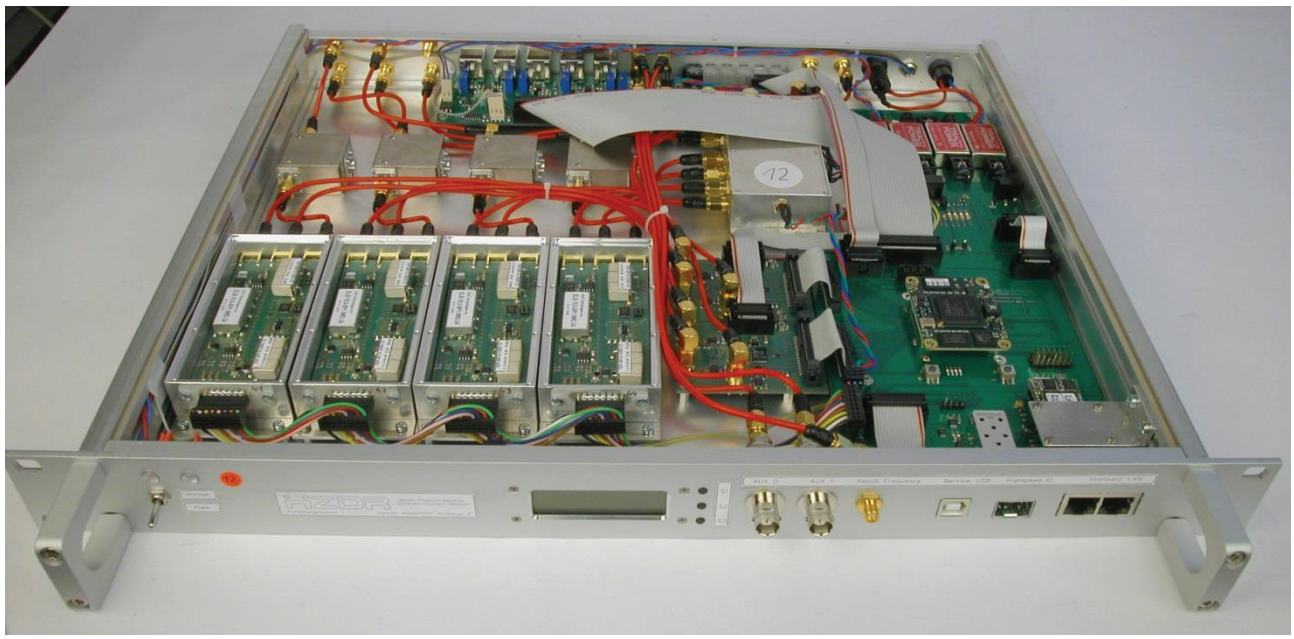

Figure 5: New BPM/DCM electronics.

### *Interpolation Filter*

To fulfil the sampling theorem a multirate FIR interpolation filter is used before digital to analogue conversion. The reconstruction filter is based on several "raised cosine half-band filter" stages. The filter was optimized for the time domain and uses only simple rational coefficients – the most "complicated" coefficients are 7/32 and 21/16. It converts the sampling rate up to 406 kSPS. The conversion rate together with the interpolating CIC-filter implemented in the DAC is 64 to 6.5 MSPS. The overall -3 dB frequency is 17.3 kHz (roughly 1/6 of the original sampling frequency) with more than 65 dB alias band rejection. The rise time is 20.8 µs with 1.0 % overshoot and 204 µs delay. This is sufficient fast compared to the beam signals. The beam response times are determined by the control loop bandwidth of the ELBE superconducting cavities.

### *DAC*

For compatibility and quick service reasons all results are converted to analogue signals. This is done with 7 DACs – 5 for the outputs at the back and 2 for the outputs at the front of the BPM. The DACs have 16 Bit resolution and operate with 6.5 MSPS. The DAC sampling rate is increased by 16 with an internal interpolating CIC-filter. The main advantage of it is the reduction of the serial I/O speed to 6.5 Mbit/s. Because of the digital interpolation filter and the high sampling rate only a simple RC-filter is needed to do the remaining analogue filtering.

## SUMMARY AND OUTLOOK

A new BPM for the ELBE accelerator was developed. It solves the bunch mode dependency problem inherent in the old BPMs and DCMs and gives a huge improvement in dynamic range. The implemented DCM functionality reduces the system costs.

At the end of September 2013 the first 15 new BPMs will go in operation. Altogether the use of 50 new BPMs is planned. In next summer shut down the old BPMs and DCMs shall be completely replaced by the new ones. This helps to operate ELBE better and safer.

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