# A LEADING-EDGE HARDWARE FAMILY FOR DIAGNOSTICS APPLICATIONS AND LOW-LEVEL RF IN CERN'S ELENA RING

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*Abstract*

The CERN Extra Low ENergy Antiproton (ELENA) Ring is a new synchrotron that will be commissioned in 2016 to further decelerate the antiprotons transferred from the CERN's Antiproton Decelerator (AD).

The requirements for the acquisition and treatment of signals for longitudinal diagnostics are very demanding, owing to the revolution frequency swing as well as to the digital signal processing required. The requirements for the Low-Level Radio-Frequency (LLRF) system are very demanding as well, especially in terms of revolution frequency swing, dynamic range and low noise required by the cavity voltage control and digital signal processing to be performed. Both sets of requirements will be satisfied by using a leading-edge hardware family, developed to cover the LLRF needs of all synchrotrons in the Meyrin site; it will be first deployed in 2014 in the CERN's PSB and in the medical machine MedAustron.

This paper gives an overview of the main building blocks of the hardware family and of the associated firmware and IP cores.

## INTRODUCTION

CERN's Extra Low ENergy Antiproton (ELENA) ring [1] is a new synchrotron with a circumference of 30.4 m that will be commissioned in 2016 to further decelerate the antiprotons coming from CERN's Antiproton Decelerator (AD). Table 1 provides a summary of ELENA's main parameters.

Table 1: ELENA Main Parameters

| Parameter | Injection | Extraction |
|---|---|---|
| Momentum, MeV/c | 100 | 13.7 |
| Revolution frequency, MHz | 1.06 | 0.145 |
| Expected number of particles | $3 \cdot 10^7$ | $1.8 \cdot 10^7$ |
| Number of extracted bunches | 4 (operationally) | |
| $\Delta p/p$ of extracted bunches [95%] | $2.5 \cdot 10^{-3}$ | |
| Emittance (h/v) at extraction, $\pi \cdot$mm$\cdot$mrad, [95%] | 6/4 | |
| Extracted bunches length, m/ns | 1.3/300 | |

ELENA's main task is to increase the number of antiprotons available to the experiments by reducing the particles lost during the post-AD deceleration. Furthermore, the beam emittances will be reduced by an electron cooler. Figure 1 gives a schematic view of the ELENA cycle. Its duration is expected to be of at least 20 seconds. The main actions performed in the cycle, namely bunched beam for deceleration when RF is ON and electron cooling on two plateaus, are also indicated.

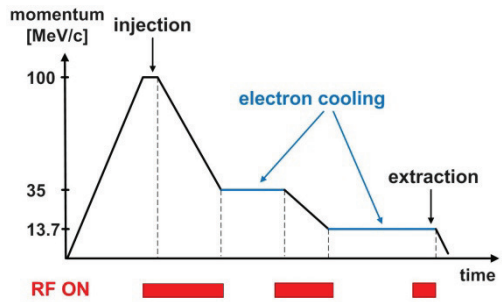


Figure 1: Schematic view of the ELENA cycle.

The ELENA Low-Level Radio-Frequency (LLRF) system will be implemented by using a leading-edge hardware family developed for CERN's small synchrotrons. Features implemented will include phase, radial and extraction synchronisation loops. A double-harmonic voltage operation is envisaged and the LLRF will implement cavity voltage and phase loops. The acquisition and data treatment for longitudinal diagnostics will be implemented by the same family, for the baseline solution [2] as well as for a novel method [3].

ELENA is a very challenging machine. The wide revolution frequency $f_{REV}$ sweep requires a special sampling frequency treatment. The synchrotron frequency can reach a few kHz thus calling for a high beam phase loop bandwidth. All noise sources in the cavity drive chain must be minimised so as not to excite the beam. The required cavity voltage dynamic range is 86 dB, ranging from 25 mV to 500 V. The combined dynamic of the bunched and Schottky beam signals is of 115 dB. The digital signal processing to be implemented is very demanding and the execution time allowed very short (the expected sampling period for the LLRF loops is 5 µs). Several boards have to collaborate and interact in real time to carry out the required processing, since the functionality and number of inputs required cannot be taken care of by a single board.

## OVERVIEW

This new hardware family described in this paper, developed by CERN's RF Group, is an evolution of that successfully operational in CERN's Low-Energy Ion Ring (LEIR) since 2006 [4]. The building blocks are conceptually the same, but differences exist in the actual hardware and software implementation. The new family is based upon the VME Switched Serial (VXS) [5] enhancement of the VME64x standard, which supports switched serial fabrics over a new, high-speed P0

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connector. The VITA57 standard FPGA Mezzanine Card (FMC) [6] is used for the daughtercards. Many of the selected components, such as the motherboard's Virtex 5 FPGAs and the daughtercards' 16-bit ADCs and DACs, are amongst the most advanced units on the market. The analogue signal acquisition and generation, and associated processing, is clocked by an RF clock which as a programmable high harmonic of $f_{REV}$. A revolution "TAG" (single or double) marks each turn and guarantees phase synchronism between all boards in the system. The RF clock harmonic is changed within each cycle to maintain its frequency in the 60 to 120 MHz range; the changes are synchronised via a double TAG.

The main benefits of using a digital system are its full, remote and cycle-to-cycle controllability; built-in diagnostics and extensive signal observation capabilities are also important characteristics. Its digital nature grants an excellent repeatability as well as the implementation of extensive archiving capabilities; this will allow recalling previously-validated sets of control parameters [7].

The hardware family provides a very high processing power, is compact, flexible and modular. Before being deployed in ELENA, this family will be commissioned in 2014 in the CERN's PS Booster (PSB) and in the medical synchrotron of MedAustron [8] to implement their LLRF systems. It will be then retro-fit to CERN's LEIR LLRF to standardise the LLRF implementation across machines. Figure 2 shows the two-board LLRF tests system installed in CERN's PSB during the 2012-13 run.

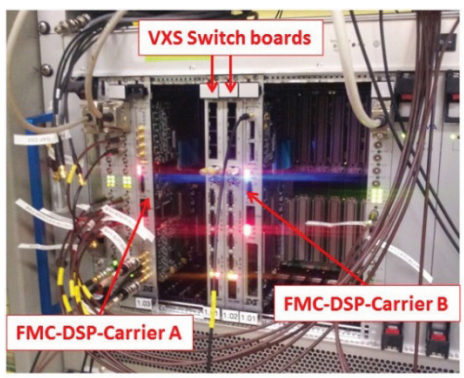


Figure 2: Two-board LLRF test system installed in CERN's PSB during the 2012-2013 run.

## HARDWARE

### *VXS Switch Board*

The VXS Switch board allows using the VXS fabric to interconnect boards via full-duplex Giga-bit serial links. Each VXS crate is fitted with two Switch boards each positioned at a starpoint, called "A" and "B" allowing full routing of a total of eight full-duplex links of up-to 3.125 Gbit/s between any payload slots. The Switch boards also implement a multi-cast capability that is being used to distribute RF Clock and Tag across the VXS fabric. Figure 3 shows the interconnect structure.

The VXS Switch board is also compatible with ELENA's new B-train distribution protocol, based upon White Rabbit [9]. Under this scheme, the B-train information is sent to the VXS-DSP-FMC Carrier board that requires it via a spare full-duplex channel.

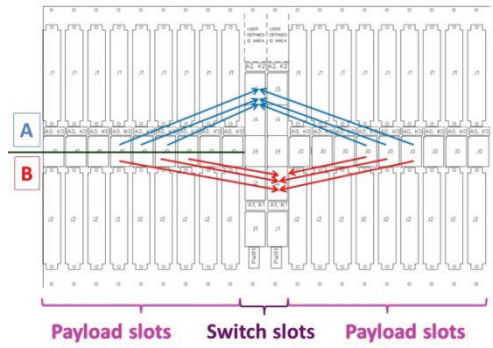


Figure 3: VXS interconnect structure obtained with two Switch boards.

### *VXS-FMC-DSP-Carrier Board*

The VXS-DSP-FMC Carrier board is a 6U unit board carrying a SHARC Digital Signal Processor (DSP) ADSP-21368 and two Xilinx Virtex 5 Field Programmable Gate Arrays (FPGAs), referred to as Main FPGA (XC5VLX110T) and FMC FPGA (XC5VSX95T). The former is the hearth of the communication; the latter, optimised for digital signal processing, controls the FMC hardware and implements the required data treatment.

Two dedicated full-duplex VXS channels from each Carrier board routing to Switch board B distribute RF clock and TAG. The other six full-duplex VXS channels, bonded to form three 32 bit data paths, are used to transfer 10b8b-encoded data between Carrier boards at a raw link rate of 2 Gbit/s or 100 MSPS (32 bit). Each Carrier board can host up to two FMC daughtercards with a high-pin count format. The Carrier board also includes several memory banks for observation purposes. In particular, two, 4Mx18 bit banks are clocked at 100 MHz and two, 1Mx4x18 bit banks are clocked at the RF clock frequency. Figure 4 shows a functional overview of the Carrier board.

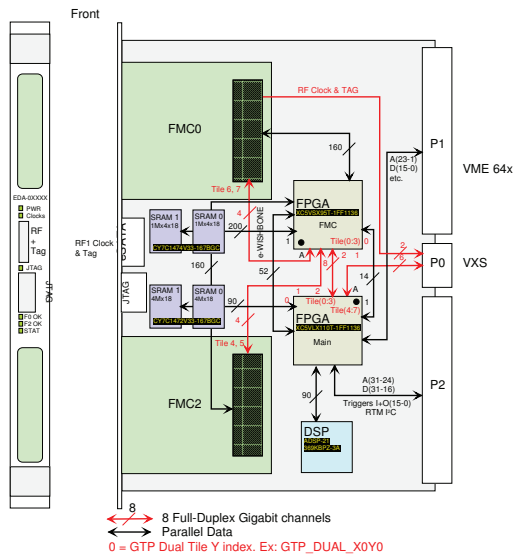


Figure 4: VXS-DSP-FMC Carrier boards overview.



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### *Rear Transition Module (RTM)*

The RTM is the VXS-DSP-FMC Carrier's companion board. Installed in the rear side of the VXS crate and interfaced to the Carrier via the J2/P2 connector, it carries all major secondary power supplies needed by the Carrier. The RTM front panel provides sixteen general purpose digital inputs and eight general-purpose digital outputs using stacked LEMO 00 connectors. The digital inputs can be configured as high impedance of TTL 50 Ohm. These are directly interfaced to the Main FPGA. An $I^2C$ bus, driven from the Main FPGA, is used to control the RTM LEDs, the input impedance and to interface with the RTM power manager.

### *FMC Modules*

There are three types of daughtercards, namely the Direct Digital Synthesizer (DDS), the Analogue-to-Digital Converter (ADC), and a Digital-to-Analogue converter (DAC) FMC modules.

The DDS FMC daughtercard uses the AD9858 IC as the DDS core; it is a high quality, compact clock generator, featuring two independent channels synchronised to the same reference and allowing up to 232 mHz frequency step resolution.

The ADC FMC daughtercard uses an AD9286 ADC and includes four independent digitisation channels with up to 125 MSPS of 16 bits resolution. Its analogue front-end, based on the LT6409 IC, provides signal conditioning with DC coupling, low noise, low distortion and a controllable gain switching of 18 dB, corresponding to 3 LSBs. The measured wideband spurious-free dynamic range exceeds 70 dB, the signal-to-noise ratio exceeds 74 dB thus allowing 12.5 equivalent number of bits. Figure 5 shows the ADC FMC; a scale in centimiters at the bottom of the picture underlines the small daughtercard size.

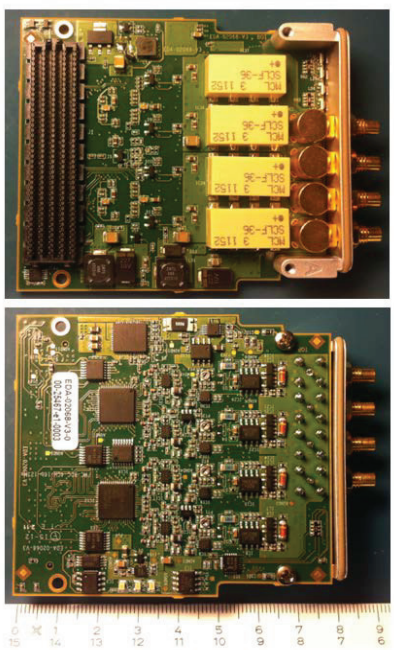

Figure 5: ADC FMC top (above) and bottom (below).

The DAC FMC daughtercard is based on the AD9747 IC and allows four independent digital-to-analogue conversion channels with 16 bits resolution in the conversion and programmable gain switching of 18 dB. The output is DC coupled, with a 40 MHz analogue bandwidth and a full scale, peak output voltage of 3.6 V. The sampling rate of the DAC mezzanine can go up to 250 MSPS and the front-end, like the ADC board, includes low distortion and low noise electronics.

ADC and DAC FMC daughtercards provide features such as voltage/temperature monitoring, precise board identification with a silicon ID chip, EEPROM for storing board specific information, namely the FMC family type, the version number and the current level. In addition, ADC and DAC FMC both are equipped with a DAC (for the ADC FMC) and an ADC (for the DAC FMC) to carry out an automatic offset compensation.

## SOFTWARE

### *Main FPGA*

The firmware running on the Main FPGA implements the essential infrastructure for the system communication and data exchange. Several communication channels are implemented, such as: a) VME64x (A32/D32); b) DSP (A16/D32); c) Carrier-to-Carrier (VXS full-duplex dual 32 bit link with a transfer rate of 100 MHz); d) communication and data exchange with the FMC FPGA (full-duplex 32 bit Gigabit links); e) $I^2C$ link to control the RTM configuration and LEDs; f) $I^2C$ link to control the board front-panel LEDs; g) $I^2C$ to control the VXS Switch module; h) $I^2C$ links to exchange IPMI [10] information with the FMC FPGA. The communication architecture is configured such that no arbitration is required on any of the link nor bus interfaces for simplicity and overall system reliability.

The same firmware implements other capabilities, such as; a) a dual, 128 channel timing generator, b) 16 channels, 32 bit x 1024 vector function generators; c) 48 channels, 32-bit x 2048 programmable digital signal observation. The firmware allows remote updating of FPGA and DSP software. Finally, numerous diagnostics functions are available. The firmware will be the same for all boards; the capabilities will be enabled or disabled through controls depending on the desired board function.

### *FMC FPGA*

The FMC FPGA is optimised for DSP resources and implements the custom FMC hardware control and data treatment. Digital signals observation will be possible via configurable buffers clocked at the RF clock and located in the fast memory on the Carrier board.

The code in the FMC FPGA is customized to the actual FMC hardware via the instantiation of FMC IP cores. Each daughtercard is complemented by an FPGA IP core running on the FMC FPGA. These IP Cores are developed in independent version-controlled libraries through a collaborative design. The FMC FPGA common firmware is held in a separate library; the FMC FPGA

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design instantiates the required IP Cores in each slot. An overall "VHDL compile and generate" creates the customized FMC FPGA source. Separate logic Synthesis and Place & Route projects are used for each IP Core configuration to allow using specific constraints. Figure 6 shows the IP-cores instantiation in the FMC FPGA.

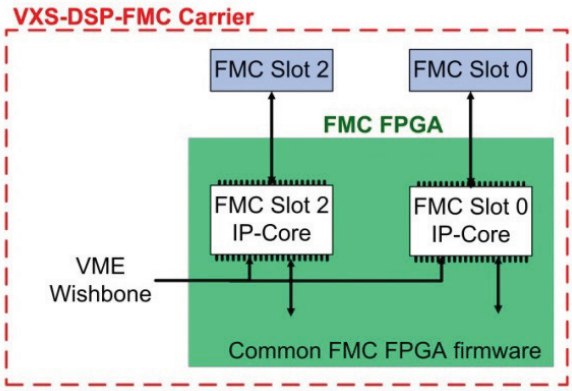


Figure 6: IP-cores instantiation in the FMC FPGA.

The *ensemble* FMC daughtercard and corresponding IP core implements the functionality of a of Master Direct Digital Synthesizer (MDDS) for the DDS FMC, a Digital Down Converter (DDC) for the ADC FMC and a Slave Direct Digital Synthesizer (SDDS) for the DAC FMC.

The MDDS generates a clock that clocks all daughtercards at a high $f_{REV}$ harmonic. The TAG signal synchronises in phase all DDC and SDDS channels in the system. The encoding protocol allows transferring both the RF clock and the tag as two separate signals over optical fiber (AC-coupled fabric). This will be especially useful for the implementation of system described in [3], since its crate might be about 200 m distant from the LLRF system. Figure 7 shows the implemented RF clock and TAG encoding.

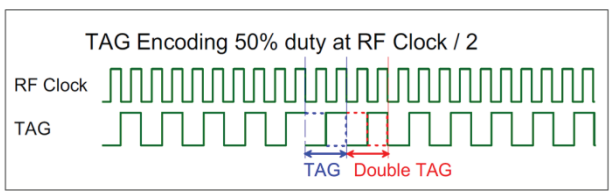


Figure 7: RF clock and TAG encoding.

The DDC daughtercard performs digitisation, low-pass filtering and decimation, thus greatly increasing by digital signal processing the ADC equivalent number of bits.

The SDDS generates RF analogue signals of programmable $f_{REV}$ harmonic and phase, as well as fully-programmable noise. Data acquisition and control are done in {I,Q} coordinates.

### *DSP*

The DSP code is developed in C language as interrupt-driven; it does not make use of a real-time operative system owing to the strict time constraints required. The DSP code implements the core data treatment functionalities, such as the beam and cavity control loops for the LLRF, thus fully exploiting its floating point processing capabilities.

The DSP code will entirely depend on the functionality of the board hosting the DSP itself and will allow the full system customisation. An advantage of this approach is the short time required to compile the code and download it into the hardware, as opposed to that required by a complex FPGA. This will minimise the downtime due to code modifications during machine studies.

### *Development and Test Support Tools*

Several Python scripts have been developed to carry out interactive, automatic or overnight tests of the various boards. This has been a great advantage for the pre-series validation/characterisation in the laboratory and is going to be an essential tool when testing the series production.

A toolset [11] for memory map management and automatic driver generation has also been developed by CERN's BE/RF group. The toolset allows the creation of memory maps for all interfaces involved and the generation of VME software driver definitions, VHDL register banks and DSP header files.

## CONCLUSIONS

A leading-edge hardware family is under development at CERN to address the LLRF needs of several CERN;s synchrotrons. After being deployed in machines at CERN and abroad, it will be used for the LLRF and for the longitudinal diagnostics implementation in the ELENA ring. This hardware family provides very high processing power by making advanced use of FPGA and DSP resources. Furthermore, it is compact, flexible and modular. Its planned wide-spread use will allow for an easier maintenance and a better spares management.

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