DESIGN AND BEAM TEST RESULTS OF BUTTON BPMS FOR THE EUROPEAN XFEL*

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Abstract

The European X-ray Free Electron Laser (E-XFEL) will use a total of ~300 button BPMs along the whole accelerator, and additionally 160 cavity BPMs. The pickups for the button BPMs have been designed by DESY, whereas the electronics has been developed by PSI. This paper gives an overview of the button BPM system, with focus on the RF front end electronics, signal processing, and overall system performance. Measurement results achieved with prototypes installed at the DESY FLASH linac and at the SwissFEL Injector Test Facility (SITF) are presented. The position noise obtained with button pickups in a 40.5 mm aperture beam pipe is as low as ~11 μm at 20 pC bunch charge.

INTRODUCTION

The E-XFEL 17.5 GeV superconducting linac and undulator will employ different types of BPMs [1]. At locations where sub-micron resolution is needed, e.g. in undulators or few locations in the warm beam transfer lines, cavity BPMs are chosen [2][3]. In other parts of the machine, more cost efficient button BPMs are preferred, e.g. in warm beam transfer lines, or the cold superconducting cryostats where ~70 button BPMs are complemented by ~30 re-entrant cavity BPMs.

For the standard BPMs the beam pipe apertures are 40.5, 94, and 78 mm depending on the location. Nominal bunch charges range from 0.1 to 1 nC. The BPMs must be able to measure position and charge of single bunches with 220 ns spacing, in trains of up to 2700 bunches, repeated at 10 Hz. Train-by-train averaged rms position resolution must be better than 10 μm, bunch-by-bunch resolution better than 50 μm. The same values apply for hourly and weekly drifts, respectively. The range for maximum resolution is ±3 mm. Monotonicity must be guaranteed over ±10 mm. Identical electronics should be used for all ~300 button BPMs. These requirements do not allow to re-use BPM technology previously available at PSI or DESY, therefore calling for new developments.

BUTTON BPM SYSTEM

The E-XFEL button BPM electronics consists of four main blocks:

- Button pickups: The beam position sensor pickups use four capacitive electrodes (buttons). The ratio of signal amplitudes among the electrodes is related to the transversal beam position.
- RF front end with RF/analog electronics (RFFE): Four channels, each with RF pulse-stretching filter, amplifiers and step attenuators, diode detectors and hold capacitors, discharger, baseband buffer. An on-board pulser enables self-testing and linearization.
- Analog-to-digital converter (ADC) module: Base–band signals are digitized simultaneously with 12-bit resolution at sampling rates up to 500 MSa/s.
- Digital back end: The general purpose digital platform "GPAC" provides generation of timing signals, processing of ADC waveforms, position and charge calculation, and interfacing to other accelerator subsystems.

The pickups have been developed by DESY, while the electronics and firmware/software were developed at PSI.

Button Pickups

For the standard BPMs, button BPMs were chosen over alternatives such as striplines, due to their lower costs and compact design [4]. Their simpler geometry is also better suited to the particle cleanliness requirements of the superconducting machine. See photos in Fig. 1 below.

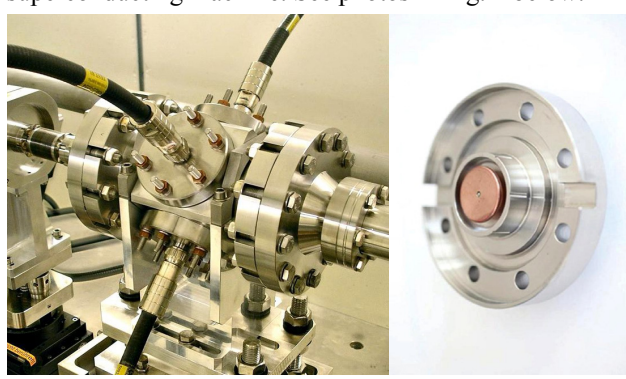

Figure 1: Cold button pickup mounted at SITF and copper button electrode.

The button is designed to increase the signal level and avoid resonances up to the upper bandwidth limit of the electronics (2.7 GHz) by optimizing the button pickup geometry. The reflections at the feedthrough should be small and the transmission high to avoid loosing signal level and depositing energy in the vacuum insulator. Additionally, the cold button pickup must withstand a few temperature cycles between 2 and 300 K. The cold buttons consists of copper to minimize the heat loss from higher order traveling modes of the nearby accelerator.

Beam position is calculated from the pickup electrode voltage magnitudes v_i as shown in Fig. 2, which is a first-order approximation, valid close to the center of the beam

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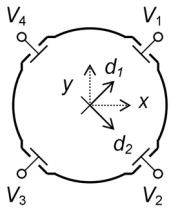
pipe. A lower pickup geometry factor k [mm] implies higher position sensitivity and lower BPM position noise.



$$d_1 = k\,\frac{v_1 - v_3}{v_1 + v_3}$$

$$d_2 = k\,\frac{v_2 - v_4}{v_2 + v_4}$$

Figure 2: Button pickup electrode configuration (beam is into paper) and calculation of measured beam position.

For the cold button pickup in 78 mm aperture pipe the button diameter is 20 mm and the geometry factor 17 mm. For the warm button pickup in 40.5 mm aperture pipe the respective numbers are 16 mm and 11 mm. A measure for charge sensitivity or absolute signal level is the fraction of beam image current that crosses a button. When the beam is centered this is ~8.0 % for the cold and ~12.7 % for the warm button. The expected charge limited position noise of the cold button is 2.7 times worse than for the warm.

RF Front End

The purpose of the RFFE is to convert the pickup signals to a signal suitable for the digitizers, while preserving relative amplitude information. Due to its proven performance and simplicity, the concept of linear filtering and peak detection is employed.

An RFFE contains four RF/analog channels on a VME card, allowing parallel processing of all four electrode signals per pickup (as opposed to time-domain multiplex–ing). Fig. 3 shows the block schematic of one out of four identical channels.

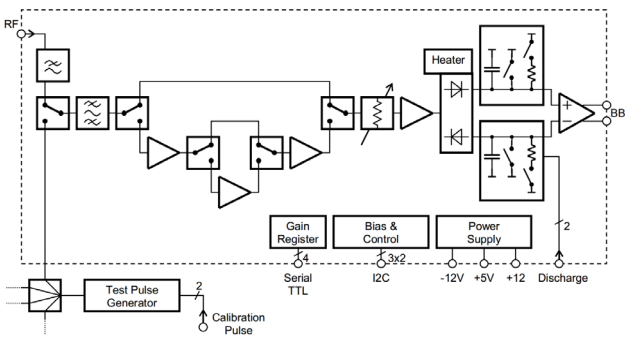


Figure 3: Block diagram of a single RFFE channel.

Pickup signals arrive through the RF inputs. A first low pass filter removes undesired spectral components above 2.7 GHz to protect the first switch from the extremely high pickup signal spikes. It also suppresses parasitic modes of the pickup, i.e. slot resonances in the circular gap around the buttons and resonances of the beam pipe.

A switch serves to select between the pickup signal and the on-board test pulser. Test pulses are generated by an avalanche transistor, and split equally to all channels. They have a duration of ~300 ps full-width half-max, an amplitude equivalent to a ~2 nC bunch, and the frequency spectrum is similar to the beam signal of a button pickup. The pulser is used for in-situ self-tests and for character-ization of the detector transfer functions.

The test pulser switch is followed by a chirp filter with a bandpass frequency range from 1.5 to 2.3 GHz, realized as add-on PCB in stripline technology (see Fig. 4). This filter has a dispersive phase response to stretch the resulting signal pulse, which relaxes the requirements of the subsequent amplifiers and detector. While pulses coming from the button have sub-nanosecond duration, the chirped pulses have a 3-dB envelope width of ~8 ns, and significantly lower signal amplitude. Compared to a resonant pulse stretcher, the chirp filter preserves more pulse energy and has a finite-duration response. The pulse stretching reduces the linearity requirement of the amplifiers and allows the detector circuits to acquire the signal over a longer period of time. The filter also cuts out the desired part of the pickups's broadband frequency spectrum and rejects the machine RF of 1.3 GHz and harmonics thereof.

A variable gain stage in front of the peak detector allows adapting the analog gain to the beam charge. It combines three selectable gain paths (20 dB steps) with a 31.5 dB range step attenuator (0.5 dB steps).

The gain stage is followed by a temperature-stabilized balanced peak detector (Avago HSMS-282C). It detects the signal amplitude and holds the value in capacitors.

A high-speed differential buffer, having high input impedance and 50 Ohm output impedance, drives the balanced baseband (BB) output of the RFFE. Because the difference signal produced by the detector is unipolar (pulse height is between 0 and 2 V), the buffer adds a difference mode offset to match the ADCs differential input voltage range (±1.15 V). It also adds a common mode offset to comply with the ADCs input bias voltage (+450 mV on each phase). The balanced baseband signal is fed to the dc-coupled ADC via two coaxial cables.

Resetting the detector is done by discharge switches across the hold capacitors, controlled by the FPGA of the digital back end. Additionally, switchable resistors across the hold capacitors provide control of the droop rate (self-discharge), allowing operation in two modes as shown in Fig. 7: a) High self-discharge, without activating the discharge switches, since the discharge resistors prevent signal pile-up over successive bunches; b) low droop rate, with discharge switches activated by the FPGA for each bunch. Mode a) can be used when the bunch arrival time is unknown (self-triggering), e.g. during accelerator com-missioning. Mode b) will be used for standard operation of the BPM to achieve higher performance, resulting from the larger signal and jitter-insensitive sampling.

All RFFE functions and adjustment parameters are remotely controlled via digital interface. Supply voltages, currents, and temperatures can be monitored. The board supports live insertion. A non-volatile memory provides storage for calibration data.

Photographs of the RFFE board are shown in Fig. 4. The board was designed in a VME64x from factor (233 x 160 mm^2). RF and BB connectors are located on the front panel, power supply and user defined control I/O on the

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bus connectors. Using a modular approach for the critical circuits (calibration pulser, chirp filter, detector, and discharger/buffer) allows modifying these circuits without having to replace the whole board.

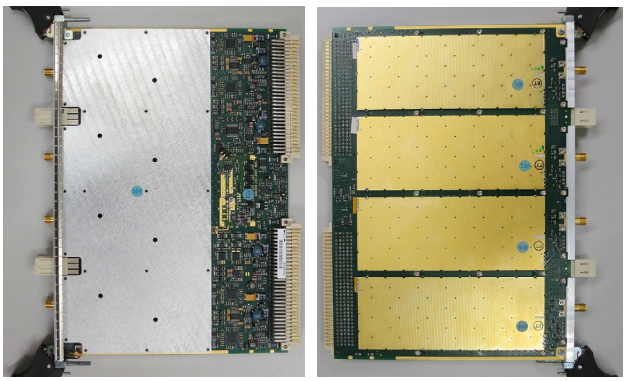

Figure 4: RFFE board. Top side (left) with shield on RF/analog sections; bottom side (right) with stripline filters.

Analog-to-Digital Converter

The ADCs are mounted on piggyback modules on the GPAC digital carrier board. Each module has eight 12-bit 500 MSa/s ADCs (Intersil KAD5512P). Tests confirmed 10.5 bits effective resolution for 10 MHz sinusoidal input signals, and 9.5 bits for 500 MHz. The module is shown in Fig. 5. Its size is 85 x 145 mm^2.

ADC clocks can be derived from either an externally supplied reference or from an on-board oscillator. A PLL can synthesize the ADC clock from a wide range of input frequencies and clean jitter from noisy input references. A clock splitter features adjustable delays for each channel.

The ADC module also provides timing signal outputs for the RFFE's test pulser and discharge circuits. Differential signaling and coaxial cables are used for the connections to and from the RFFE.

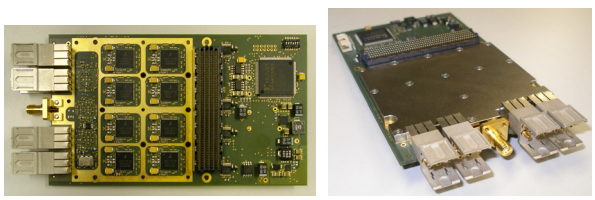

Figure 5: 8-Channel 500MSa/s ADC piggyback module.

Digital Back End

The setup of digital electronics consists of one GPAC board and two ADC mezzanine cards as a generic digital platform developed by PSI and described in [5]. With two ADC piggyback modules the digital carrier board can serve up to 16 signal channels or four button BPMs.

A block diagram of the GPAC is given in Fig. 6. The SYS FPGA handles communication between the machine control system connected to one of the external interfaces (VME bus or SFP fibre optic link), and all other FPGA chips. The digital processing of the ADC signals is done in the two BPM FPGAs (Xilinx Virtex-5). The BP FPGA provides interfacing via backplane to the RFFE boards.

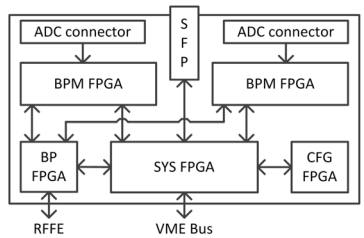

Figure 6: Block diagram of GPAC board.

Triggering

The system can operate with an external trigger or self-triggered. In self-triggered mode, the trigger is derived internally from the waveforms recorded by the ADCs, independently for each BPM. The self-trigger algorithm involves summation of the four signals, differentiation, threshold checking, and peak detection. The self-trigger fires at the instant when the edge speed of the sum of the input signals exceeds a threshold and is maximum.

SIGNAL PROCESSING

Pulse Height Analysis

The digitized waveforms are analyzed to find the pulse heights (see Fig. 7). First the position of the rising edge is determined. Then, a number of samples are picked just before the edge and averaged to give the "baseline" value. Also, a number of samples are picked just after the edge and averaged to give the "top" value. The difference of the two is the pulse height used in subsequent processing.

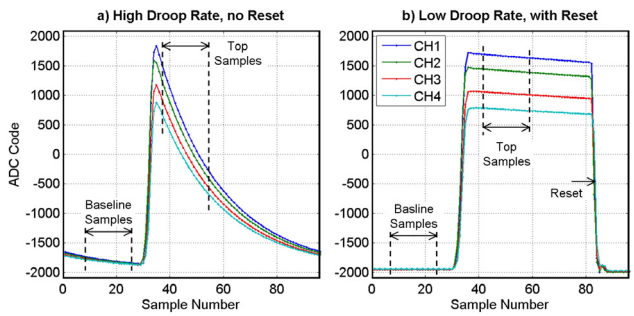

Figure 7: Digitized waveforms of one bunch (433 MSa/s).

Detector Linearization

The RFFE channels have differing gain and non-linear transfer characteristics, leading to large systematic errors in measured beam positions if the beam is far off-axis.

To correct these errors, a model that accounts for channel gain, detector threshold and curvature is used for each channel. The models are calibrated by using the on-board test pulser to simulate equal pickup signals at each RF input, and the step attenuators to sweep the level.

During BPM operation, the inverse models are applied to correct the above described systematic errors. The implementation is table-based for numerical efficiency and low latency. The applied linearity correction doubles the detector's usable dynamic range to a ratio of 5:1.

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Position and Charge Calculations

The measured beam position is calculated by applying equations in Fig. 2 to the linearized baseband voltages. If the electrodes are arranged diagonally as shown in Fig. 2, the resulting vector must be rotated by 45°.

The beam charge is proportional to the sum of the linearized baseband voltages. Charge measurement must be calibrated by comparison to a dedicated charge sensor.

Firmware/Software Implementation

The digital signal processing is implemented in FPGA firmware in VHDL supplemented by C software in a PowerPC processor on the same FPGA. The functional topology is shown in Fig. 8. The lower three blocks form a computation pipeline which process raw ADC data and deliver calibrated position and charge values. The pipeline is triggered with every bunch. The QDR II SRAM block is an interface to off-chip memory, used to store the ADC waveforms for off-line analysis. The DDR2 SDRAM block stores position and charge values of every bunch. Data from both memories is accessible by the PowerPC and/or the accelerator control system.

The PowerPC executes high level procedures between subsequent bunch trains or in off-line mode. It also controls the RFFE boards (gain control, bias voltage correction, monitoring), and handles the model fitting and table generation for detector linearization.

The Timing Control block performs trigger detection. It also synchronizes the computation pipeline, memory acquisition, and generates interrupts to the processor.

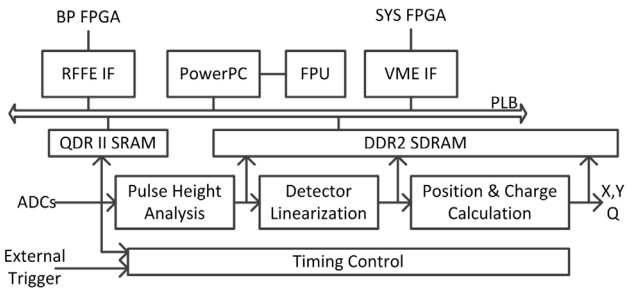

Figure 8. Block diagram of firmware in BPM FPGA.

TESTS

In 2012, a complete E-XFEL button BPM system was first tested with beam at SITF/PSI. These tests used the more challenging cold button pickup (and 25 m long pickup cable), with single electron bunches rather than bunch trains. The resolution obtained with the present BPM electronics was <5 µm rms at 90 pC, which is about ten times better than the minimum requirement. The improved performance is highly beneficial for the new E-XFEL operation modes at low bunch charges down to 20 pC, or at even lower charges during commissioning.

After single bunch tests at PSI, tests with trains of up to 400 bunches were performed at the FLASH linac at DESY with a warm button pickup. The pickup signals were split to two RFFEs, as shown in Fig. 9.

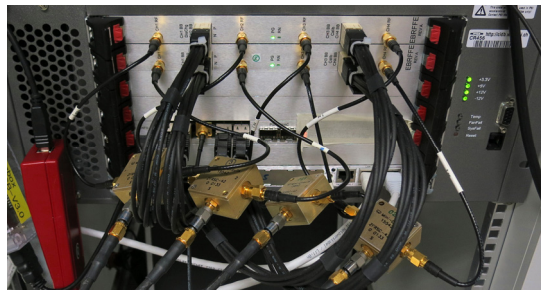

Figure 9: Test crate with two RFFEs, a GPAC and ADC.

Bunch-by-bunch position and charge rms noise for 200 bunch trains and effective bunch charges Q_B from 4.5 to 55 pC (accounting for the signal split) are shown in Fig. 10. Measured values are marked by circles. The straight lines represent $\sigma = a/Q_B$, with parameter a chosen to match measurements below 20 pC. The charge limited position noise is $a = 200$ pC·µm. Above 50 pC, the position noise settles at 5.5 µm, and the relative charge noise at 0.35 ‰.

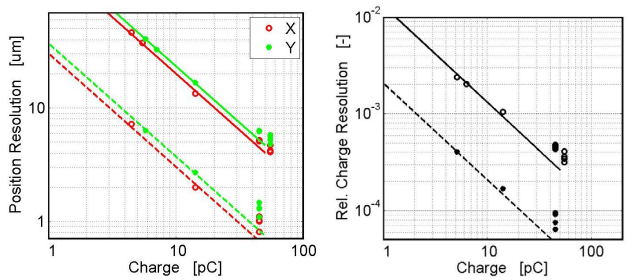

Figure 10: Measured position and relative charge resolutions vs. bunch charge. Solid: bunch-by-bunch; dashed: train-by-train (averaged over 40 bunches per train).

CONCLUSIONS

We presented the design and first tests of the E-XFEL button BPM system. Tests conducted at the PSI SwissFEL Injector Test Facility and DESY FLASH were successful and proved that the BPM hardware and software/firmware work as expected so far. The most critical performance parameter, the position resolution at low charge, safely exceeds E-XFEL requirements. Further tests of resolution at higher charge, linearity, and drift are ongoing at SITF.

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