NEW DESIGN OF THE 40 GHz BUNCH ARRIVAL TIME MONITOR USING MTCA.4 ELECTRONICS AT FLASH AND FOR THE EUROPEAN XFEL

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Abstract

At free-electron lasers, today's pump-probe experiments and seeding schemes make high demands on the electron bunch timing stability with an arrival time jitter reduction down to the femtosecond level. At FLASH and the upcoming European XFEL, the bunch train structures with their high bunch repetition rates allow for an accurate intra-train stabilisation. To realise longitudinal beam-based feedbacks a reliable and precise arrival time detection over a broad range of bunch charges, which can even change from 1 nC down to 20 pC within a bunch train, is essential. Benefitting from the experience at FLASH, the current bunch arrival time monitors, based on detection of RF signals from broad-band pick-ups by use of electro-optic modulators, are further developed to cope with the increased requirements. In this paper, we present the new BAM prototype, including an adapted electro-optical front-end and the latest development of the read-out electronics based on the MTCA.4 platform.

INTRODUCTION

The bunch arrival time monitor (BAM) detects the time at which an electron bunch passes an RF pick-up and compares it to a femtosecond precise reference. This is given by timing stabilised laser pulses of the optical synchronisation system, as in permanent operation at FLASH [1]. At this FEL user facility, five BAM systems are currently installed, reflecting different design stages due to an on-going development over the past 4 years. It has been shown, that the BAMs in their current state achieve an intrinsic measurement resolution of below 10 fs for bunch charges above 300 pC [2]. These monitors are currently subject to further improvements, in order to cope with the raised demands associated with the amendment of FLASH [3] and with the upcoming European XFEL. The goal is to not only achieve a robust and reliable monitor system as a standard diagnostic device for FELs, but to also provide a high measurement resolution across a broad range of bunch charges, i.e. as low as 20 pC and up to 1 nC and above.

FLASH also provides the possibility to test new hardware and software for the European XFEL. Up to ten BAM stations are planned to be installed at the European XFEL, (see Fig. 1). Most of the BAMs will be included into the longitudinal, intra-train feedback (ITFB) system together with bunch compression and beam energy monitors. The ITFB uses beam-based information from every bunch, i.e. arrival time, compression and energy, to add corrections to the LLRF regulation acting onto the RF field which is fed into the accelerating cavities. At FLASH, a reduced timing jitter of the bunches to well below 25 fs behind the last accelerating module has already been achieved [4].

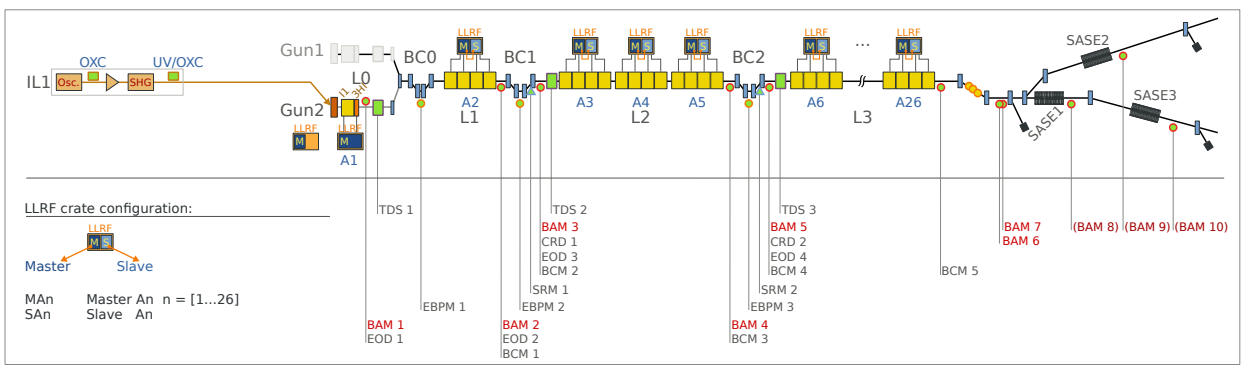

Figure 1: Schematic of the European XFEL with locations of the longitudinal diagnostics. Besides the BAMs, there are also: bunch compression monitor (BCM), energy beam position monitor (EBPM), electro-optical diagnostics (EOD), transverse deflecting structure (TDS), coherent radiation diagnostics (CRD) and synchrotron radiation monitor (SRM).

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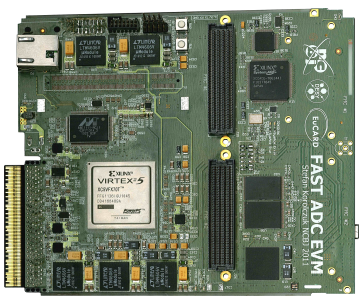
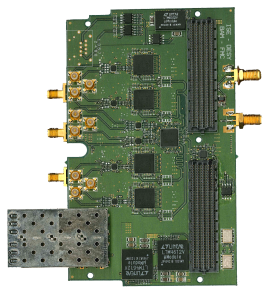


(a) Prototype FPGA based dual FMC carrier board.



(b) Prototype dual FMC mezzanine card.

Figure 2: Photographs showing the new MTCA.4 BAM electronics, with (a) the prototype of the DAMC-FMC25 carrier board and (b) the prototype of the DFMC-DSBAM FMC mezzaniane board.

In addition to the BAMs that are incorporated into the ITFB, five more locations are foreseen for BAM installations at the European XFEL, two behind the main linear accelerator, *L3*, and three in the different branches of the undulator sections, named *SASE1* to *SASE3* in Fig. 1. Besides delivering the bunch timing information to the user experiments, they could also provide valuable information on timing drifts and jitter performance of the facility infrastructure. In this case, it is foreseen to install two identical BAMs, *BAM6* and *BAM7* (Fig. 1), next to each other for out-of-loop and correlation measurements. The destinctive feature of this setup is that one of those BAMs will be connected through a 1.9 km link to the master laser-oscillator, located close to the injector, whereas the other identical BAM will be connected via a 1.5 km link to the slave laser-oscillator, located in the experimental hall, for details see [5].

GENERAL LAYOUT OF THE BUNCH ARRIVAL TIME MONITOR

The arrival time monitor system consists of three main parts: RF front-end, electro-optical (EO) front-end and electronics for read-out and control.

RF Front-End

The RF pick-up of the original BAM design provides a bipolar voltage signal with a bandwidth from DC up to 10 GHz. This leads to a limited performance for small bunch charges due to a too low amplitude and slope, as shown in [2]. Two years ago, a new pickup with a higher bandwidth, from DC up to 40 GHz, has been developed [6] and installed at FLASH for first tests. Since the required RF components and cables have a considerably high attenuation at such high frequencies, the pick-up design has been further optimised to compensate for those losses. The expected peak-to-peak voltages from this pick-up at a bunch charge of 20 pC is up to 4.5 V_{pp} with a slope of 300 mV/ps [7]. Those pick-ups will provide the capability to reach the projected resolution of 10 fs also for bunch charges well below 300 pC.

Electro-Optical Front-End

The central component of the EO front-end is the electro-optical modulator (EOM) which translates the voltage signal into an amplitude modulation of the pulsed optical signals. It is difficult to find suitable EOMs on the market which not only allow to use the full RF bandwidth of up to 40 GHz but which can also cope with the short laser pulses (around 1550 nm) with 200 fs to 500 fs FWHM and up to 46.3 pJ pulse energy. There are modulators available with different substrate materials, such as $LiNbO_3$, InP, GaAs and thin film polymer on silicon (TFPS). In a comparative study in a laboratory test set-up, summarised in [8], the most promising candidate has been found to be a TFPS modulator from *GigOptix* [9], which offers a low operation voltage (V_π), smaller than 3 V, with a high EO bandwidth of up to 35 GHz and small dependance of the modulation on the optical wavelength. This is important for applications with pulsed signals. Further tests with actual pick-up signals from the electron bunches are scheduled to be performed at FLASH in late 2013.

Electronics

The existing readout electronics for the BAMs at FLASH, described in [10], is based on the VME standard and is limited by the available computational resources. One of the major limitations was to transfer all data collected during a 2 ms accelerator RF pulse and process it during the 98 ms time window (10 Hz repetition rate at FLASH). It occurred that this task could not be completed and data from the previous pulse was still being transferred when the new pulse was coming. In such cases, data from the new pulse could not be recorded, but was simply dropped. In the worst case, about 80 % of the events were lost. Another inconvenience of the VME based system is that it has no hot-swap capability, i.e. power cycling

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of the entire crate is required, whenever a hardware change is made, which affects all devices in the crate, also those which are working correctly.

DESIGN OF NEW BAM ELECTRONICS IN MTCA.4 STANDARD

To solve the issues related with the VME system, it has been decided to upgrade the BAM readout electronics to the MTCA.4 standard. Instead of a parallel (multi-drop) bus, shared between all boards in the crate, MTCA provides a backplane with different point-to-point connections between particular units, such as AMC boards or to the MicroTCA Carrier Hub (MCH). Thus, a failure of one device will not affect communication between others, as it could happen in case of the VME. Those connections are optimised to handle serial protocols such as PCI Express, Gigabit Ethernet, Serial ATA, Serial RapidIO, and many more. Except faster communication, MTCA provides a much more reliable environment, where all components (boards, power supplies, fans) are remotely managed and hot-swap capable.

Like in the previous generation of BAM readout electronics, a single device is made out of two parts: the base board with digital electronics, and a mezzanine board with analogue and optical input circuits, depicted in Fig. 2. The base board has been designed as a MTCA dual FMC carrier, while the optical inputs with the analogue part have been implemented as a dual FMC mezzanine card. The versatile FMC carrier board, DAMC-FMC25, was developed at DESY in MTCA.4 standard [11].

The base board is equipped with a Virtex-5 FPGA, which is the main data processing device. In addition to this, the board also has a second FPGA dedicated to do common board management tasks, such as Virtex-5 firmware upgrade and clock signal management. Thus, the Virtex-5 can fully be utilised for data processing. The carrier board is equipped with many diagnostic devices, a Module Management Controller (MMC) which is responsible for handling IPMI communication with the MCH in the crate, several on-board voltage and temperature sensors as well as a USB-Serial interface. All of these devices are foreseen to provide flexibility and ease of use during both, firmware or software development and in permanent installation.

The mezzanine board, schematic shown in Fig. 3, is equipped with a clock distribution chip and with four 16-bit ADCs. The board has three optical inputs, each with a photodiode of about 800 MHz bandwidth. One of those is used as a source of the clock signal, and the other two receive the data signals. Each data signal is then split and attached to two ADCs, which are sampling the same signal with a small difference in phase between each other, such that the relative height of the laser pulse can be measured by sampling both, the peak of the laser pulse and its baseline. The main task of the clock distribution chip is shifting the phase of the clock signals for the individual ADCs. Further details can be found in [12].

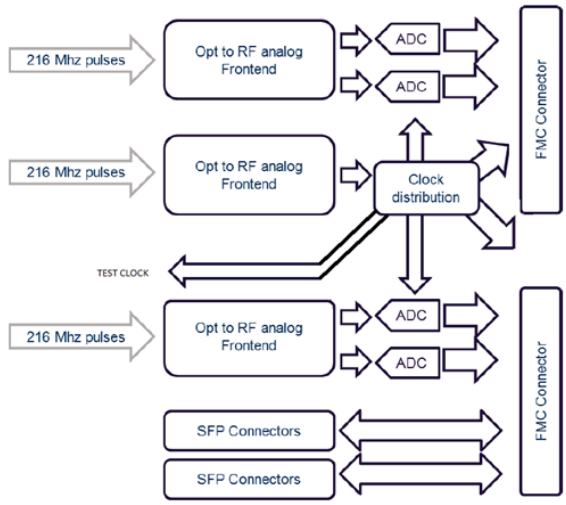

Figure 3: FMC mezzanine card block diagram.

In comparison to the VME based system where 125 MSPS ADCs had been used, the new ADCs can sample signals with a maximum frequency of 250 MSPS. The laser pulses from the optical synchronisation system at FLASH have a repetition rate of 216.7 MHz. Thus, the VME based system was able to only measure every second pulse. The new design will read and analyse all of the incoming laser pulses, which is a big advantage.

FIRST MEASUREMENTS WITH THE PROTOTYPE BOARD

The prototype MTCA board (carrier and mezzanine), shown in Fig. 2, has been used to perform initial measurements of the pulse shape from the 216.7 MHz repetition rate laser after passing the analogue electronics. It has been measured in two setups: first, the output of the photodiode has been sampled with an oscilloscope and, second, with the on-board ADCs of the new system. In the latter case, the pulse shape has been retrieved by measuring one sample per laser pulse and shifting the phase between data and clock signal.

The phase shift was done in two ways: for the precise short range shifting, the built-in *fine delay* blocks in the clock distribution chip have been used, and for wide range adjustments the optical delay length in single-mode fibre has been changed. The on-board phase shifting covered the range of up to 1 ns with over 32 steps. The data of the laser pulse shape, as plotted in Fig. 4, was collected from several individual measurements. A total optical path length of 80 cm was covered by subsequently adding short fibre parts, and in between, short range phase sweeps were performed. For each measurement point, 1024 samples have been collected in the FPGA memory and used for calculation of standard deviation (STD) and mean values.

At the flat regions of the baseline and at the peak of the pulse, the STD was below 10 ADC counts. With the covered range of 24766 ADC counts, this gives a sampling pre-

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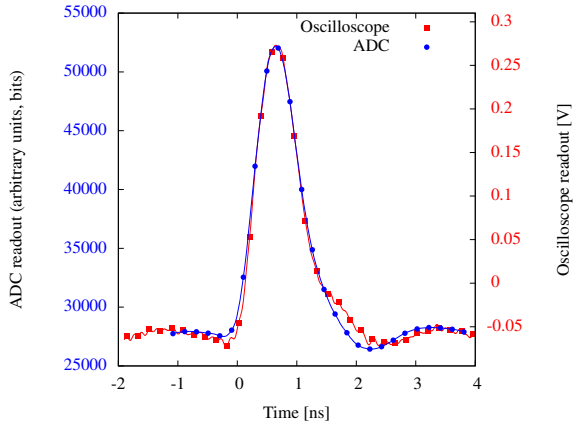

Figure 4: The plot shows the mean values from 1024 subsequent laser pulses measured with the oscilloscope and onboard ADCs.

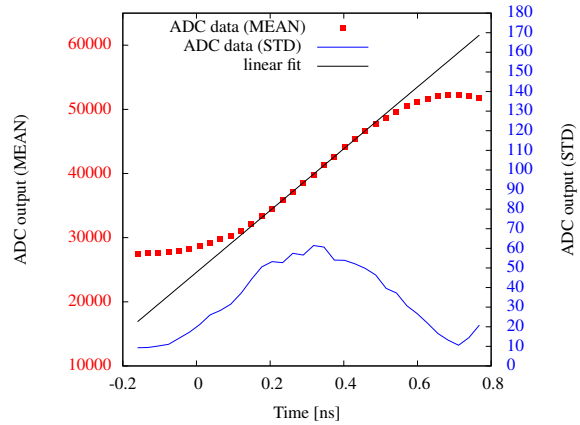

Figure 5: Measurement of the clock jitter contribution during a phase sweep with 1 ns range.

cision of $10/24766 \cdot 100\,\% = 0,04\,\%$. On the rising and trailing edges of the pulse, the STD amounts to 85, which is a precision of $0.34\,\%$. In the last case, the major contribution to the STD comes from the clock jitter, introduced by the clock distribution chip *AD9516-4* from *Analog Devices*. According to the datasheet, an additive jitter from 0.5 ps to 3.8 ps RMS is expected, depending on the parameter settings of the *fine delay* blocks.

The contribution of that chip to the STD of the ADC trace has been estimated from the collected data. The plot in Fig. 5 shows only the rising edge (from Fig. 4) with a linear fit applied to it, $y = 47704.78$ ns/bit$\cdot x + 89281.46$ bit, for a time calibration. The minimum value of the STD (from signal noise mostly) is about 10, and is located on the flat areas on baseline and peak of the pulse. The maximum value of the STD (from the noise and jitter) is located at the middle of the slope with values up to 60. Concerning this, the jitter contribution to the STD is about 59. Using the time calibration, a timing jitter of $\delta\tau = \mathrm{STD}_{\mathrm{jit}}/47704$ (ns/bit) results in a $\delta\tau$ of about 1.24 ps, which fits to the value from the datasheet.

CONCLUSION

The BAMs at FLASH are subject to on-going improvements, especially with regard to the upcoming European XFEL. This concerns the central components of all three parts of the BAM system. In this paper, we present first measurements with the prototype of the new electronics, comprising carrier and FMC mezzanine board in MTCA.4 standard. Further investigations are scheduled to evalutate their performance in comparsion to the old system. As soon as the fully functional final version is available, one complete system will be installed at FLASH for firmware and server development with actual BAM signals. Until end of 2014, it is scheduled to upgrade all of the existing BAMs at FLASH to the new design.

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