HIGH-POWER TESTS AT CESRTA OF X-RAY OPTICS ELEMENTS FOR SUPERKEKB

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Abstract

X-ray beam size monitors at SuperKEKB must withstand high, sustained incident power loads. Two prototype optics elements were fabricated and tested at CesrTA, using incident X-ray power densities comparable to those expected at the SuperKEKB LER. One element was based on a silicon substrate, the other a CVD diamond substrate, with each substrate supporting a coded aperture mask pattern in gold on its surface. The diamond substrate mask showed superior performance to the silicon substrate mask, with the the mask pattern on the silicon substrate melting at the highest incident power level tested, where the diamond-substrate mask survived. We will present here the high-power test results, along with a simulation of X-ray power absorption and heat transfer in the two prototype elements, and the resulting implications for the design of the optics, beam line and heat sink for SuperKEKB.

INTRODUCTION

X-ray beam size monitors will be used at SuperKEKB to measure low-emittance bunch profiles in both the Low Energy Ring (LER) and High Energy Ring (HER).[1][2] The total beam currents in the LER and HER will be 3.6 A and 2.6 A respectively, which creates a high average SR power load on the optics elements. Two types of prototype optics elements (URA masks[3]) have been fabricated and are being used for both imaging tests and high-power burn tests at CesrTA. The latter tests are described here.

Table 1: Mask Parameters

Parameter	Silicon mask	Diamond mask
Substrate material	625 μm monocrystalline silicon	350 μm polycrystalline CVD diamond
Buffer material	5 nm Cr	100 nm Cr
Mask material	18.75 μm Au	8.7 μm Au
Mask pattern	31 x 5 μm URA	59 x 10 μm URA

The two types of mask tested are described in Table 1. The first type tested, made by NTT-AT Nanofabrication, was made of 18.75 μm-thick gold on a 625 μm-thick silicon substrate. To prevent the gold layer from peeling away from the silicon due to differences in thermal expansion coefficients, there is a 5 nm buffer layer of chromium between the gold and silicon. There is no chromium in those parts of the mask pattern where there is no gold. The second type of mask, made by Cornes Technology, is made of 8.7 μm gold on a 350 μm CVD diamond substrate, with a 100 nm Cr buffer layer.

BURN TESTS

The burn tests were carried out at the CesrTA D Line, using 5.3 GeV beam. In the first test carried out, the silicon-substrate mask was exposed to 200 mA of beam (corresponding to the heat load expected at the LER) for approximately 5 minutes, after which it was removed from the beam line and examined, as shown in Fig. 1; at this stage, it appears completely unharmed.

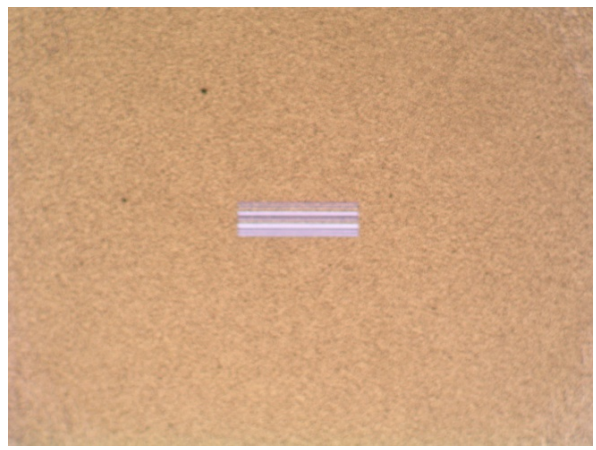

Figure 1: Au+Si mask after exposure to 200 mA beam.

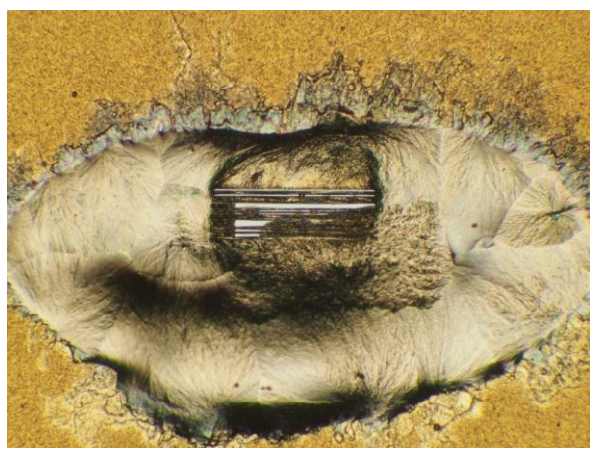

Figure 2: Au+Si mask after exposure to 243 mA beam.

To determine what margin of safety there may be, the same mask was re-installed in the beam line, and exposed to ~20% higher beam current, 243 mA. Figure 2 shows the result of this second burn test. The gold coating in the

ISBN 978-3-95450-127-4

center of the chip has melted and slumped down. The Si substrate appears to be intact, and the Cr bonding layer between the gold and the silicon appears to be still attached to the Si. The center of the mask evidently reached at least the melting temperature of gold (1064°C), but not that of silicon (1414°C), or chromium (1907°C).

Following this somewhat alarming result, a similar test was conducted on a prototype diamond-substrate mask. A factory-reject sample was used, with scratches and displaced traces. Photos of the Au+CVD diamond mask before and after exposure to beam currents up to 243 mA are shown in Fig. 3. No obvious damage resulting from the beam exposure is seen.

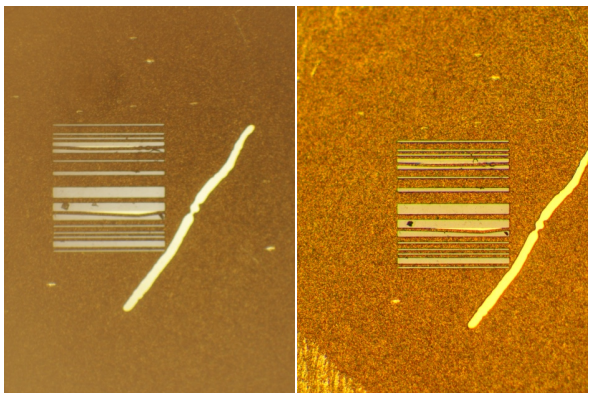

Figure 3: Au+CVD diamond mask (factory-reject) before (left) and after (right) exposure to 243 mA beam.

The 5.3 beam current was raised in steps, with beam image scans taken through the mask after each step at 4 GeV, as shown in Fig. 4. No change in the beam image through the mask is seen between the scans taken after exposure to 60 mA (left) and 243 mA (right) 5.3 GeV beam.

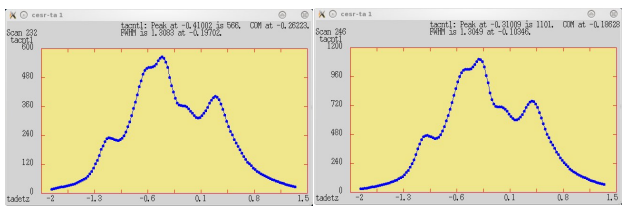

Figure 4: Beam image scans taken through Au+CVD diamond mask (factory-reject) after exposure to 60 mA (left) and 243 mA (right) beam.

From the photographs and beam image scans, the Au+CVD diamond mask would appear to have survived the exposure to the maximum beam heat load possible at CesrTA.

The superiority in high-power applications of the diamond-substrate mask over the silicon-substrate, due to the higher thermal conductivity of diamond than that of silicon, was clearly demonstrated.

SIMULATIONS

ANSYS simulations were carried out to replicate the burn test results, and to evaluate how much margin is gained by using a diamond-substrate mask. The mask is mounted flush with a copper heat sink plate with a 2.38 mm diameter hole in it, through which synchrotron radiation is incident on the mask. A stainless steel mounting bracket is used to hold the mask in close thermal contact with the copper heat sink, and the bracket is mounted with stainless bolts that pass through the copper plate. The assembly is water cooled at the center of the top surface. A drawing of the holder assembly is shown in Fig. 5; the simplified model of the assembly used in simulation is shown in Fig. 6.

The total incident power on the mask and its holder was calculated according to $P[W/mr/A]=13.8E_e^4[GeV]/\rho[m]$ (Ref. [5], Eq. 3.39, e.g.), and modeled as a heat source on the surface of the mask and holder in the form of a horizontal ribbon with a vertical width corresponding to the projection of the critical angle at the mask's distance from the source.

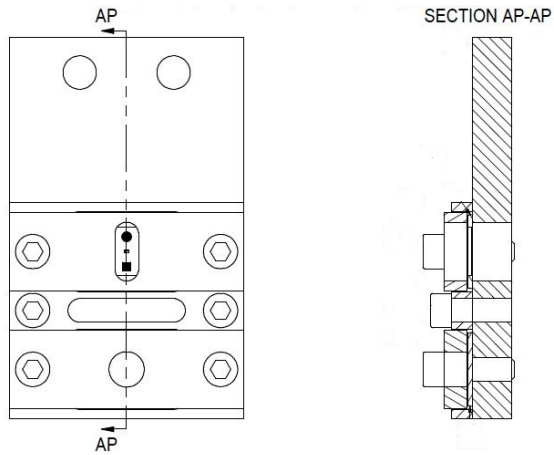

Figure 5: Heatsink mount for coded aperture at CesrTA.

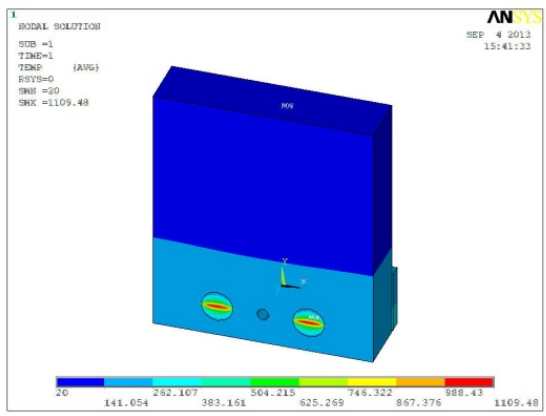

Figure 6: ANSYS simulation of temperature distribution over simplified model of heatsink mount.

For the simulation, we used the temperature-dependent thermal conductivities of the mask and holder materials from the AIST material properties database [6]. The thermal conductivity data for diamond are only available up to 400°C, so we fit the data (for the sample in the database with the lowest thermal conductivity) to an inverse power law in degrees Kelvin, and extrapolated the

ISBN 978-3-95450-127-4

thermal conductivity data out to 1500°C, following the model of phonon-phonon scattering dominance for thermal conductivity dependence in that regime [7].

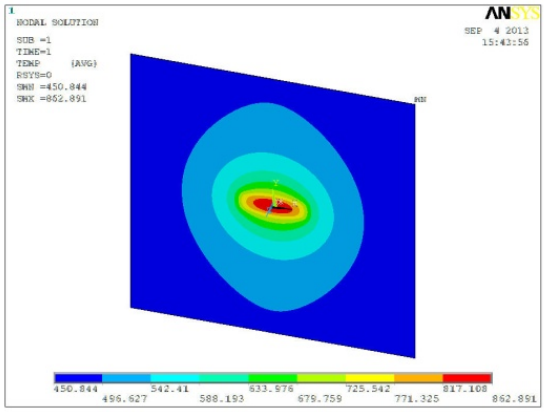

Figure 7: ANSYS simulation of temperature distribution of gold layer on silicon substrate.

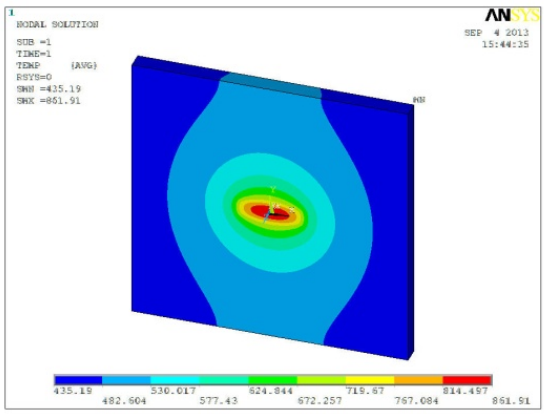

Figure 8: ANSYS simulation of temperature distribution of silicon substrate behind gold layer.

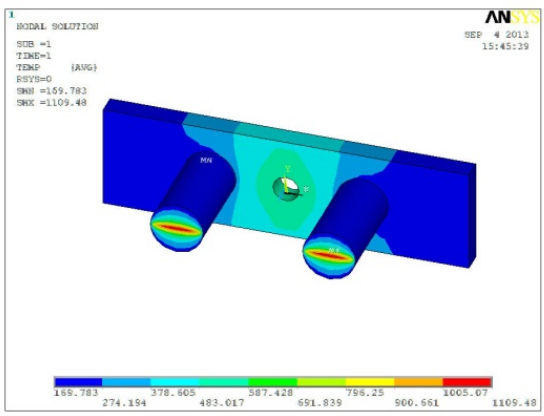

Figure 9: ANSYS simulation of temperature of stainless steel retaining bracket behind substrate, and bolts.

Figure 7 shows the temperature distribution of the gold layer of the Au+Si mask for an incident SR power equivalent to 243 mA at 5.3 GeV at CesrTA. Figure 8 shows the temperature of the underlying Si substrate, and Fig. 9 shows the temperature distribution over the stainless steel retainer bracket and mounting bolts. Finally, Fig. 10 shows the temperature of the gold layer of the Au+CVD diamond mask under the same incident heat load.

The peak temperature of Au on the Si substrate reaches 863°C, close to melting temperature of Au of 1064°C. The peak temperature of the Au on the CVD diamond substrate, on the other hand, is 327 degrees lower at 536°C. As mentioned previously, the actual Au+Si mask must have reached a peak temperature between 1064°C and 1414°C. If the actual Au+Si mask temperature was near the upper bound of 1414°C, then from the difference in peak temperatures the Au+CVD diamond mask peak temperature might have come quite close to the melting temperature of gold.

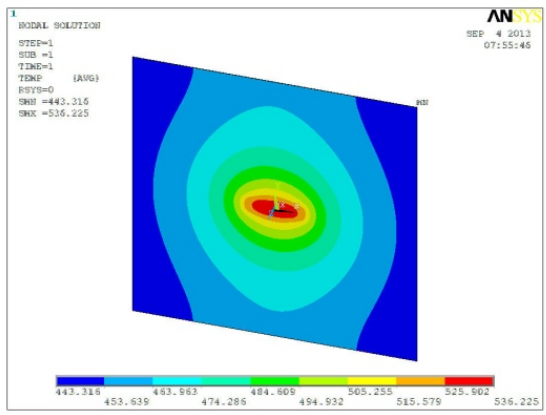

Figure 10: ANSYS simulation of temperature distribution of gold layer on diamond substrate.

EFFECT OF HEAT-SINK SHIELDING

Based on the above results, we simulated the effect of placing a slotted screen in front of the mount, to prevent SR power from being absorbed outside the mask aperture and raising the base temperature of the copper heat sink mount. The results are shown in Table 3. Placing a slotted shield in front of the holder so that the SR fan hits only the mask and not the copper heat sink lowers the peak temperature a further ~200-300 degrees.

Table 3: Maximum Au Temperature Reached in Simulation

Design	Silicon mask	Diamond mask
Unshielded heat sink	863°C	536°C
Shielded heat sink	586°C	352°C

In addition to lowering the temperature of the mask itself, such shielding also keeps the stainless steel bolts, which otherwise reach peak temperatures of 1100 degrees under direct exposure to SR, from excessive temperature build-up.

ISBN 978-3-95450-127-4

LESSONS AND PLANS FOR SUPERKEKB

Table 3 shows a summary of SR heat loads for the burn tests conducted at CesrTA, and those expected for the SuperKEKB LER and HER. Two types of heat load are shown: the on-axis solid-angle power density in W/mr^2/A (calculated as per Ref. [5], Eq. 3.13 and following), and the line power density as described above. Their projections onto the mask in terms of peak W/mm^2, and integrated W of linear power, respectively, are also shown. For the LER, while the maximum beam current is much higher than that at CesrTA, the lower beam energy and greater distance to the optics mount gives an area power density the same as that seen at CesrTA at 200 mA, 23 W/mm^2. Based on the burn test, this should be an acceptable power density for the LER.

Table 3: X-ray Beam Line Heat Loads at CesrTA and the SuperKEKB LER and HER

Parameter	CesrTA		SuperKEKB		
	D Line		LER	HER	
Energy (GeV)	5.3		4	7	
Bend radius (m)	31.65		31.74	106	
On-axis solid-angle power density (W/mr^2/A)	2,357		560	2,807	
Line power density (W/mr/A)	345		112	313	
Distance from source to optics box (m)	4.549		9.39	10.27	
Aperture width (mm)	2.38		0.5	0.5	
Current (A)	0.200	0.243	3.6	2.6	
Be filter thickness (mm)	0	0	0	0	14
Zero-degree area power density (W/mm^2)	23	28	23	69	23
Integrated line power density over aperture width (W)	36	43	21	41	13
Si burn test result	PASS	FAIL	--	--	--
Diamond burn test result	PASS	PASS	--	--	--

For the HER, the area power density is three times higher at 69 W/mm^2. In order to lower the area power density at the HER to same level as the LER, 1.4 cm of Be filter material need to be placed upstream of the optics mount. Such a filter is also needed to keep the maximum area power density on a beam stopper, which will be placed just upstream of the optics mount, below the limit specified by the manufacturer (25 W/mm^2).

For the mask substrate the Au+Si mask should be acceptable during the early commissioning period, but for better safety margin at full currents (and to allow for possible increases in heat load in the future), a CVD diamond substrate mask should be used. The mask tested here was polycrystalline; for even better thermal conductivity, a monocrystalline CVD diamond substrate mask is also under development.

A slotted shield, with a horizontal aperture width of 500 μm, will be placed in front of the optics mount to prevent unnecessary temperature rise.

SUMMARY

We carried out burn tests at CesrTA on prototype x-ray optics chips for SuperKEKB. Using an incident power intensity equivalent to that maximum nominally expected at the SuperKEKB LER, we verified that both the silicon-substrate mask and the diamond-substrate mask survive exposure to the beam. When the incident power was raised 20%, however, only the diamond-substrate chip survived, demonstrating the expected superiority of the diamond-substrate mask in this application.

In order to increase the margin of safety further, we found in simulation that it is effective to have a slotted shield in front of the holder to prevent SR power absorption in the area of the heat sink around the mask. In addition, a 1.4-cm Be filter is needed at the HER to lower the incident area power density to the level expected at the LER, and demonstrated to be acceptable at CesrTA.

In addition, a monocrystalline CVD diamond substrate mask is under development, which should have even better heat conductivity than the polycrystalline one tested at CesrTA.

ACKNOWLEDGMENTS

We would like to thank Jim Shanks for his assistance in getting the beam tuned for the beam test, as well the CHESS and CesrTA operators for their assistance.

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ISBN 978-3-95450-127-4