SYNCHRONISATION OF THE LHC BETATRON COUPLING AND PHASE ADVANCE MEASUREMENT SYSTEM

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Abstract

The new LHC Diode ORbit and OScillation (DOROS) system will provide beam position readings with sub-micrometre resolution and at the same time will be able to perform measurements of local betatron coupling and beam phase advance with micrometre beam excitation. The oscillation sub-system employs gain-controlled RF amplifiers, shared with the orbit system, and followed by dedicated diode detectors to demodulate the beam oscillation signals into the kHz frequency range, subsequently digitized by multi-channel 24-bit ADCs. The digital signals are processed in each front-end with an FPGA and the results of reduced throughput are sent using an Ethernet protocol to a common concentrator, together with the orbit data. The phase advance calculation between multiple Beam Position Monitors (BPMs) requires that all DOROS front-ends have a common phase reference. This paper presents methods used to generate such a reference and to maintain a stable synchronous sampling on all system front-ends. The performance of the DOROS prototype synchronisation is presented based upon laboratory measurements.

INTRODUCTION

The DOROS system has been primarily designed and optimised for processing beam signals from the beam position monitors (BPMs) embedded into the jaws of the new LHC collimators [1]. The system will provide orbit readings used for the automatic positioning of the collimator jaws symmetrically around the beam, which will reduce the time needed to set-up the collimators and potentially improve the collimation efficiency. The Diode ORbit (DOR) system will be complemented by Diode OScillation (DOS) sub-system optimised for processing the beam oscillation signals. The DOS part will provide data that can be used for the measurement of local betatron coupling and the phase advance between the BPMs with micrometre beam excitation.

The simplicity of the DOROS system and its already proven sub-micrometre orbit resolution [2] made it a good candidate to complement the standard LHC BPM system. This system was designed for bunch-by-bunch trajectory measurements and is limited to an orbit resolution at the micrometre level. The DOROS system will therefore be installed on all BPMs close to the LHC interaction points, where a better orbit resolution will help in optimising the collision process. Electrode signals of these BPMs will be passively split and sent to both systems. This way the standard system will provide bunch-by-bunch beam trajectories while the DOROS will measure precisely beam orbits. In addition, the DOS part of the DOROS system will be capable of providing oscillation data with micrometre beam excitation for betatron coupling and phase advance measurements.

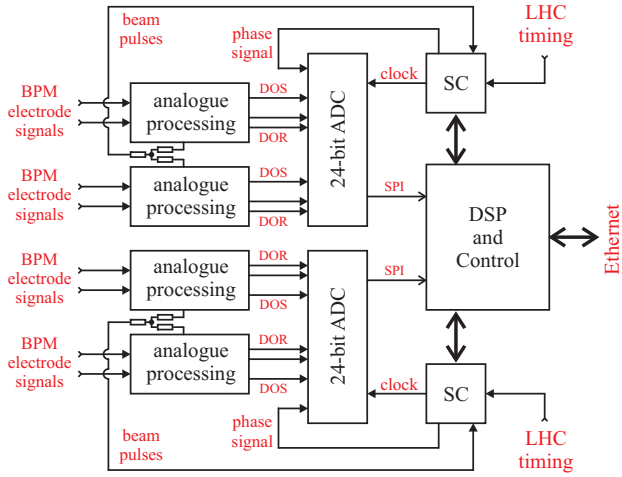

Figure 1: Block diagram of a DOROS front-end. Abbreviations: SC – synchronisation circuits, DOR – diode orbit, DOS – diode oscillation, SPI – serial peripheral interface link.

DOROS SYSTEM

The DOROS front-ends will be built as 1U 19" modules distributed around the LHC. Each front-end is foreseen to process signals from four BPM electrode pairs. Typically it will be up-stream and down-stream BPMs of two collimators or horizontal and vertical electrodes of two stripline BPMs [2]. The block diagram of one DOROS front-end is depicted in in Fig. 1.

The analogue processing channels of each electrode pair provide two low frequency orbit signals (DOR) proportional to the BPM electrode voltages, which are produced by compensated diode detectors [2], and one oscillation signal (DOS), resulting from the difference of the beam oscillation signals demodulated by diode peak detectors. All three signals are low-pass filtered and are digitized by a 24-bit ADC at the rate of the LHC revolution frequency (f_{rev}) of about 11.2 kHz. The subsequent digital signal processing (DSP) of the samples is implemented in an FPGA. The same FPGA provides the system control and timing as well as the Ethernet communication and data transmission to a common DOROS concentrator. The DOROS data transmission uses the same Ethernet protocol and the 25 Hz frame rate as the standard BPM system. The total DOROS data throughput is about 40 KB/s per front-end.

ISBN 978-3-95450-141-0

In general, each LHC beam can have slightly different revolution frequency and therefore the LHC has two networks distributing the beam synchronous timing (BST). Since each DOROS front-end is foreseen to process simultaneously signals from both LHC beams, the digitalisation is done with two ADCs. As seen in Fig. 1, the ADCs are independently clocked with the signals obtained from dedicated synchronisation circuits (SC) blocks, each using an individual timing, which can come from either of the LHC timing networks.

The ADC selected for the DOROS system is of Σ/Δ architecture to obtain the 24-bit resolution and excellent linearity of the conversion. The ADC has been chosen for its very good performance for both DC and AC signals, required for the DOR and DOS systems, respectively. In addition each ADC accommodates 8 simultaneously sampled channels, fitting well to the DOROS architecture.

The DOS sub-system is based on synchronous demodulation of the beam oscillation signals [3] resulted from micrometre beam excitation at a constant frequency f_{exc}, typically chosen close to the betatron frequency f_β, which for the LHC is in the range 3.1 – 3.6 kHz for both horizontal and vertical planes. The oscillation phase advance is measured with respect to a local oscillator (LO) signal having exactly the same f_{exc} frequency as the beam excitation. This LO f_{exc} signal is generated with a direct digital synthesizer (DDS) [3] synchronised to a revolution frequency timing derived from the LHC BST and referred to as timing revolution frequency, f_{revT}. While the frequency of this signal is guaranteed to be the same in each DOROS front-end, it is not the case for its phase. The phase of f_{revT} in a particular DOROS front-end depends on its location around the LHC and the delay of the BST optical fibre link. Therefore, the f_{revT} signal phase must be aligned to the same beam bunch in each front-end, which will be done with a single bunch circulating in the machine. If the timing distribution does not change, in general this alignment needs to be performed once. This paper describes the circuitry and algorithms that will allow a reliable phase synchronisation of the timing f_{revT} derived from the LHC BST, with the focus on the synchronisation circuits accommodated in SC block in Fig. 1. The required accuracy of the phase advance measurements obtained from the DOS data is in the order of 0.1°, corresponding to some 80 ns at 3.6 kHz, the highest frequency at which the phase advance measurements will be typically done. The synchronisation between the DOROS front-ends should preferably be much better, in the order of 8 ns, equivalent to about 0.03° at f_{rev}. The described synchronisation was designed with the aim of achieving at least this accuracy.

SYNCHRONIZATION CIRCUITS

A diagram of the synchronisation circuits is shown Fig. 2. Its first block, a Beam Synchronous Timing receiver (BSTrx), decodes the LHC timing, distributed over fibre optics links from a single timing source. The block provides the bunch frequency f_{RF} (about 40.1 MHz)

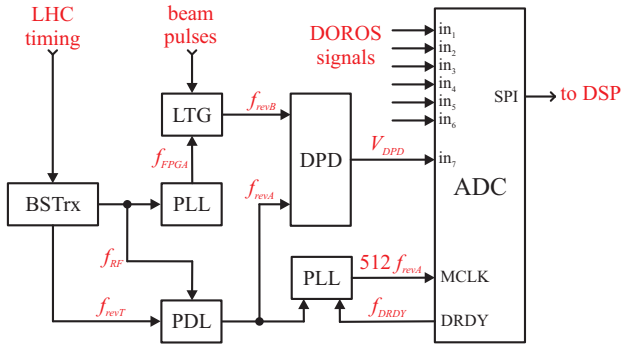

Figure 2: DOROS synchronisation circuits. BSTrx – beam synchronous timing receiver, LTG – local timing generator, PDL –programmable delay line, DPD – differential phase detector, MCLK – master clock, DRDY – data ready signal.

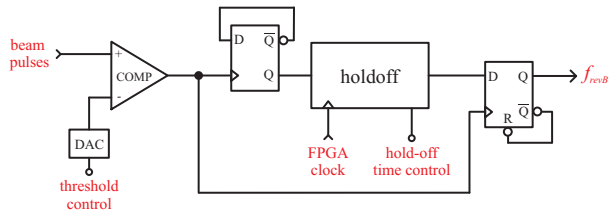

Figure 3: Block diagram of the Local Timing Generator (LTG).

which is multiplied by a factor of four in an FPGA PLL block to produce the FPGA global clock f_{FPGA} (about 160 MHz). The BSTrx block delivers also the earlier introduced timing revolution frequency signal f_{revT}, whose phase can be shifted by a Programmable Delay Line (PDL) to match the phase of the revolution frequency reference f_{revB}, which is derived from the beam pulses. The PDL provides the beam aligned revolution frequency reference f_{revA}, used as a phase reference for the PLL synchronising the ADC sampling signalled by the data-ready (DRDY) pulses. The PLL produce a low-jitter ADC master clock (MCLK), whose frequency is 512 times higher than f_{revA}, that is about 5.8 MHz. The PLL is optimised for low jitter and is based on a classical architecture with a charge-pump phase detector and a voltage controlled oscillator (VCO) built as an LC generator tuned with a varicap diode.

The beam reference f_{revB} is provided by a Local Timing Generator (LTG), synchronised by the beam pulses produced by a passive combination of the processed BPM electrode signals, as sketched in Fig. 1. The phase of the timing f_{revT} and beam f_{revB} signals is compared in a differential phase detector (DPD). This precise phase detector is designed in such a way that its output voltage read by one dedicated ADC channel has a maximum when the both input signals are phase-aligned. During the phase alignment procedure the delay of the PDL is adjusted to obtain a maximum voltage from the DPD.

ISBN 978-3-95450-141-0

This way the phase-match condition does not depend on the input offset voltage of the ADC, which would otherwise cause an important error.

Local Timing Generator

The phase of the revolution frequency reference f_{revT} obtained from the LHC timing system in each DOROS front-end is foreseen to be synchronised with the beam with just one bunch circulating in the machine. However, the Local Timing Generator (LTG), schematically shown in Fig. 3, is designed to provide a beam revolution frequency reference f_{revB} synchronised to the same beam bunch regardless of the actual LHC bunch configuration. The LTG employs an asymmetry in the bunch train and locks to the first bunch following the largest gap in the bunch train. In the case of the physics beam the largest gap constitutes the so called abort gap, a 3 µs period with no bunches, corresponding to the risetime of the LHC dump kicker.

The operation of the LTG is based upon bunch pulses derived from the BPM electrode signals. The pulses are converted into short logic signals by a comparator and stretched in time by the following flip-flop. Once the LTG is already locked, the first bunch after the largest gap triggers the flip-flop generating a short pulse before being auto-reset. The same bunch starts the counter in the holdoff block, resetting also its output, which in turn disables the output flip-flop. The flip-flop gets enabled after the holdoff counter reaches the time falling already in the following bunch gap. The LTG locks to the first bunch after the largest gap when the holdoff time is set as

$$T_{holdoff} = T_{rev} - T_{largest\ gap} + \Delta T \qquad (1)$$

where $T_{rev} = f_{rev}^{-1}$ is the revolution period of about 88.9 µs, $T_{largest\ gap}$ is the time of the largest gap in the bunch train and ΔT is a small interval, typically a few ns.

The operation of the comparator can be optimised by changing its threshold voltage through a dedicated DAC.

Programmable Delay Line

The phase of the timing revolution frequency reference f_{revT} can be shifted with the resolution much better than one FPGA clock using the Programmable Delay Line (PDL), whose block diagram is shown in Fig. 4. The PDL is built from two parts: a raw delay, delaying the f_{revT} reference by a programmable number of f_{RF} clock cycles (25 ns) and a fine delay. The fine delay, which can be programmed in 100 ps steps, employs the feature of an FPGA PLL block, producing a delayed version of the f_{RF} timing, which clocks the raw delay block.

Differential Phase Detector

Since the phase measurement at the 0.01° level cannot be done with the FPGA logic, the measurement is performed with a specially designed Differential Phase Detector (DPD) built from discrete components and shown schematically in Fig. 5, together with simplified waveforms in the key nodes of the circuit. Such a phase detector delivers a DC voltage with the maximum value

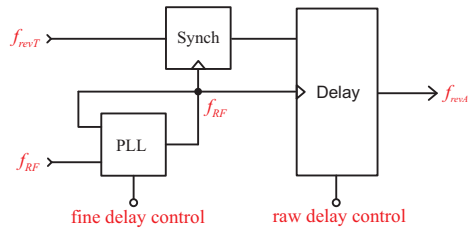

Figure 4: Programmable Delay Line (PDL). Abbreviations: Sync – synchronisation circuit.

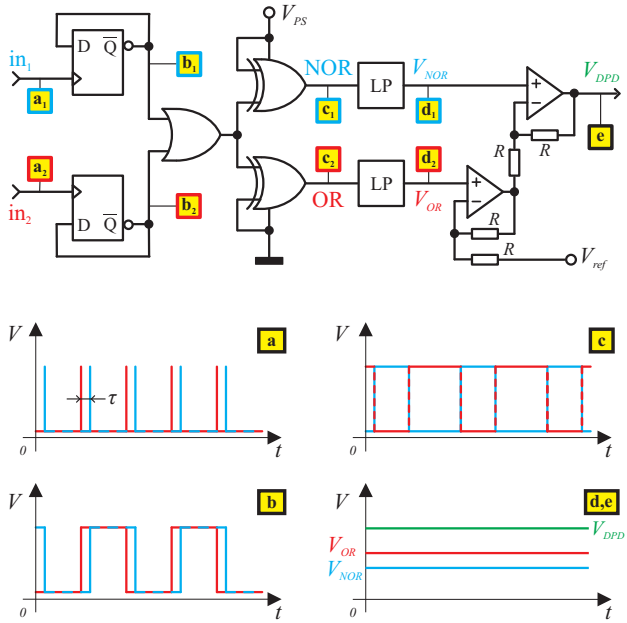

Figure 5: Block diagram of the Differential Phase Detector (DPD) and simplified waveforms in its key nodes. LP – low pass filter.

when the rising edges of the pulses at both DPD inputs coincide and the voltage is digitized by one channel of the DOROS ADC.

The pulses of both DPD inputs clock two flip-flops producing two signals with 50 % duty cycle, which conserve the delay τ between the two input signals. The flip-flops drive the inputs of an OR gate, followed by two XOR gates, working in a buffer and an inverter configuration, guarantying an equal delay for both, OR and NOR outputs. If both input signals have the same phase (i.e. $\tau = 0$), then the OR and NOR signals have equal 50 % duty cycles, which are converted by identical passive low pass (LP) filters into analogue voltages of exactly equal amplitude. The LP output signals are subtracted by a differential amplifier, whose output voltage, shifted by the ADC reference voltage (V_{ref}), is digitized by one channel of the ADC. The differential amplifier with the gain of two is built as a classical instrumentation amplifier with two op-amps.

ISBN 978-3-95450-141-0

For $\tau \neq 0$ the OR duty cycle increases and NOR decreases, resulting in a decrease of the DPD output voltage. In general, the DPD output voltage V_{DPD} is

$$V_{DPD} = V_{ref} - V_{PS}\frac{|\tau|}{T_{rev}} \quad (2)$$

where $V_{PS} \cong 3.3$ V is the power supply of the CMOS XOR gates, defining the output high level. V_{PS} voltage influences the DPD gain but it is not the case for $\tau = 0$, where the DPD operation is the most important. In addition, V_{PS} can be measured by one ADC channel, which is switched by an analogue multiplexer between key nodes of the DOROS circuits.

Please note that according to (2) the phase difference of 0.01° changes the DPD output voltage only by some 90 µV. The DPD configuration is the only one found by the authors which was able to resolve such small phase changes.

LABORATORY MEASUREMENTS

The DOROS synchronisation was tested in a laboratory with locally generated signals and this paper presents some measurements of the most important blocks.

The functionality of the local timing generator was tested with beam pulses simulated with an arbitrary waveform generator in conditions representative of LHC beams. One such measurement is shown in Fig. 6, presenting the LTG holdoff output pulses (top trace in blue) triggered upon the first pulse after a larger gap in the pulse train (bottom trace in magenta). The LTG capability of locking to any asymmetry in the bunch train allows permanent monitoring of the synchronisation between the timing f_{revT} reference and the beam.

The performance of the differential phase detector is summarised on the plots in Fig. 7. In the first measurement the phase of the DPD input signals was changed in 200 ps steps. The steps, with the size selected for good plot readability, were produced using the programmable delay line, proving its good operation. The samples of the DPD output were averaged over 40 ms and 1 s intervals, corresponding to the standard processing applied to DOROS orbit samples. This way the DPD signal is processed and transmitted along with other DOROS samples.

In the second measurement the phase of the DPD input signals was kept constant for some 7 minutes. It can be seen that increasing the sample averaging by a factor of 25, from 40 ms to 1 s, only reduces the peak-peak noise by roughly a factor of 2. This indicates that the DPD output noise is dominated by low frequency content, which did not average out well over 1 s periods.

The peak-peak noise seen on the traces in Fig. 7 is of the order of the 200 ps steps, which corresponds to 0.0008° at f_{rev}. This resolution is by far sufficient for synchronising the DOROS units, with the goal of 0.01°. Please note that the phase noise of 200 ps_{pp} corresponds to some 7 μV_{pp} read by the ADC at the output of the DPD.

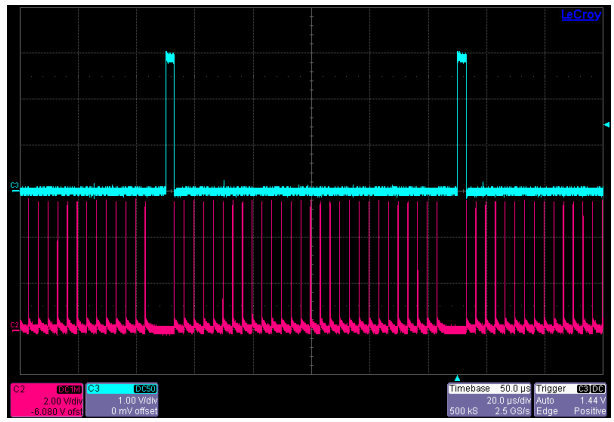

Figure 6: Laboratory testing of the local timing generator (LTG). Shown are the input and holdoff output waveforms in magenta and blue, respectively.

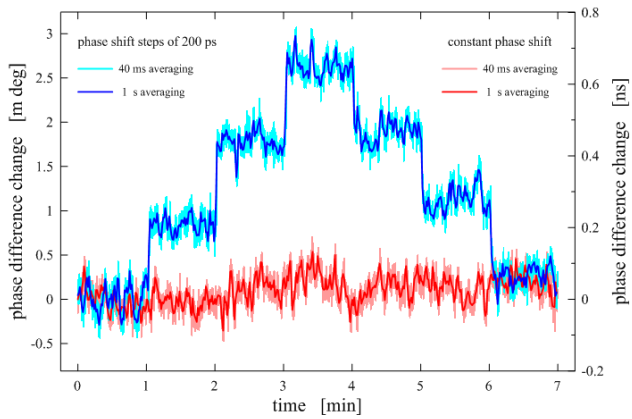

Figure 7: Response of the differential phase detector upon 200 ps delay steps (in cyan and blue) and the detector 7 minute stability (in red).

The jitter of the ADC master clock was measured to be about 5 ps_{RMS}. Its good quality resulted in the sampling jitter of about 30 ps_{RMS}, as measured on the data ready pulses.

CONCLUSIONS AND OUTLOOK

The timing and synchronization circuits are an important part of the DOROS system, particularly so for the phase advance measurement sub-system. For such measurements all DOROS front-ends need a common f_{revA} reference with the phase adjusted to the same bunch of the circulating beam. However, for the betatron coupling measurements the phase of the f_{revA} reference in each the system front-ends is not important and for the orbit measurements even its frequency does not matter.

For the phase advance measurements the revolution frequency reference f_{revT} derived from the LHC timing system needs to be aligned to the same beam bunch. As each LHC filling always starts from an injection of a low intensity pilot bunch, this bunch can be used for the

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timing alignment or its verification. In addition, the presented local timing generator is capable of deriving the revolution frequency reference from the LHC beam in practically all beam configurations. This reference can be used for a continuous monitoring of the phase of the adjusted timing reference f_{revA} by comparing the two signals using the differential phase detector, whose output is digitized in parallel to all other DOROS channels.

The presented differential phase detector allows measurements with a resolution in the order of 0.001º while the programmable delay line allows a fine adjustment of the timing f_{rev} reference in 100 ps steps. Both values are by far sufficient for achieving the synchronisation between the DOROS units at the 0.01º level.

After the LHC restart in 2015 the embedded BPMs of the 18 new collimators will operate with the DOROS system. In addition, DOROS front-ends will be installed on selected BPMs close to the LHC experiments, operating in parallel to the standard BPM electronics. This first DOROS operational installation, containing a few tens of front-ends, will allow its systematic testing and optimisation of its three measurement modes: orbit, local coupling and phase advance. The phase advance will be a real test bed for the performance of the presented DOROS synchronisation.

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ISBN 978-3-95450-141-0