ALS TIMING SYSTEM UPGRADE*

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Abstract

The Advanced Light Source (ALS) is in the process of upgrading its timing system as a part of the ALS Instrumentation and Controls Upgrade project. The timing system built upon construction of the machine at the beginning of the 1990s is still in operation today, and a replacement of the machine timing system is under way based on a commercially available solution, benefiting from 20 years of improvements in the fields of digital electronics and optical communications. An overview of the new timing system architecture based on a Micro-Research Finland (MRF) solution is given here.

INTRODUCTION

The primary function of the ALS timing system is to synchronize and sequence all systems required to deliver beam from the gun through the injection system to the storage ring. In addition, the timing system synchronizes diagnostics to the beam and provides controls for optimizing injection efficiency and selecting the operating mode.

The existing timing system has a centralized architecture that performs control and logic functions locally and distributes individual signals with coaxial or single-fiber optical cables. The hardware modules are primarily based on discrete ECL and TTL logic and reside in eurocard bins [1]. The remote control interface is provided by three embedded Intelligent Local Controllers (ILCs) [2] that communicate with the logic modules through the custom bin backplanes. The ILCs communicate with the rest of the control system through a multi-drop 2 Mb/s serial link connected to a Multibus I processor which now connects to the newer EPICS-based control system equipment.

The timing system upgrade is part of a larger Instrumentation and Controls Upgrade (ICU) project at the ALS to modernize controls, improve machine performance, and reduce vulnerability to single-point failures and aging equipment. Many of the ILCs have been replaced by a plug-compatible ILC Replacement Module (IRM) [3], but it was not feasible to use this solution for ILCs in systems such as the timing system where their usage is more specialized. The ICU project also includes new systems with timing requirements that could not be met by the existing system without significant changes to the infrastructure. Some of these systems, such as Beam Position Monitors (BPMs) based on the NSLS-II BPM architecture [4], rely on event-based timing, which the existing system does not support.

A survey of similar, more modern accelerator timing systems revealed that the most common commercial solution for event-based timing systems was based on Micro Research Finland (MRF) [5] hardware. In particular, NSLS-II had developed EPICS drivers for the MRF hardware in their timing system [6]. MRF hardware was chosen as the platform for the new ALS timing system to accelerate development by leveraging demonstrated commercial hardware with EPICS drivers.

Since the timing system has many existing clients that are not in the scope of the ICU project, interfaces to existing equipment had to be carefully considered to define the scope of the timing system upgrade. In general, timing logic and distribution infrastructure that could be slaved to a new trigger from the MRF system was retained. In particular, the existing sequencing and trigger generation system for the Linac, the trigger distribution infrastructure for Booster magnets, and the user timing and gating systems for beamlines will be slaved to the new MRF system.

The existing timing system relies on a measurement of the Booster dipole magnetic field to generate raw Booster injection and extraction field triggers, and then synchronizes them to the RF domain and the beam, as described here [7]. The new system uses time-based field triggers, so the field measurement was separated into a new diagnostic system. This system takes the field triggers as inputs and provides a "field" stamp of the measured field at the time of each field trigger, which is available for monitoring in the control system.

An additional challenge with this upgrade is commissioning a complex new system on a multi-user accelerator with minimal impact to experimenters. This constraint requires careful planning to minimize the risk of downtime during installation, testing, and commissioning of new system components. To accommodate this, where possible the project has been broken into several phases so new functions, features, and equipment can be tested in smaller groups. A bench test environment and a parallel machine test system have been set up so development can be demonstrated as fully as possible before migrating to production.

ARCHITECTURE

The ALS event system consists of a central Event Generator (EVG), event distribution using high speed serial transceivers, fiber optic cables, and electro-optical fanouts, and an array of Event Receivers (EVRs) placed as close to existing client signal inputs as feasible, or embedded in the system firmware of new clients. Each EVG and physical EVR resides in a VME crate with an IOC running EPICS connected to the ALS control system

*This work was supported in part by the U.S. Department of Energy under Contract Number DE-AC02-05CH11231.
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ISBN 978-3-95450-141-0

via Ethernet. The physical EVRs generate analog triggers and clock signals for the various existing client systems. A block diagram of the timing system fiber optic network is shown in Figure 1.

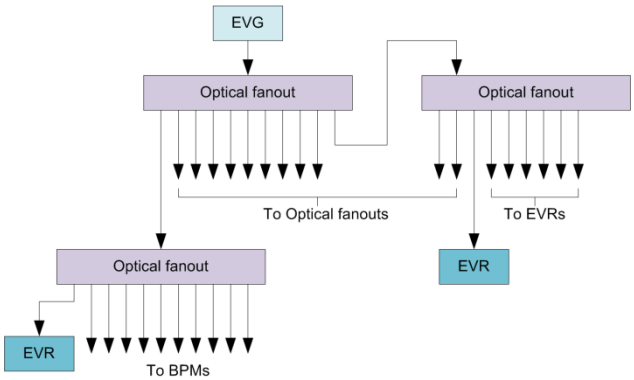


Figure 1: Timing System Event Link Block Diagram.

HARDWARE

A combination of commercial and custom hardware was used to construct this system. The commercial MRF components include the EVG (MRF VME-EVG-230), EVRs (VME-EVR-230RF), optical fanouts (VME-FOUT-12), as well as various MRF Universal I/O boards and carriers. MVME3100 CPU boards serve as IOCs. VME crates were built by Dawn (1U, 3U sizes) or Wiener (5U). All fiber optic trunk and patch cables are standard 50um OM3 multi-mode cables (typically aqua colored).

Two custom chassis were designed to provide signal and connector translations between the MRF outputs and existing client system inputs at several locations throughout the accelerator. The TTL Translation Rate Limit Chassis converts TTL signals on LEMO connectors to either differential TTL or differential NECL outputs on Twin BNC connectors. It also provides a hard-coded rate limit on all signals to protect clients against mis-setting the sequence rate in the EVG.

The CML Translation Chassis converts CML signals on a pair of LEMO connectors to TTL outputs on SMA connectors or differential NECL outputs on Twin BNC connectors. It also takes a raw 60Hz AC signal from the line cord and converts it to a TTL output on a LEMO connector, and a 500MHz sine wave on an SMA connector to a differential NECL output on a Twin BNC.

The Booster field diagnostic system consists of 2 IRMs with slightly modified firmware and some discrete TTL logic inside an ILC chassis.

Embedded Event Receiver

An MRF-compatible embedded event receiver was developed by NSLS-II and included in their accelerator instrumentation platform [8]. This platform serves as the Digital Front End (DFE) board in the NSLS-II BPM chassis, which was adopted for use in the new ALS BPMs.

The NSLS-II embedded EVR was modified so that the phase relationship between the EVG event clock and the EVR recovered clock is fixed, permitting synchronous RF-based clock recovery. In the ALS BPM, the recovered clock is used to regenerate the orbit clock that is the reference for the BPM ADC sampling clock.

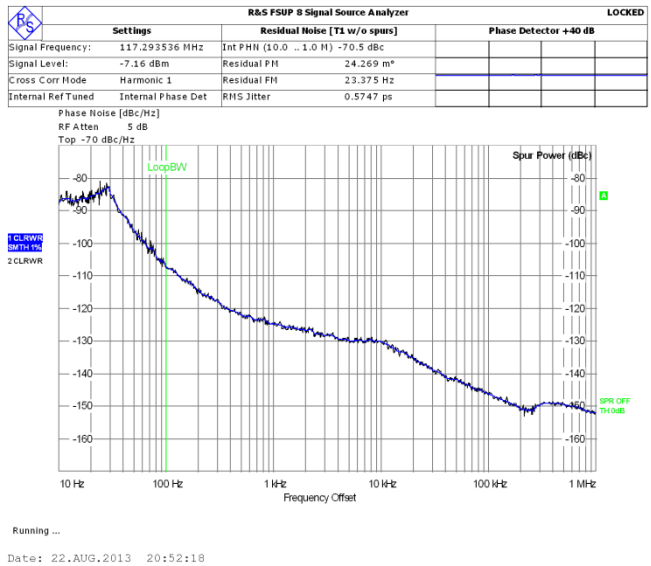


Figure 2: Embedded EVR Phase Noise.

A measurement of the ADC sampling clock phase noise using the embedded EVR as the PLL reference is shown in Figure 2, with a corresponding RMS jitter of less than 600ps. The SINAD of the BPM in this configuration was compared to the MRF EVR analog reference configuration. No degradation in performance was noted.

This modified embedded EVR has since been ported to the new ALS Bunch Current Monitor (BCM) system, where it is also used to derive an RF-synchronous reference for the sampling clock.

The embedded EVR was designed to use a Xilinx Virtex-6 series high speed transceiver [9]. However, it is possible to port the design to another Xilinx device family or different FPGA vendor by replacing only the hardware-specific portion of the EVR code. This EVR only requires an FPGA with a high speed serial transceiver supporting transfer rates of 20x the event clock rate (2.5Gb/s for ALS) connected to an SFP port and a local reference clock close enough in frequency to the event clock rate that it can be used as a reference for the transceiver clock recovery PLL.

SOFTWARE

The ALS Timing System IOCs run the MRFIOC2 EPICS device and driver support developed for the MRF hardware in the NSLS-II Timing System. NSLS-II also provided EDM engineering screens that control the MRF hardware at a low level. The IOC will provide support for the ALS event sequence control, as well as EPICS databases with ALS system-specific records. The high level interface will support EDM, Matlab, and other standalone applications to provide the array of functions and operational modes of the accelerator.

ISBN 978-3-95450-141-0

Timestamping

The event system achieves accurate and precise timestamps by combining the accuracy of a GPS NTP server with the precision of the event link, as shown in Figure 3. The timing IOCs get GPS time from the NTP server via Ethernet at boot time. The server also sends a GPS-locked Pulse Per Second (PPS) trigger to the EVG. The EVG sends this trigger out on the event link to the EVRs, which resets the event clock tick counters and generates an interrupt to increment the seconds counter in the IOC. The IOC combines the NTP time at boot, the IOC seconds counter, and the EVR event clock tick counter to form a timestamp.

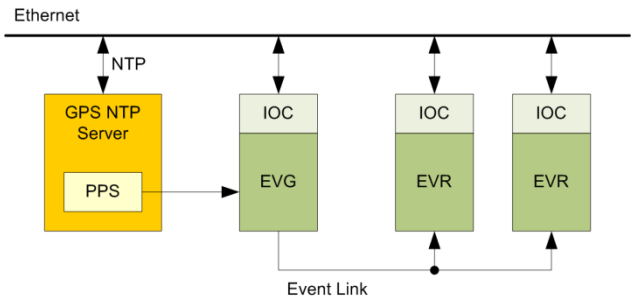


Figure 3: Event System Timestamping Block Diagram.

EVENT SEQUENCE

The Booster event sequence consists of a minimum of 7 event epochs, as shown in Figure 4. Before the Booster is ramped, some setup is required. Just over 200 ms before the start of the next sequence, the EVG sends the Setup Interrupt Event (event 62), which interrupts the master IOC (in the same crate). The interrupt triggers the IOC to read local EPICS records containing parameters defining the next sequence, reset the mode to default (no beam), and increment the sequence number.

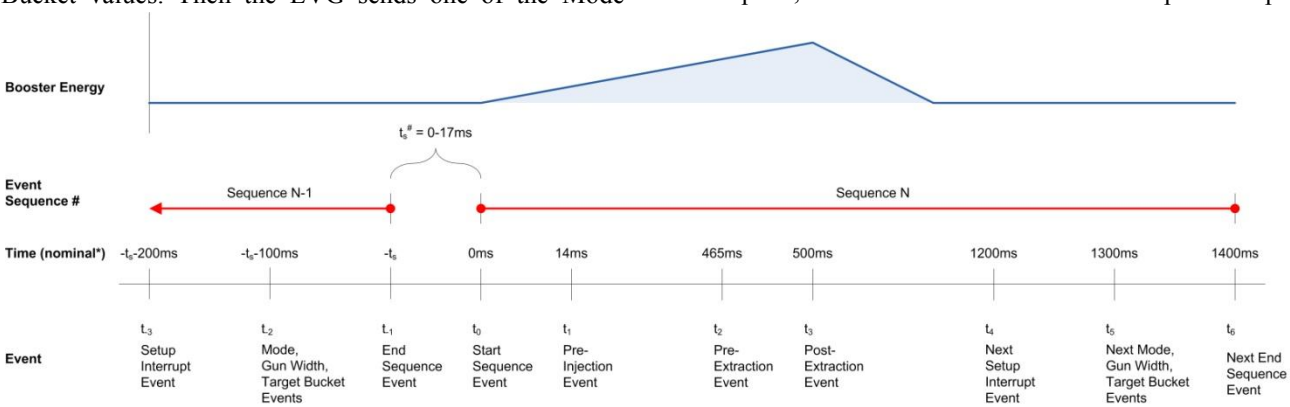
About 100 ms after the Setup Interrupt Event, the EVG sends 12 events (event 60 for binary 0, 61 for binary 1) that encode the Gun Width and Storage Ring Target Bucket values. Then the EVG sends one of the Mode Events (50-59). The modes cover the various anticipated operating modes of the accelerator, as defined in Table 1. EVRs that use these parameters load the values into their interrupt FIFOs. When the EVR IOCs receive these interrupts, they shift the values into their local parameters, and then use this information to set up trigger enables and delays for the next sequence.

Table 1: Mode Event Definitions

Event #	Definition
50	Enable Booster ramp triggers only (no beam)
51	Linac tuning
52	Booster tuning
53	BTS tuning
54	Enable all triggers
55	Custom (enable/disable triggers based on local PVs)
56-58	Reserved for future expansion
59	Disable all triggers

About 100 ms after the Mode Event is sent, the EVG sends the End Sequence Event (127). The EVG then waits for the next rising edge of the 60Hz line, followed by the rising edge of Coincidence Clock (COIC), which is generated by a free-running counter in the EVG. Once the EVG is synchronized to these signals, the next sequence can begin.

At the start of the sequence, the EVG sends out the Start Sequence Event 10 and enables the event sequence counter. Pre-Injection, Pre-Extraction, and Post-Extraction events are then sent according to the timestamps in the sequence table. After the Booster ramp is complete, the EVG sends the next Setup Interrupt



*Time values are approximate since events occur in multiples of 4/f_{RF} (~8ns).
#t_s= the variable time to synchronize to the AC Line (16.666ms) and then Coincidence Clock (~82us).

Figure 4: ALS Event Sequence Diagram. The event sequence number and event epochs are shown with respect to relative time and the Booster energy ramp.

ISBN 978-3-95450-141-0

Event, and the cycle repeats. ALS Booster operation and timing constraints are described in more detail here [7].

CONCLUSION

The ALS timing system upgrade combines mature and widely used commercial hardware with custom hardware for ALS-specific functions and interfaces. This allowed a reduction in the scope of the project while providing a flexible, expandable and event-based timing master. Leveraging the NSLS-II embedded EVR firmware and MRFIOC2 EPICS support greatly accelerated development.

Building the RF-clock recovery into the embedded EVR reduced the number of MRF EVRs and physical connections needed, significantly reducing equipment installation, cost, and maintenance in the long-term. The embedded EVR can be included in any new instrumentation firmware requiring machine timing.

A flexible and configurable event sequence scheme provides support for existing and future modes of ALS operation. Timestamps are accurate and precisely synchronized across all timing system clients, providing a level of multi-system diagnostic data correlation previously unachievable at ALS.

Project Status

ALS timing system development is well underway. The majority of production hardware has been installed, but not yet commissioned. Currently, the MRF EVG feeds field triggers to the existing timing system and the field diagnostic system, and has been providing time-based field triggers during accelerator operations for nearly a year. The first production client to make use of the embedded receiver was the BCM system, commissioned earlier this year. The first set of new production BPMs were commissioned in the Storage Ring this summer, and the new timing system provides all BPM timing via embedded receivers. The majority of the remaining work involves implementing the event sequence scheme in the IOCs, developing ALS-specific databases, and implementing the high level control interface.

ACKNOWLEDGMENTS

The authors would like to thank Michael Davidsaver, Joe DeLong, and Joe Mead of Brookhaven National Lab for support of NSLS-II components, including the MRFIOC2 support package, the embedded timing receiver, and its usage in the NSLS-II BPM DFE firmware. The authors are also grateful to John Dusatko and Patrick Krejcik at SLAC for sharing advice and experience regarding the LCLS timing system. Finally, the authors acknowledge Mike Chin at LBL for providing guidance and measurement support during development of the embedded receiver and the timing interface to the ALS BPM, and Helen Chen, Rick Lellinger, and the rest of the technical support staff at ALS for their care and attention to detail in coordinating and installing all the new equipment and infrastructure required for this project.

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ISBN 978-3-95450-141-0