FIRST TESTS OF A MICRO-TCA-BASED DOWNCONVERTER ELECTRONIC FOR 5GHz HIGHER ORDER MODES IN THIRD HARMONIC ACCELERATING CAVITIES AT THE XFEL†

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Abstract

Beam excited higher order modes (HOM) in 3.9GHz accelerating cavities at the European XFEL are planned to be used for beam position monitoring. The specifications of the monitors have been defined during an extensive study on the 3.9GHz module at FLASH. Selected HOMs for precision measurement are located around 5440MHz and 9040MHz. An electronics developed by FNAL has been recently installed at FLASH and provides a basis for the XFEL electronics.

The paper will present the design and first test of the hardware for the MicroTCA standard used for the XFEL. The hardware consists of three different Rear Transition Modules (RTM), two four channel downconverter RTMs (5GHz and 9GHz) and a third RTM with two phase locked loop synthesizers on board for LO generation. Presently the 5GHz and the PLL RTMs are under construction. The first measurements with these cards will be presented.

INTRODUCTION

The European X-ray Free Electron Laser 3.9GHz accelerating cavities are located right after the 1.3GHz injector module before the first bunch compressor, as shown in Fig. 2 [1]. The module is similar to the ACC39 module built by FNAL for the Free Electron Laser Hamburg (FLASH) [2], containing four third harmonic cavities.

The XFEL 3.9GHz module consists of eight cavities each with two HOM couplers respectively as shown in Fig. 3. We want to equip four couplers, the respective outer two, with electronics for modes around 5440MHz and fourteen for modes at 9060MHz suitable for beam monitoring as obtained in tests at FLASH ACC39 [3].

System Overview

At the XFEL the MicroTCA.4 [4] standard will be used. Figure 1 shows the planned fully equipped MicroTCA crate, consisting of five four channel downconverter RTMs with its particular SIS8300 AMC card [5]at the other side (not visible), one for the 5.44GHz modes and four 9.06GHz boards. We also see the HOM-PLL (Higher Order Mode Phase Locked Loop) RTM with a DAMC2 [6] card on the other side (not visible) to generate the LO-frequency and the uLOG for LO amplification and distribution over the MicroTCA backplane. [7]

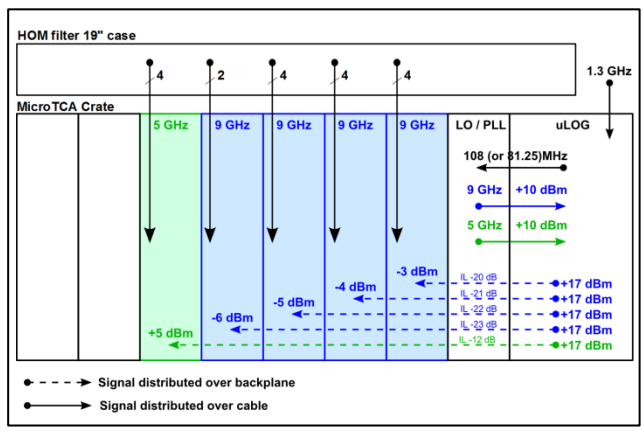

Figure 1: Overview over the complete system installation.

Above the crate there is a case which contains the HOM selecting bandpass filters for each channel. The outputs of the HOM coupler will be connected to the HOM filters.

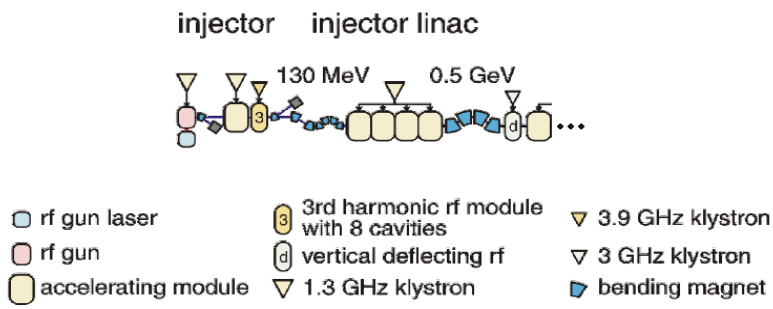

Figure 2: Schematic layout of the European XFEL injector [1].

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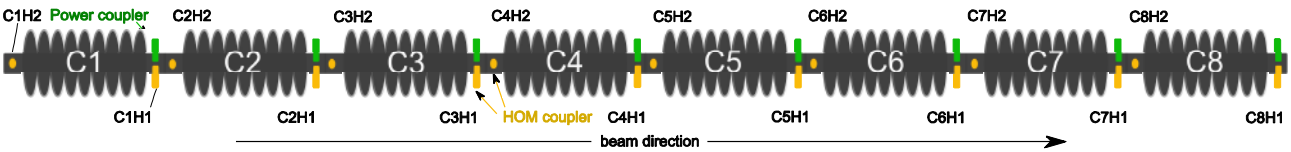

Figure 3: Cavity arrangement inside the module.

HOM FILTER CASE

The HOM bandpass filters are too big (compare Fig. 5) to include them on the RTM board, so we had to put them in an extra case. The benefit is that we could use the downconverter cards for other frequencies, if there is any application for it in the future.

A sketch of the HOM filter box is shown in Fig. 4. Since the modes around 5.44GHz propagate in whole of the module, only two cavities, the outmost ones, are planned to be connected to the 5GHz RTM. For monitoring the beam position in each single cavity we use the 9.06GHz modes, since these are trapped in each cavity. According to former studies, the respective outer couplers are not suitable, so that we need only 14 channels instead of all 16. Two signals from the outmost cavities (C1H1 and C8H2) will be split for monitoring both 5 and 9GHz modes, so that we have 18 output signals in total.

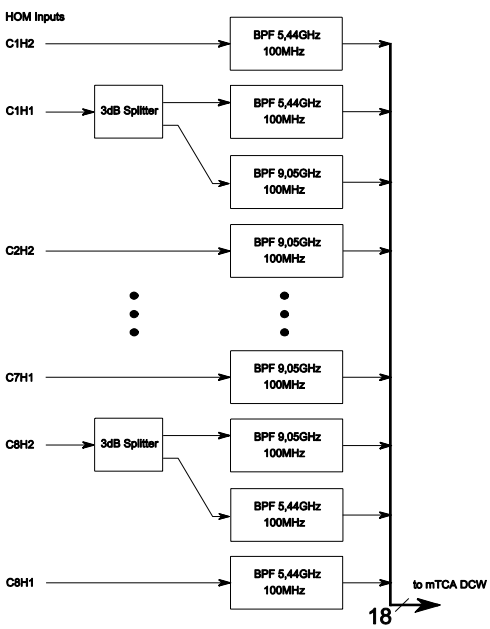

Figure 4: HOM filter case overview.

The already completed HOM filter case is shown in Fig. 5.

Figure 5: HOM filter case.

PLL SYNTHESIZER

The designed HOM-PLL (Higher Order Mode Phase Locked Loop) RTM includes two PLL synthesizers generating 5GHz and 9GHz accordingly. Figure 6 shows its block diagram.

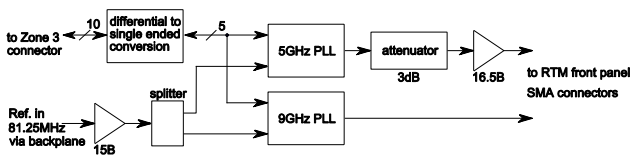

Figure 6: HOM PLL block diagram.

The Zone3 connector on the MicroTCA middle plane passes the signals from the DAMC2 AMC to the HOM-PLL RTM. The DAMC2 card includes a FPGA which manages the PLLs and provides the link to our control system.

The chosen VCO (Voltage Controlled Oscillator) for the 5GHz PLL has an operating range from 5 to 5.5GHz and the 9GHz VCO from 8.6 to 10.2GHz. In operation we set the PLLs to fixed frequencies needed to downconvert the particular HOMs but we are able to change them easily. To reach the needed input power for the uLOG (compare Fig. 1) power, we have to amplify the 5GHz LO signal. The output power of the 9GHz part is high enough and does not need additional amplification.

As reference frequency we use 81.25MHz. The PLL needs at least -6dBm at its input, so we put an amplifier and attenuator in front of the PLL input to adjust the power (the attenuators in front of the reference input are not shown in Fig. 6)

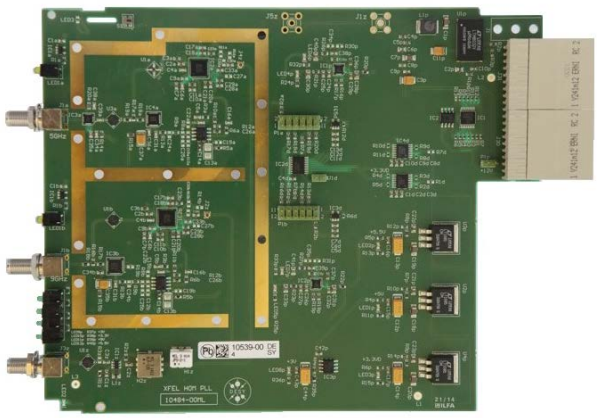

Figure 7: HOM-PLL RTM.

In Fig. 7 we see the finished HOM-PLL RTM. The uncoated lines delimit the PLL and VCO (Voltage Controlled Oscillator), on top of these lines a metallic case will be placed to protect the electronic from external effects. Only the top side of the RTM is assembled with components.

HOM PLL Test

The setup for the HOM-PLL test is shown in Fig. 8. A signal generator provides the reference frequency of 81.25MHz for the PLL. A PC is used to tune the settings of the PLL, a spectrum analyser shows the output signal.

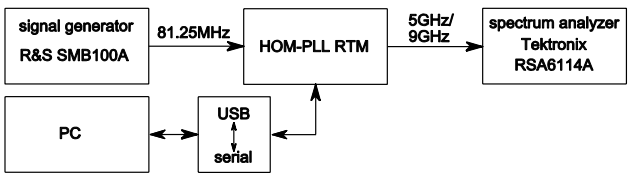

Figure 8: HOM-PLL RTM test setting.

Figure 9 shows the 5GHz output. The output power is less than expected at ca. 5dBm. We also see sidebands but they are almost 60dB below the carrier signal and should have no negative effects.

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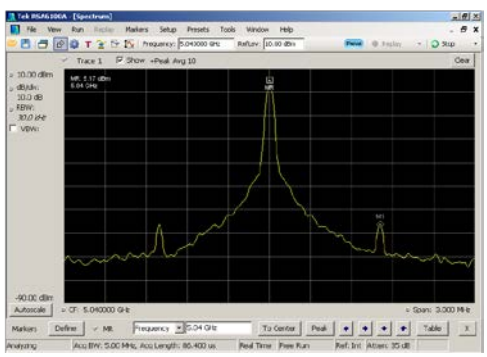

Figure 9: HOM-PLL 5GHz output.

Figure 10 shows the 9GHz output. The output power is very small at -3.7dBm. We have to find out if the signal is possibly too noisy but it is 30 dB below the carrier.

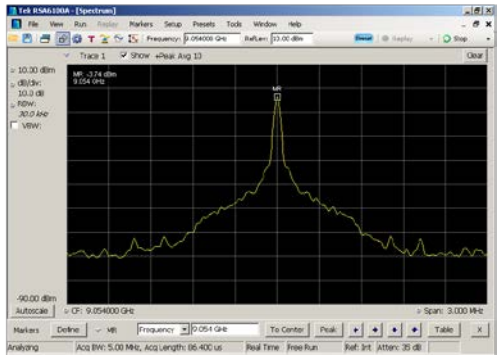

Figure 10: HOM-PLL 9GHz output.

To reach the needed output power of +10dBm we will place external amplifiers at the output and if needed attenuators for adjustment. A power connection for them is already provided on the synthesizer card.

DOWNCONVERTER CARD

Altogether we have 18 channels we want to use: four channels at 5.44GHz and 14 channels at 9.06GHz. We put four channels onto one RTM so we need only one card for the 5GHz and four cards for the 9GHz signals (compare to Fig. 1).

Figure 11 shows the general arrangement of a downconverter card. The LO frequency from the PLL-RTM will be applied over the RF backplane connector. For tests in the laboratory it is possible to connect the LO also via an SMA connector at the front panel. The signal from the HOM filters will be connected via SMA cables (circled with dotted line).

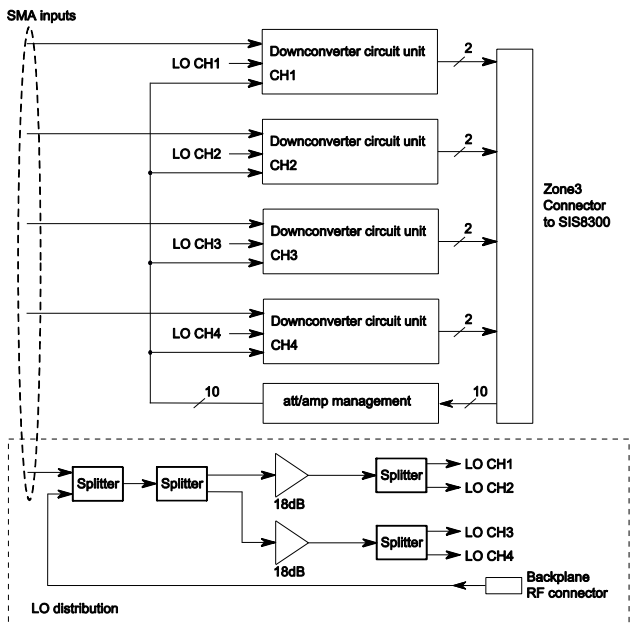

Figure 11: Block diagram of a downconverter card.

The 5GHz Downconverter Circuit

The 5GHz downconverter is arranged as shown schematically in Fig. 12. There is a step attenuator

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settable from 0.5-31.5dB in 0.5db steps at the beginning of the chain. The following 15dB amplifier can be switched off in case of high input amplitude. This chain has a tuneable input range of 46dB to ensure the required input level for the mixer to reach the optimum power level for the ADC at the end.

The bandpass filter (BPF) behind the mixer determines the intermediate frequency (IF) of 30MHz with a bandwith of 20MHz. According to the LO frequency, different areas of the spectrum within the 100MHz bandwith of the input filter can be downconverted.

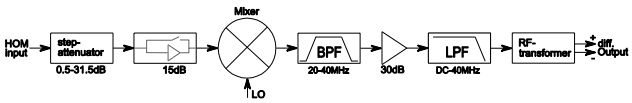
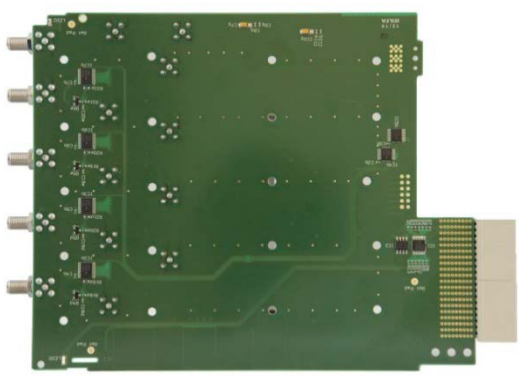


Figure 12: Block diagram of 5GHz downconverter channel.

The IF amplifier increases the IF power to reach the required input level for the ADC. The low pass filter (LPF) decreases the noise at the end. The RF-transformer changes the single ended signal to a differential signal needed by the ADC.

The design of the 5GHz RTM has been finished and a manufactured card can be seen in Fig. 13. One can easily notice the 4 channels. The uncoated lines on the top create space to place a metallic case on top of the RF electronic.

(a)



(b)

Figure 13: HOM downconverter: bottom side (a) and top side (b).

The 9GHz Downconverter Circuit

The 9GHz downconverter has almost the same arrangement as the 5GHz one. They only differ at the beginning of the chain as it can be seen in Fig. 14.

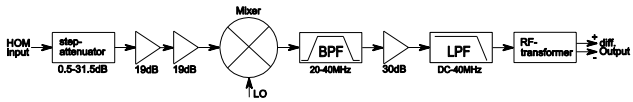


Figure 14: Block diagram of 9GHz downconverter channel.

Due to the higher amplification needed for the lower power signals of the 9GHz modes as against to the 5GHz modes, the 9GHz circuit will have an input range of 70.5dB.

The electronic of the 9GHz card is very similar to the 5GHz RTM. It will be manufactured after finishing tests with the 5GHz card.

Downconverter Tests

The 5GHz downconverter card was recently manufactured. A soldering issue with the footprint of the mixer component was found and it seems that it will have to be remade.

The test setting looks like mapped in Fig. 15.

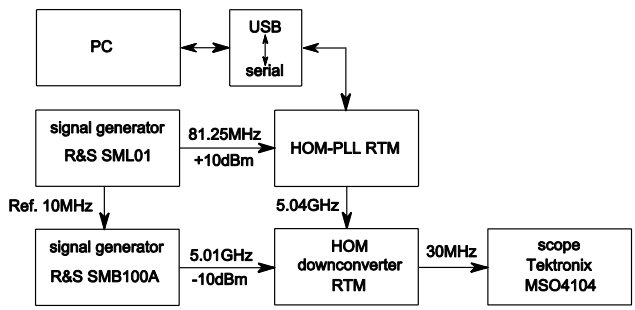


Figure 15: HOM downconverter test setup.

Even if we cannot measure anything at the scope, because the mixer does not work, we checked the input signals of the mixer. The LO frequency at the mixer input (compare Figs. 12 and 14) with +10dBm input power to the card is -6dBm (see Fig. 16). The mixer should work with this amount of power.

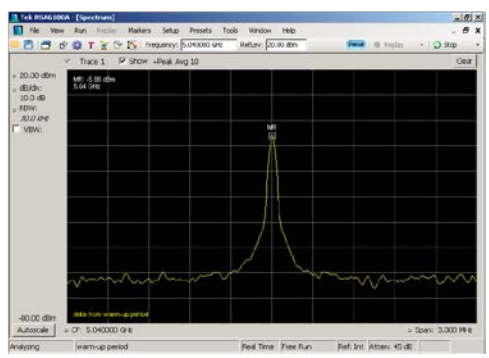


Figure 16: Measured power at mixer input.

We also checked the efficiency of the step attenuator and amplifier. With maximum amplification (without attenuation) with an input power of -10dBm we reach -15dBm at the mixer input (see Fig. 17).

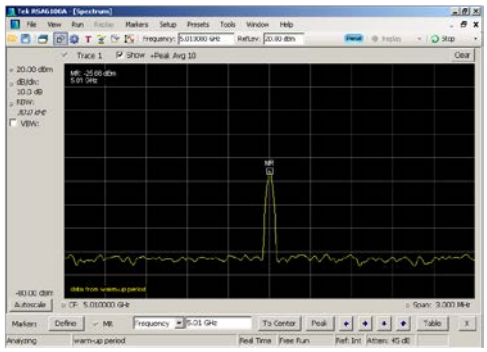


Figure 17: Signal input power at mixer (proportion 1/10).

We must add 10dBm to the measured signal as the point of measurement is connected via an 1 to 10 divider, whereas Fig. 16 shows the correct power because of using a connector cutting the following structure and connecting it directly to the spectrum analyser.

CONCLUSION

The PLL card is working well and is ready to use. Unfortunately the 5GHz downconverter card does not work yet and needs to be remade. After the successful testing of the new 5GHz card, the 9GHz card will be designed. The difference between both cards is very small so the design of the 9GHz one will be very fast.

OUTLOOK

The following step will be to test the whole system under real conditions with beam at FLASH and compare to the electronic from Fermilab.

It is planned to eventually implement the beam position calculation, now being made with a MATLAB code, in the FPGA on the Struck SIS8300 digitizer card, and thus speed up to information transferred to the control system.

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