STATUS OF THE SIRIUS RF BPM ELECTRONICS

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Abstract

A modular and open-source RF BPM electronics based on the PICMG® MicroTCA.4 and ANSI/VITA 57.1 FMC standards is being developed to be used at Sirius, a 3 GeV low emittance synchrotron light source under construction in Brazil. This paper reports on the latest development advances focusing on bench tests of the second version of the RF front-end and evaluation of the electronics with beam at SPEAR3 (SSRL/SLAC). The interface of the BPM electronics with the orbit feedback system is also discussed.

INTRODUCTION

Sirius is a new 3 GeV synchrotron light source under construction in Brazil [1], targeting a 0.28 nm.rad natural emittance. Storage ring commissioning has been rescheduled and should occur in the 1st semester of 2018.

The Sirius RF BPM electronics is composed of a low noise RF front-end (RFFE) which process the signals coming from RF BPM pick-ups and a typical FPGA-based digital receiver employing direct RF sampling technique and further difference-over-sum algorithm to extract beam position information. The RFFE uses the "switching electrode" principle [2] to compensate for low frequency drifts originated in the RF chains. Instead of multiplexing the four BPM signals into one single RF chain or using a full four-by-four crossbar switching scheme [3], only diagonal BPM antenna signals are switched, as seen in [4].

The system is modular, based on proven industrial standards and is being developed as an open source project. Information on technical choices and hardware and software structures were detailed in the past [5, 6, 7].

During the last year, effort to consolidate the hardware has been done by the development team. Open questions about performance limitations were solved and a new spin of the RFFE and ADC boards was concluded.

Bench tests revealed the current BPM electronics performance status. In addition, beam tests performed at SPEAR3 (SSRL/SLAC) showed the operation of the electronics with realistic broadband BPM signals.

The MicroTCA.4-based digital platform, composed of CPU and FPGA boards for readouts and fast orbit feedback (FOFB) implementation, is currently being integrated and will be detailed in future work.

SYSTEM REQUIREMENTS

BPM electronics specification is mainly driven by beam orbit stability requirements. At Sirius, the most stringent electron beam stability requirement is given by the vertical beam size at the center of the longer straight sections, namely 1.94 µm. In order to achieve position stability better than 5% of this beam size within a 0.1 Hz to 1 kHz bandwidth, the corresponding vertical plane RMS orbit disturbance shall be lesser than 97 nm. By allocating half of this budget to orbit distortions exclusively caused by electronic and mechanical BPM noise, which is transferred to the beam through the fast orbit feedback loop, a 69 nm RMS orbit disturbance specification was derived for BPMs.

Simulations with the Sirius storage ring show that a factor of 0.72 translates uncorrelated RMS noise in all storage ring BPMs to an RMS orbit disturbance at each of the long straight sections. Hence the 69 nm orbit distortion specification derived above can be relaxed to 95 nm when translated to noise on the BPMs. From this resulting number, a 50 nm upper bound RMS BPM noise is reserved for mechanical vibration on the BPM stands, thus leaving 80 nm RMS noise (or resolution) budget for the BPM electronics itself.

Table 1 summarizes BPM electronics resolution specification alongside more general requirements for the Sirius's BPM system. The numbers have been reviewed since last publications [6].

Table 1: Requirements of Sirius RF BPM Electronics

Parameter	Value
Resolution (RMS) @ 0.1 Hz to 1 kHz	< 80 nm
Resolution (RMS) @ turn-by-turn full bandwidth	< 3 µm
1 hour position stability (RMS)	< 0.14 µm
1 week stability (RMS)	< 5 µm
Beam current dependence (decay mode)	< 1 µm
Beam current dependence (top-up mode)	< 0.14 µm
Filling pattern dependence	< 5 µm
First-turn resolution (RMS)	< 0.5 mm
Horizontal/Vertical plane coupling	< 1%

HARDWARE IMPROVEMENTS

The tests carried out in 2013 [6] were performed with the first versions of the RFFE and ADC boards, which has partially fulfilled specifications. The following sections describe the modifications made since then.

RF Front-End Board

The RFFE v1 board concept consisted of an analog front-end in which several calibration and compensation schemes (channels switching, pilot tone and temperature control) were available for comparative tests [8]. The RFFE v2 was designed as a cost-optimized board in

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which only the most effective calibration schemes were present. The major changes on RFFE v2 are listed below:

- Improvement of noise figure by reducing 6 dB on insertion loss before the first amplifying stage.
- A low pass filter has been added before the diagonal switching circuit in order to avoid high peak voltages on the RF switches.
- Reduction in the number of RF amplifiers per channel, from 3 to 2, and in the number of RF programmable attenuators per channel, from 2 to 1.
- Reduction in the number of temperature control elements in each RF diagonal channel. Only one temperature controller per diagonal pair of channels has been placed close to the devices upstream of the RF diagonal switching scheme. Temperature control has proved necessary only for those elements upstream of the RF switches, such as low pass filters and matching network.
- Redesign of the diagonal switching scheme using DPDT RF switches. The switching response time was decreased by a factor of 100, from 2 µs to 20 ns (90% stabilization time).

Figure 1 shows the RFFE v2 prototype emphasizing one of the RF channel pairs.

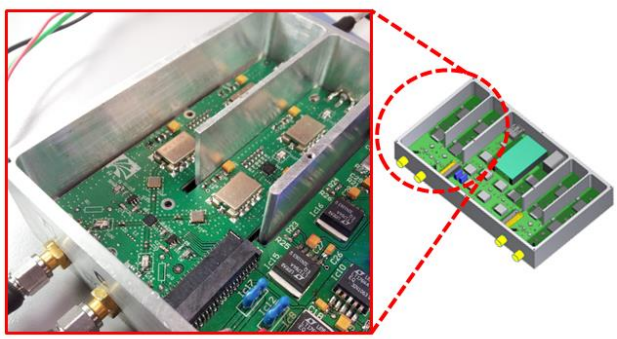

Figure 1: RFFE v2 prototype board. The dimensions of the prototype aluminum box are 20 cm x 11.5 cm.

An important shortcoming of the RFFE v2 was the reduction in dynamic range due to the removal of an amplification stage of the RF chain. An additional amplification stage will integrate the final version of the RFFE, currently under development.

FMC ADC Board

Two variants of FMC (FPGA Mezzanine Card) four-channel fast ADC boards were designed and produced since the very early stages of the project, differing by the data converters in use: LTC2208 (130 MS/s ADC) or ISLA216P25 (250 MS/s). Efforts have been concentrated on the former board, on which a few hardware modifications have been implemented:

- RF traces at signal inputs were carefully symmetrized.
- The ADC LTC2208 matching network was improved resulting in 2.5 dB reduction in insertion loss at 500 MHz, keeping the S_{11} parameter lower than -20 dB.
- Lower additive phase noise RF switch has been used as reference clock selector.
- Standard ADC digital LVPECL clock terminations were adopted, slightly improving SFDR performance by ~2 dB.

EXPERIMENTAL SETUP

Figure 2 shows the setup used in all tests herein described. This test platform does not rely on the MicroTCA digital hardware platform which has been developed for the final BPM system [7], although FPGA digital signal processing firmware and control software are kept essentially the same. The described setup is based on a FPGA development kit and a small form factor mini-ITX PC board with PCI Express connectivity, to allow easy transportation of the system for different environments. Several RF signal and external clock sources were used across the tests.

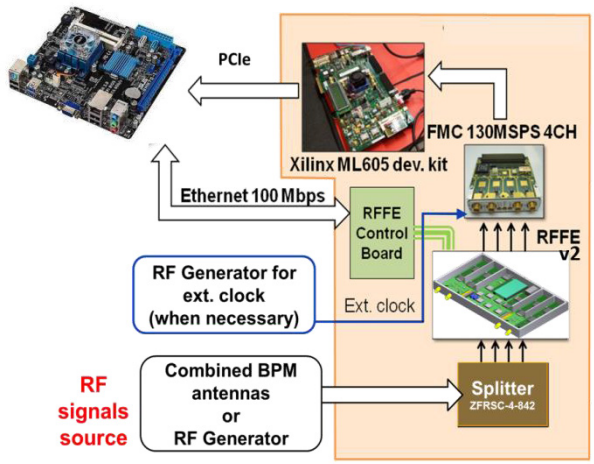

Figure 2: Block diagram of the setup used for the BPM electronics test.

PERFORMANCE IMPROVEMENTS

Previous tests with the Sirius BPM electronics have already met filling pattern dependence and temperature dependence specifications. On the other hand, resolution and beam current dependence (BCD) performance figures were only partially within specifications [6]. In 2014 several laboratory tests were carried out in order to understand the referred limitations and find solutions for improvements. The following sections show the results of such effort.

Unless otherwise noted, all bench tests herein presented have been performed using two locked R&S SMA100A RF signal generators for both clock and signal inputs. Centered beam was simulated by splitting by four the generated signal. The switching frequency was made identical to the FOFB data rate frequency (~110 kHz).

Resolution

From RFFE v1 to v2, the following facts have led to improvements on resolution performance:

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- Due to wrong FPGA calibration of delays between ADC clock and data paths, one of the four channels had one clock cycle delay relative to the others, resulting in a loss of correlation between diagonal channels and hence reducing the diagonal switching effectiveness. The correction of this issue has improved resolution performance.
- Faster RF switches allowed swapping the RFFE channels at higher rates thus reducing the loss of signal power and guaranteeing smooth transition of signal phase when transitioning switches' states.
- Noise figure has improved due to RFFE circuit redesign.

Figure 3 shows the resolution in function of input power obtained after the improvements. An integration bandwidth of 2 kHz and a BPM geometric factor of $k = 10$ mm have been used to allow comparison with previous results. It has been measured for centered beam with optimized RFFE attenuator values. The 80 nm resolution specification could be reached for input power levels higher than -25 dBm, corresponding to a beam current above 200 mA at Sirius.

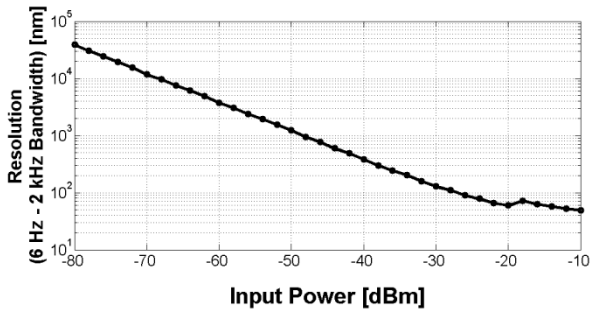

Figure 3: Resolution in function of input power.

The integrated RMS noise for two input power levels, -10 dBm and -20 dBm, with diagonal switching on and off, is showed in Fig. 4. The noise suppression effect of the switching is more evident at lower frequencies.

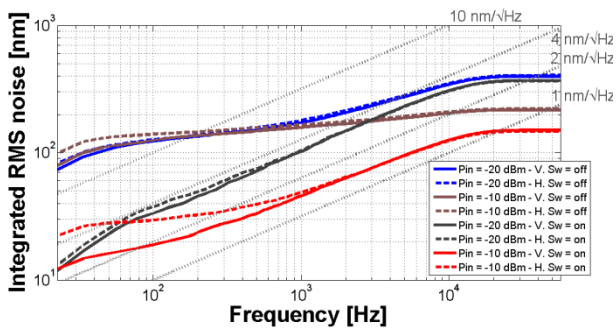

Figure 4: Integrated RMS noise for different input power and diagonal switching scenarios.

Beam Current Dependence

BCD tests were recently performed using new data acquisition software, with longer buffers and automated acquisition, which has made it possible to evaluate beam position average value with less uncertainty at lower input power conditions.

The long range BCD simulating a beam decay mode operation is depicted in Fig. 5. It shows that the ±1 µm requirement is satisfied for input power levels above -45 dBm, corresponding to a beam current of approximately 20 mA at Sirius. Nonlinear behavior of the RF chains, in the order of ~0.001 dB, is responsible for these observed BCD characteristics.

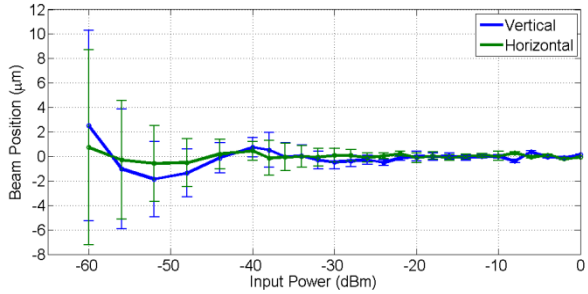

Figure 5: Long range BCD for centered beam.

The short range BCD for five different input power levels, from -40 dBm to -10 dBm, was also verified and met the ±0.14 µm top-up operation requirement with considerable margin, as can be seen in Fig. 6.

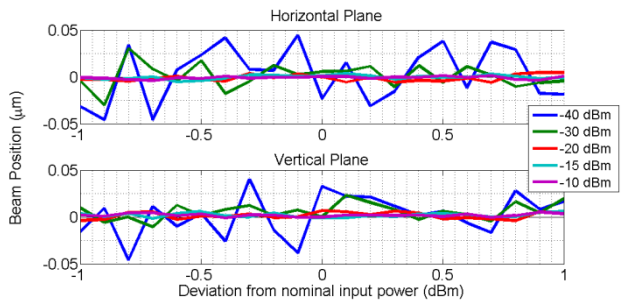

Figure 6: Short range BCD for centered beam.

TESTS WITH BEAM

In March 2014, tests with beam were performed at SPEAR3 storage ring in order to verify system performance under realistic conditions. Figure 7 shows the test setup used for the tests, essentially the same as depicted in Fig. 2.

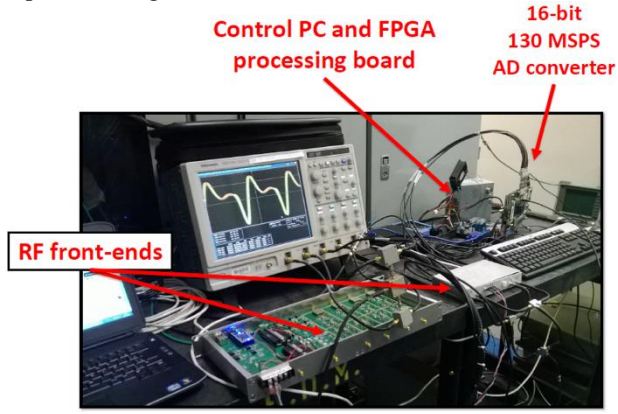

Figure 7: Setup used for the tests with beam at SPEAR3.

Four beam signals coming from a spare button BPM were combined and then split by four with a broadband

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splitter in order to emulate a perfectly stable beam. The ADCs external clock input was sourced by a 64.02 MHz sine wave clock locked to the beam frequency coming from SPEAR3's timing system. This clock frequency was chosen by convenience since it was readily available. The tests were performed under the following beam conditions:

- Parasitically to user beam: a 500 mA stored beam current relying on top-up refills every 5 minutes with standard filling pattern. The beam's first RF harmonic at 476 MHz provided -13 dBm power at the BPM electronics inputs. Different sets of external attenuators were used to emulate different beam currents.
- Accelerator physics shift: a 200 mA stored beam, low alpha mode with 4.5 ps RMS bunch lengths with a variety of filling patterns. No external attenuator was used.

Figure 8 shows the integrated RMS noise values for four situations where the input power was kept nearly the same in order to keep the same RFFE attenuators configuration (except for a 0 dBm generator experiment also showed for reference).

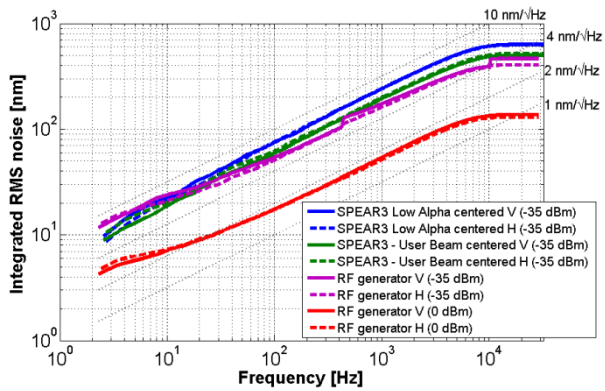

Figure 8: Integrated RMS position noise for four different conditions: (i) SPEAR3 beam in low alpha mode (200 mA), (ii) SPEAR3 beam during user shift (500 mA), (iii) RF generator R&S SMB100A at -35 dBm, and (iv) RF generator R&S SMB100A at 0 dBm.

Integrated RMS beam position noise for SPEAR3 low alpha beam shows that even for bunch lengths as short as 4.5 ps there is no relevant intermodulation products in the spectrum which could affect the beam position measurement at the FOFB data rate. Since the natural bunch length of Sirius is expected to be roughly 9 ps, this can be considered as a worst case scenario with considerable margin. Moreover, coaxial BPM signal cables at Sirius (LMR195) are expected to have higher dispersion than those used at SPEAR3 (LMR240), thus providing additional filtering of beam's RF harmonics.

EXTENDED DISCUSSION

RF Channels Switching Mechanism

As it will be shown in this section, the usage of the diagonal switching scheme virtually eliminates electronic noise originated from the RF chain downstream of the switches. Long term and flicker noise drifts on RF channels' gain are almost completely compensated and hence puts the ultimate beam position resolution limitation on the ADC clock source's phase noise and on long term drifts of all elements upstream of the RFFE diagonal switching.

A practical criterion to distinguish the high, medium and low frequency ranges is described below and is based on the coherence function of channels' noise when the diagonal switching mechanism is active.

The coherence function of two signals, x and y, is defined as $C_{xy}(f) = \frac{|P_{xy}(f)|^2}{P_{xx}(f)P_{yy}(f)}$, where $P_{xx}(f)$ and $P_{yy}(f)$ are the Power Spectral Density (PSD) of signals x and y, respectively, and $P_{xy}(f)$ is the Cross Power Spectral Density (CPSD) of both signals. The coherence function measures how well frequency components of the two signals are correlated with each other.

Figure 9 shows the coherence for all combinations of channels when the diagonal switching scheme is turned on or off. The test has been performed with 0 dBm input power and considered a typical configuration of RFFE attenuators, satisfying both resolution and BCD requirements.

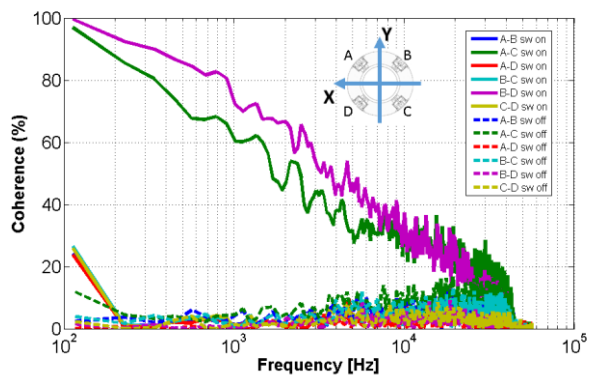

Figure 9: Coherence function between pairs of antenna baseband signal additive noise at FOFB data rate (~110 kHz). BPM signals naming convention is indicated.

It can be noted that the switching scheme is responsible for introducing coherence between the diagonal channel pairs (A-C and B-D) from DC to approximately 40 kHz. For frequencies below 100 Hz, coherence is better than 95%. A rough classification can be thus proposed:

- Low frequency range (from DC to ~100 Hz): noise is dominated by long term drifts and flicker noise of elements downstream of the switches; all drifts on RF channels are considered to be vanished due to common mode noise rejection in difference-over-sum position calculation algorithm.
- Medium frequency range (from ~100 Hz to 40 kHz): the higher the frequency the higher is the noise contribution of uncorrelated RF channel gain and ADC clock phase noise.
- High frequency range (from ~40 kHz to a few GHz): noise is dominated by clock jitter integrated over the

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~40 kHz to the ADC clock input bandwidth (typically a few GHz).

This result shows that the switching scheme could be used to compensate for noise from very low frequency up to roughly half of the switching frequency, including clock phase noise and long term gain drifts originated in the RFFE chains, such as RF amplifiers' flicker noise.

Reference Clock

Although the bench tests herein presented have been performed with ADC clocks directly sourced by RF signal generators, preliminary results showed that position measurement resolution is not significantly degraded when the PLL-based clock synthesizer available on the FMC ADC boards is used. This result was already expected, since the switching mechanism introduces high coherence below the chosen PLL bandwidth, 300 Hz. On the other hand, white noise introduced by Si571 VCXO and clock distribution broadband jitter (from 30 kHz to 3 GHz) is not significant (< 250 fs) and is responsible for a resolution performance degradation of less than 10 nm.

Orbit Feedback and BPM Delay

The BPM system was conceived with a strong focus on its integration with the FOFB system. A 1 kHz cross-over frequency performance goal for closed-loop orbit feedback was established in order to allow disturbance attenuation greater than 20 dB for frequencies below approximately 100 Hz. Combined fast steering magnets, power supplies and vacuum chamber response was optimized for a -3 dB bandwidth above 10 kHz for kick amplitudes below 25 µrad, making closed-loop latency the most critical parameter for performance optimization.

The fundamental limiting factor in terms of FOFB latency was found to be the accelerator-wide sensors and actuators data distribution. Detailed calculations showed that the usage of multigigabit digital communication through FPGAs and efficient network topology would allow a theoretical minimum latency of ~5.3 µs for Sirius, out of which ~2.5 µs would come from light propagation through several optical fibers along half storage ring circumference (250 m). The calculations considered frame headers, checksums and FPGA logic overheads, as well as a factor of 2 fiber length safety margin. Considering additional margin in the latency budget, a goal of 10 µs latency for a complete data distribution cycle was determined.

Given that scenario, BPM delay, typically dominated by decimation filters group delay, should be ideally made comparable to (or lesser than) the data distribution latency. A preliminary performance goal of 10 µs BPM group delay was thus established. In order to reach this number, the FOFB update rate was set to 115 kHz (turn-by-turn rate divided by 5), which allows reaching 8.64 µs of BPM group delay with a simple Cascaded Integrator-Comb (CIC) decimation filter with two sections and one differential delay. Refinements to help lower the BPM delay, either by improving the decimation filter response or increasing the FOFB update rate, are under study.

CONCLUDING REMARKS

Several refinements on the Sirius RF BPM electronics, mainly on the analog part of the design, led to significant performance improvements. Critical specifications are now met with exceeding performance. The electronics has undergone tests with short length beam at SPEAR3 and proved to keep its performance figures with broadband BPM signals.

The third spin of the RFFE board has been launched to provide higher input power dynamic range and final enclosure form factor based on industrial standards. LTC2208-based FMC ADC board is in advanced development stage and should not require new hardware modifications. After the conclusion of this new R&D cycle, scheduled to be concluded by the end of the 2nd semester of 2014, the RFFE and ADC hardware efforts will be redirected for pre-series production of a complete Sirius's storage ring superperiod BPM system (12 BPMs) and long term reliability tests with beam at LNLS UVX storage ring.

Substantial integration work on the digital back-end will take place in the 2nd semester of 2014 and throughout 2015.

ACKNOWLEDGMENTS

The authors would like to thank Jean-Claude Denard, Boris Keil, Andrej Košiček, Jim Sebek and Grzegorz Kasprowicz for the always insightful discussions about BPM systems, and Donald J. Martin, Jim Sebek, Fernando da Silva Rafael and Antonio Carlos de Lira for their support during the technical visit to SLAC.

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ISBN 978-3-95450-141-0