UPGRADE DEVELOPMENT PROGRESS FOR THE CERN SPS HIGH BANDWIDTH TRANSVERSE FEEDBACK DEMONSTRATION PROCESSOR*

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Abstract

A high bandwidth feedback demonstrator system has been developed for proof of concept transverse intra-bunch closed loop feedback studies at the CERN SPS. The system contains a beam pickup, analog front end receiver, signal processor, back end driver, power amplifiers and kicker structure. The main signal processing function is performed digitally, using very fast (4 GS/s) data converters to bring the system signals into and out of the digital domain. The digital signal processing is itself implemented in an FPGA allowing for maximum speed and flexibility. The signal processor is a modular design consisting of commercial and custom components. This approach allowed for a rapidly-developed prototype to be delivered in a short time with limited resources. Initial beam studies at the SPS using the system prior to the CERN long shutdown one (LS1) have been very encouraging. Building on this success, we are planning several key upgrades to the system, including the signal processor. This paper describes these key upgrades and reports on their progress.

OVERVIEW AND UPGRADES TO THE DEMONSTRATION SYSTEM

The high-current operation of the SPS for HL-LHC injection will require mitigation of possible Ecloud and TMCI driven intability effects [1]. A single-bunch wideband digital feedback system (Fig. 1) was initially commissioned in November 2012 and used through the February 2013 SPS LS1 shutdown. During the CERN LS1 interval we are upgrading the Demonstration system to add functions necessary to validate a full-featured control system.

PHASE I UPGRADES

The Demo system [3] was rapidly developed in 2012 and the first operational version included a snapshot mode that captures 32000 turns of digitized bunch motion. This data can be processed offline to study beam motion in the frequency domain and see changes in the beam motion as the feedback parameters are varied. The original studies contained some hard to understand narrowband spectral features that were not from the beam, but instead from interactions with the SPS RF and timing systems, as well as some internal digital clocks which were visible roughly 8 - 10 dB above the digitizer noise floor. As part of the upgrade, the A/D boards were relocated within the system chassis, grounded to a common copper plate and the narrowband interferring signals are now neglible. Additional studies and development of the RF and sampling clock signals have also been completed and we anticipate the next round of measurements to be free of the spurious interferring signals.

The beam dynamics measurements use an excitation/response formalism with chirps applied to the beam while the response is recorded. In these first measurements the existing 4 GS/s excitation system [2] was used to excite the beam with an analog summation of the feedback signal into the power amplifier input. These measurements required careful synchronization and alignment of the excitation system, feedback system and beam signals. As an upgrade, we have integrated the excitation system function within the demo system, so that the same system clocks drive the excitation sequence and the DSP aquistion and filter functions, so the summation of the excitation signal and filter output is now a digital addition with controlled saturation and gain.

The second major improvement is a phase-locked loop for system clocks. The DAC device (Maxim Semi MAX19693) does not have a mechanism to resynchronze its 4:1 input data mux, for many frequency domain applicationsthis is not a concern. This arbitrary synchronization meant that the excitation sytem and DSP processing had to be manually timed for each set of measurements, or after any interruption of the system power or clocks. The upgraded system uses a phase lock technique to adjust the phase of the input clocks to the D/A so that the divided parallel data clock is always consistently syncronized to the beam. This important upgrade makes the system timing repeatable and consistent from measurement to measurement. It also provides a path for a future upgrade allowing energy ramping and compensation for vaiations in synchronous phase and system timing with acceleration. In conjunction with the new operating modes, the system operator's interface has been simplified and expanded.

WIDEBAND KICKER STRUCTURES AND POWER AMPLIFIERS

A kicker structure to apply correction fields to the beam is a critical system function. A July 2013 design report

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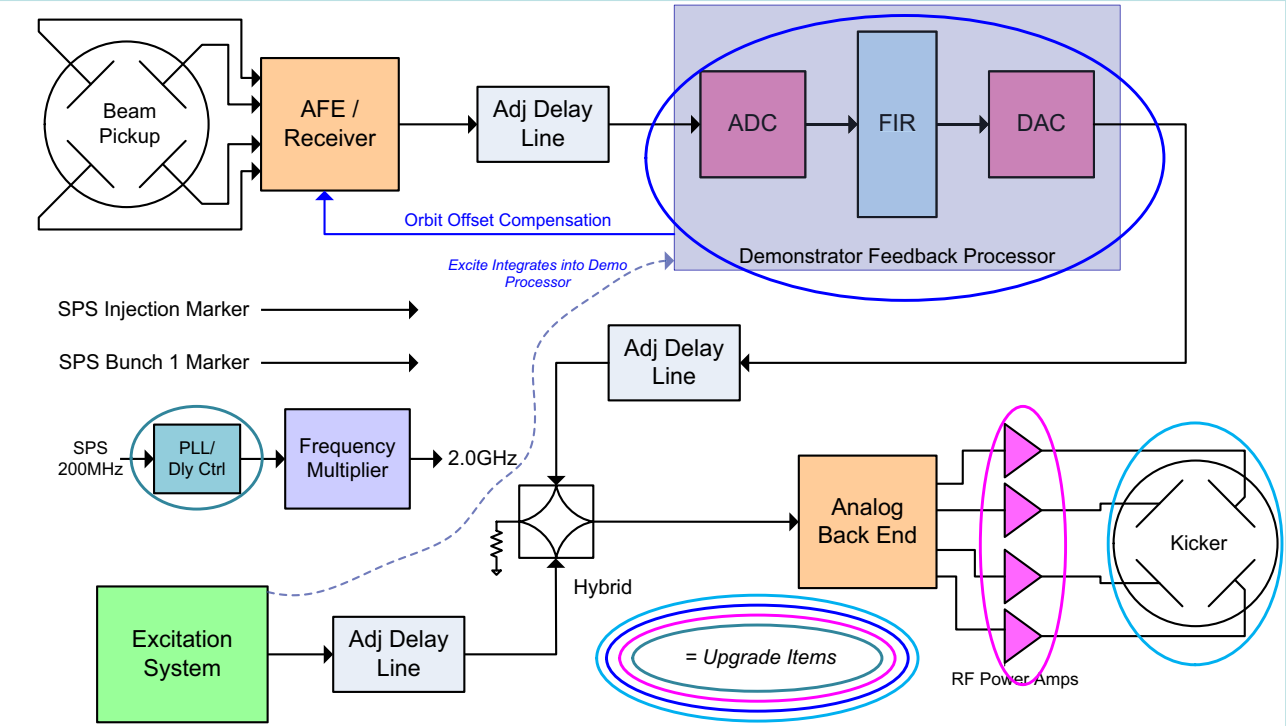

Figure 1: System block diagram highlighting the expansion in progress to the Demonstration system. The first expansions include combining the excitation and feedback functions within the DSP processing, the new wideband kicker structures and amplifiers, and the improvements to the high speed timing and synchronization to the SPS RF. The second phase of expansions will add control for a short 16 bunch train, and allow control of a special adjecent bucket scrubbing fill. Subequent efforts will increase the dynamic range of the input A/D functions through improved orbit offset rejection techniques, and implement synchronization of the beam/kicker signals throughout an energy ramp cycle.

summarized requirements and three possible technical implementations [4]. The stripline design is more mature, and three stripine kicker prototypes have been fabricated by CERN with the first kicker installed in August 2014. Figure 3 shows the first stripline kicker just before final assembly and installation. The slotline design is in the optimization phase, but should be fabricated starting winter 2015.

Either wideband kicker design requires suitable RF amplifiers to drive them. We have studied commercial RF amplifiers for possible use, with criteria of linear phase response and clean time response. After evaluating 8 possible amplifers, we have selected a 5 - 1000 MHz 250 Watt RF amplifier for the first tests with the new stripline kickers. Procurement is underway to have a pair available for beam tests in early 2015.

SECOND PHASE UPGRADES

A second upgrade is planned for integration at CERN starting January 2015. In this phased upgrade we will expand the system beyond the single bunch control capability to allow control of 16 bunches at the 25 ns separation. A related upgrade will implement control of two consecutive buckets (5 ns separation) used in special scrubbing fill.

The receiver $\Delta\Sigma$ processing generates individual bunch slice error signals, but orbit offset still appears and must be budgeted in the input dynamic range (the offsets are removed by the filter processing and do not appear at the output). We are exploring two co-methods to increase the input dynamic range through orbit offset rejection.

TECHNOLOGY IMPLEMENTATION ROADMAP

The goal of developing a full-function instability control system for the SPS is envisaged to span two generations of prototype hardware. Fig.2 shows a multi-year program to expand the Demonstration system, validate the kicker and control technologies, and learn from the SPS MD experiments. We plan future reconfiguration of the Demonstration system to allow studies of both IIR and FIR filter approaches. Additionally the dual ADC structure of the system can be split to allow two independent pickups, with each running at a reduced 2 GS/sec. rate. This path would allow measurements and system tests of the two pickup method if the simulations suggest the control is more robust at the higher effective sampling rates from two pickups.

In parallel, we want to explore a second hardware platform, based on a higher sampling rate A/D and D/A processing system, with associated higher-capacity FPGA processing functions. This increased processing capacity may be needed to support architectures with multiple pickups, or possible two-channel processing streams which use both the Δ signal (beam motion) and the Σ signal (bunch

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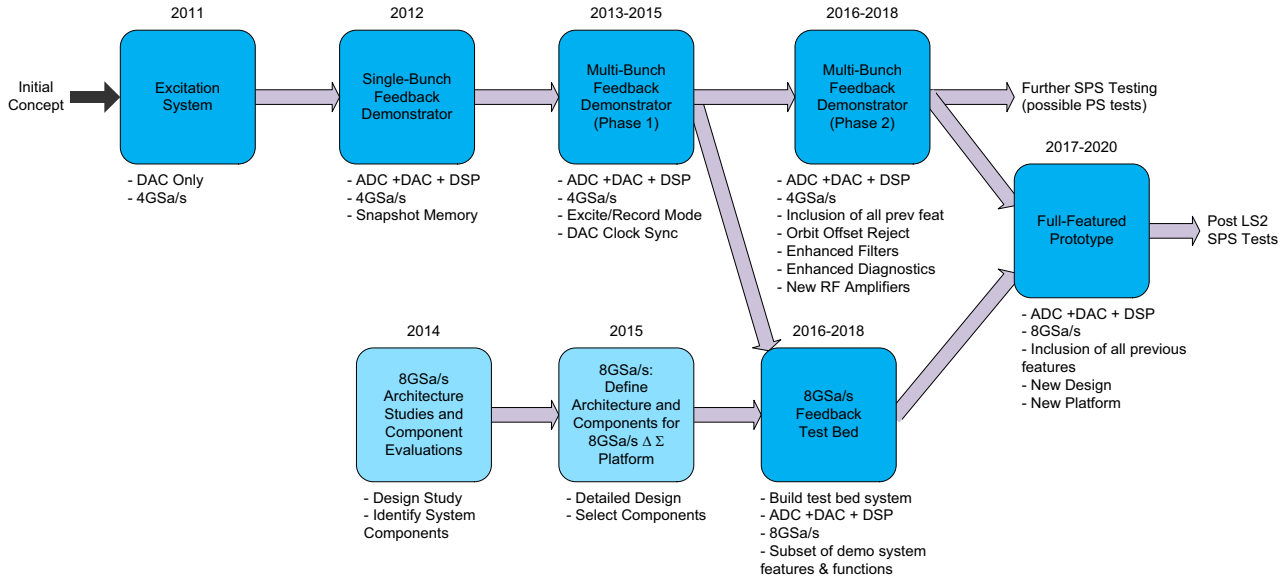

Figure 2: The technology development plan for the LARP Wideband Feedback effort, showing the path of expansion of the Demonstration system, and a parallel technology path with a higher sampling rate. We anticipate that the operational experience from the demonstrator system will guide the features to be implemented in the full-featured prototype in 2017.

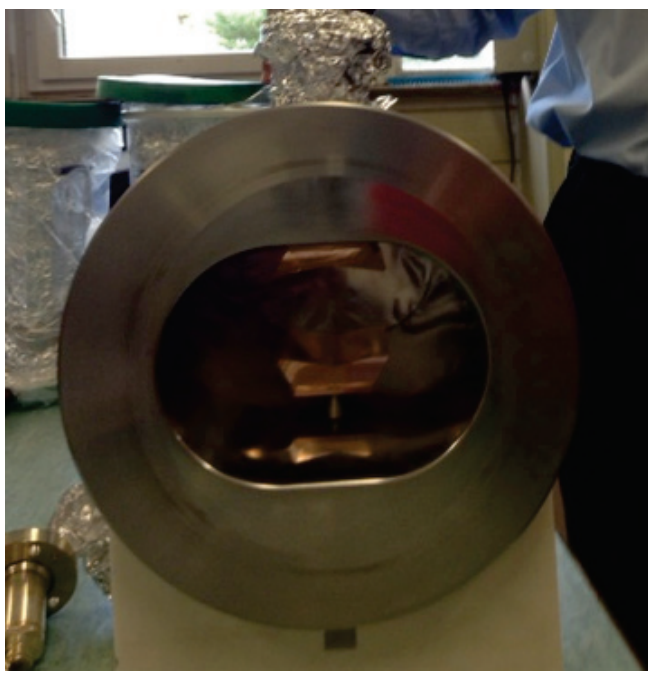

Figure 3: The first completed stripline kicker module for installation in SPS. The beam line vacuum system has been developed to allow 3 stripline kickers, as well as two slotline kickers, for beam testing. Dummy vacuum sections are in place to allow rapid and efficient installations of the third stripline kicker and a future slotline kickers.

charge) as part of the computation of a correction signal.

SUMMARY AND PLANS FOR NEXT MD STUDIES

The upgraded demonstration system will be recommissioned at the SPS in Fall 2014, with the new wideband kickers starting in 2015. We should be able to demonstrate control of 16 bunch trains and study the necessary bandwdiths for the pickup and kicker functions. Studies, and comparisons with beam instability simulations, are vital to predict the operation and margins of this beam feedback at the anticipated HL intensities and filling patterns. We plan on continuing to add features to the demonstration prototype while in parallel developing the platform for the full-featured prototype system to be commissioned after the LS2 shutdown.

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REFERENCES

[1] E. Shaposhnikova, "Intensity Upgrade Plans for CERN-LHC Injectors", 42nd ICFA Advanced Beam Dynamics Workshop Nashville, Tenn., USA, 2008, CERN-AB-2008-065.

[2] J. D. Fox, *et al.*, "A 4.2GS/sec. Synchronized Vertical Excitation System for SPS Studies - Steps Toward Wideband Feedback", IPAC 2012.

[3] J. E. Dusatko, *et al.*, "The Hardware Implementation of the CERN SPS Ultrafast Feedback Processor Demonstrator", MOPC28, IBIC 2013.

[4] J. M. Cesaratto, *et al.*, "SPS Wideband Transverse Feedback Kicker: Design Report," SLAC-R-1037.

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