FAST ORBIT FEEDBACK SYSTEM AT THE AUSTRALIAN SYNCHROTRON

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Abstract

Since the end of commissioning of the facility in 2006, implementing top up (completed 2012) and fast orbit feedback have been top priority upgrades to improve the stability of the light source for users. The fast orbit feedback system is currently being implemented and will be commissioned late 2015. The feedback system has a star topology with an FPGA based feedback processor at its core. The system will utilise the existing 98 Libera Electron beam position processors, with Libera Grouping for data aggregation, as the source of position data at 10 kHz. The corrections are calculated in a Xilinx Vertex 6 FPGA and are transmitted to 14 corrector power supplies in the 14 sectors. These power supplies are six-channel bipolar 1 Ampere and have been developed by a local company. The corrector magnets are tertiary coils on the existing sextupole magnets in the storage ring. This report shall present the design, results of Simulink simulations, the current status of implementation and future plans.

INTRODUCTION

The Australian Synchrotron (AS) is a 3rd generation light what was commissioned in 2006 [1]. The storage ring is a 14 fold symmetric Chasmann-Green lattice with leaked dispersion. In each of the 14 sectors there are 7 beam position monitors (BPMs) giving a total of 98 BPMs [2].

As the technology and techniques on the beamlines mature, their sensitivity to source stability has increased. The stability requirement at the AS is to maintain the transverse beam motion to be less than 10% of the beamsize at the source. The tightest constraint on the beam motion is at the insertion device straights where the beamsize is the smallest. With the nominal configuration (optics) the one sigma beamsize is 320 µm horizontally and 16 µm vertically at 1% emittance coupling and 5 µm for the natural coupling of 0.1%. The integrated motion at the insertion device straights is shown in Figure 1 where in the vertical plane the beam motion exceeds 10% of the vertical beamsize of 16 µm at 100 Hz.

The fundamental requirement for the fast orbit feedback (FOFB) system is to reduce the beam motion to less than 10% of the beamsize up to 100 Hz [3]. To achieve this the system was designed to try and meet a closed loop bandwidth of 300 Hz. However as shall be shown this was always going to be challenging. The second design requirement was to, where possible, reuse the existing infrastructure and equipment. The following sections will introduce the design of the system, the results of simulation studies, the different subsystem and the current state of the project.

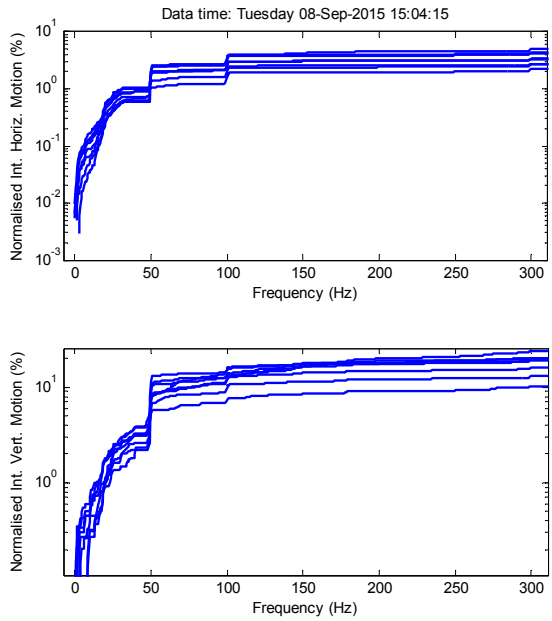

Figure 1: Integrated beam motion at all insertion device straights normalised to the beamsize in percent (320 µm and 16µm). The largest contributor to the perturbation on the beam is the 50 Hz mains frequency. At 100 Hz the integrated beam motion in the vertical plane exceeds 10%.

DESIGN

The design of the system can be broken down into 3 sub-systems as shown in Figure 2: (1) beam position measurement and aggregation, (2) feedback controller and (3) corrector magnets and power supply.

Beam Position Measurement

The beam position in the storage ring is measured using Instrumentation Technologies' Libera Electron beam processor. The processors have a real-time stream of position data at 10 kHz (Fast Acquisition data) and are aggregated across the 98 BPMs by using Libera Grouping [4]. The topology of Libera Grouping implemented here is a single a ring with one level of redundancy. The Libera Electrons transmit 98 horizontal and 98 vertical positions at a rate of 10 kHz via UDP using a GbE link.

Feedback Controller

The feedback controller receives the data, decodes packet information and translates this into corrector current values using an inverted BPM-Corrector response matrix. In the first instance the controller will be a single

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global P controller. The corrector current values are then sent to the magnet power supplies via optical fibres using a serial protocol. The chosen platform for the controller is a Xilinx Vertex 6 FPGA (on a development board).

The choice of an FPGA platform was two-fold, a strategic decision to build expertise within the Australian Synchrotron in developing on such platforms as well as the future potential of such a system to do more intensive computations without significantly compromising on the system performance.

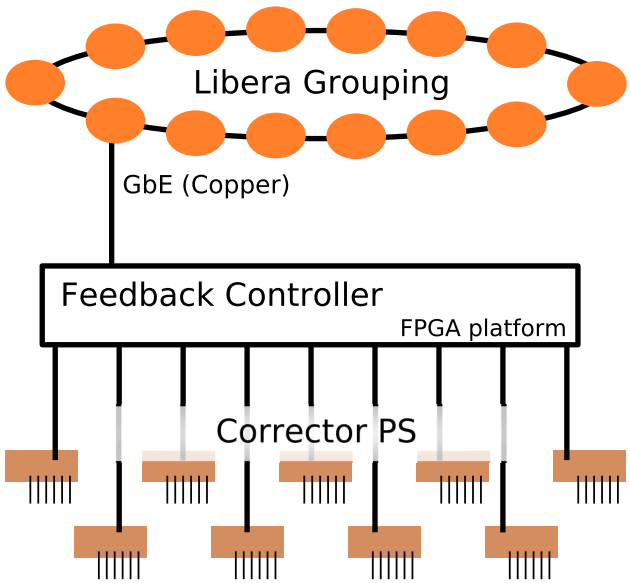

Figure 2: The three sub-systems are: (top) beam position measurement and aggregation, (middle) feedback controller and (bottom) power supplies connected to tertiary coils on the sextupole magnets.

Corrector Magnets and Power Supplies

There are three Horizontal "Fast" Corrector (HFC) and three Vertical "Fast" Corrector (VFC) in each of the 14 sectors giving a total of 84 "Fast" corrector magnets in total. These corrector magnets are tertiary coils installed on the existing sextupole magnets in the storage ring.

In the development of the design for the FOFB system the following were considered:

1. Replacing or modifying existing corrector magnets: this would have been too costly and risky.
2. Trim power supply in series: this was tested however the interaction between the slower and trip power supply introduced instabilities as certain frequencies.
3. Independent freestanding corrector magnets and power supplies: new magnets just around the insertion devices, not insignificant cost of magnets and stands.
4. Independent coils on sextupoles and power supplies: lower cost of magnets and can have correctors in the arcs. Trade off lower bandwidth due to the vacuum chambers.

The decision was made to use the coils on the sextupoles due to the lower cost and distributed nature.

LATENCIES

To estimate the bandwidth of the system it is necessary to quantify the latencies in the system. To measure the latencies of the system a simplified prototype of the feedback controller was developed to decode the position data from the Libera Electron and to output a digital signal which is triggered when the reported position changes. The change in the position is systematically created by a 10 Hz pulse that attenuates one of four input signals to the Libera Electron resulting in step changes to the position at a rate of 10 Hz. By measuring the delay between the onset of the pulse and the digital output from the comparator it is possible to measure the latency of the Libera Electron processor and position aggregation (see Figure 3). After 12000 samples the spread of the latency showed an equal distribution between with a minimum of 86 µs and a maximum of 191 µs. In the following analysis and simulations we have assumed a conservative latency of 200 µs to account for the Libera Electron processing and aggregation. The Libera Grouping's data packet contains data for 98 BPMs with a total of 1610 bytes (including headers). At 1 Gbps the transfer time is 13 µs.

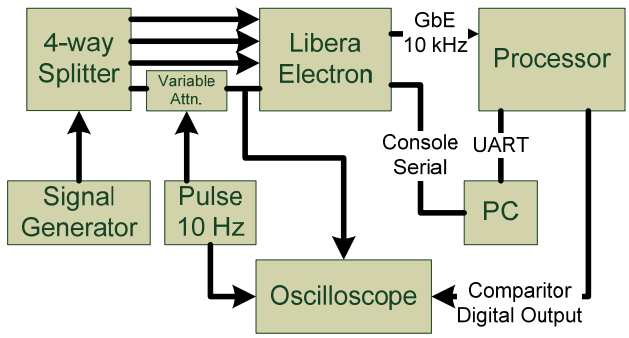

Figure 3: Setup used to measure the latency of the Libera Electron processor and the position aggregation. The pulse attenuates just one of four of the 500 MHz RF signal to the Libera Electron. The result is a step change in the position. By setting the appropriate level the comparator output will indicate when the reported position on the 10 kHz data stream changes.

Another system that can be quantified is the response of the vacuum chamber. Due to the screening effect of the 3 mm thick stainless steel vacuum chamber walls it acts as a low pass filter. The cut-off frequency was measured and shown to be 400 Hz and 1000 Hz in the horizontal and vertical planes respectively (see Figure 4).

Figure 5 shows all the known latencies in the system as well as the screening effect of the vacuum chamber. This is the fundamental limit of the feedback system. At the start, conservative limits were placed on latencies of the systems that we would be implementing (processor and the power supplies).

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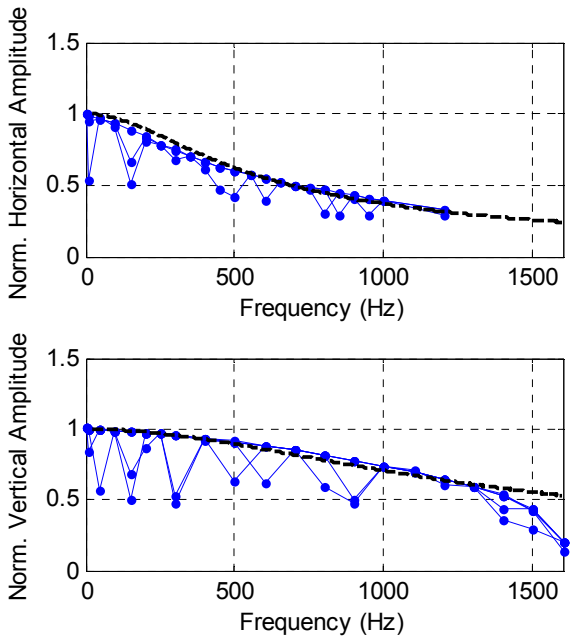

Figure 4: Measured peak amplitude of the closed orbit perturbation as a function of frequency. The corrector magnet was driven with a sinusoidal current at a constant peak amplitude of 230 mA at different frequencies (solid lines). Simulated low pass filter with a cut-off frequency of 400 Hz (H) and 1000 Hz (V) shown as a dashed line.

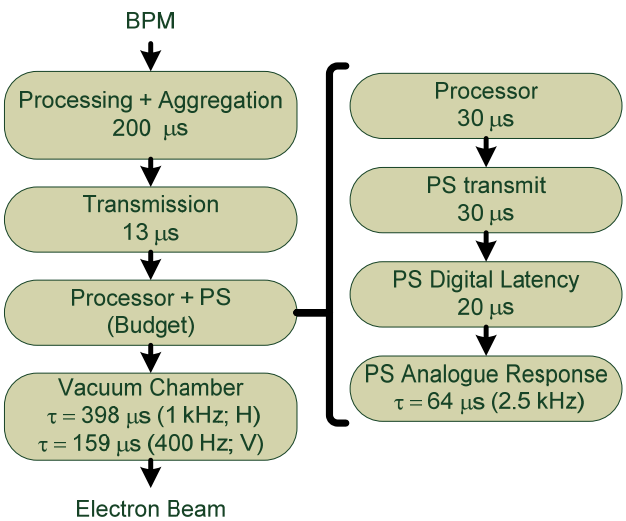

Figure 5: Summary of the estimated latencies in the various sub-systems that are fixed and the budgeted latency for the processor and power supply.

SIMULATIONS

With the above assumptions a Simulink model was created to determine the closed loop bandwidth of the system. To simulate the disturbance, 2 seconds of real position data was collected. The fast acquisition (FA) data (10 kHz) was streamed to a PC running Diamond's Fast Acquisition Archiver [6] to store and later retrieve data. A whole ring response matrix was calculated using a model of the Storage Ring using the Accelerator Toolbox (AT) [7]. The whole ring response places dipole perturbation terms in all the quadrupole and sextupole locations creating a total of 182 parameters. By using the whole ring response, the perturbations, including noise on observed on the storage ring can be modelled by 182 parameters.

The Simulink model shown in Figure 7 takes into account the fixed and budgeted latencies (Figure 5) as well as models the feedback controller and responses of the power supply and the vacuum chamber. The comparison of the closed loop gain in both planes is shown in Figure 6. Using this result the estimated bandwidth of the feedback system is 220 Hz and 310 Hz in the horizontal and vertical planes respectively.

The current design only implements a simple P controller however if the implementation over the coming months go well we will investigate the feasibility of implementing a PI or modal controller [8].

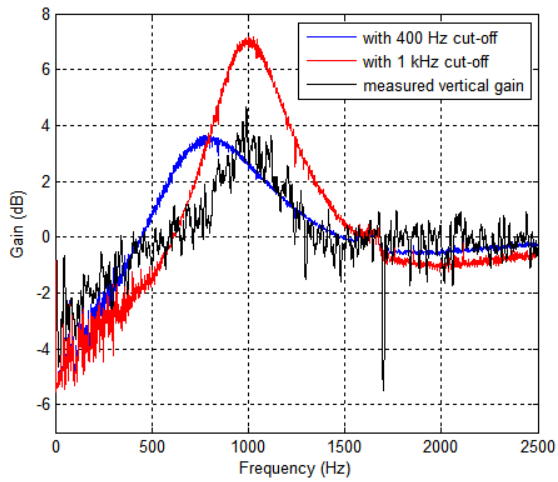

Figure 6 Simulated closed loop gain of the feedback system in both planes with the two differ cut-off frequencies of the vacuum chamber and measured vertical gain with a prototype controller. The closed loop bandwidth is estimated to be 220 Hz (Horizontal; blue) and 310 Hz (Vertical; red). Above 450 Hz (Horizontal) and 610 Hz (Vertical) perturbations are amplified. All of the above use a P coefficient of 0.9.

Prototype Test

Early in the project a prototype of the feedback controller was developed to test various components (ability to decode the Libera data packets, matrix multiplication, P controller and control of the power supplies) and determine if we could do it on an FPGA. In this test only two correctors were used in the feedback loop and results shown in Figure 6 (black) compare reasonably well with the simulations. It so happened that the power supply that we were trialling (ITEST Bilt power module) had a bandwidth ~2.5 kHz, latency of 50 μs, transmission latency of 20 μs.

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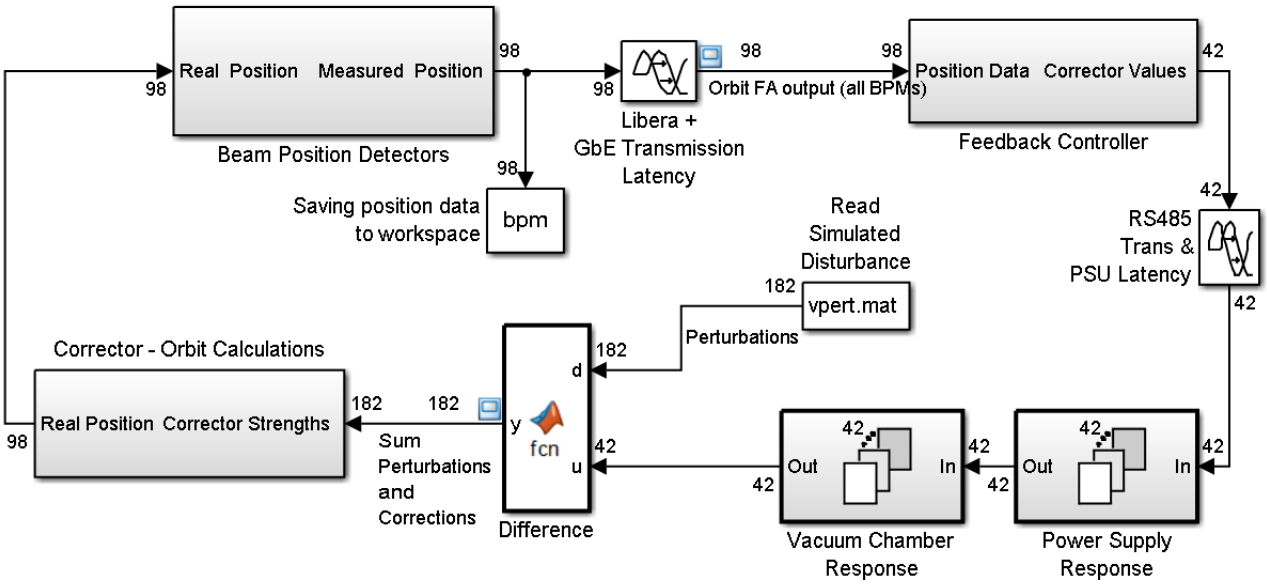

Figure 7: Simulink model of the feedback system. The perturbations are simulated by distributed dipole kicks around the ring (modelled with 182 parameters) which is converted back into position (bottom left). The BPM processors include a 220 µs transport delay (top left). The feedback processor uses an inverted fast corrector-BPM response matrix to calculate the corrections needed with a P controller (top right). The power supply is modelled by a fixed transport delay of 80 µs and a low pass filter of 2.5 kHz. The vacuum chamber is modelled by a low pass filter of 400 Hz and 1000 Hz for the horizontal and vertical planes (bottom right).

FEEDBACK CONTROLLER DESIGN

The feedback controller on a built on a Virtex 6 FPGA will be connected directly to the controls system and to a Libera Electron for the FA data (10 kHz position data). The design philosophy is to modularise the functionality as much as possible to ensure future modifications are simplified. A schematic of the design is shown in Figure 9. The control system's EPICS IOC will communicate with the controller via a GbE connection.

The primary processing chain decodes the data packet from the Libera Electron to extract the transverse position ID and status data. The transverse position is sorted by id number to form a vector to be multiplied by the inverse response matrix and scaled by a proportional factor, P. When all corrector values are updated a signal is given to the UART handler to transmit the data via the digital IO channels on the FMC. A separate daughter board has been developed to transmit the UART data to the power supplies via optical fibre links (see below).

The system operates in three modes: stop/initial, run and diagnostic. The parameters can only be updated when in the stop mode, (no queuing feature has been implemented). The data is processed when in run mode and in diagnostic mode the user can set the input position vector and/or the calculated corrector values. A software trigger then forces the calculation of the corrector values based on the input position values and another software trigger can be set to transmit the corrector values. In all modes it is possible to request a snapshot of the position data and corresponding calculated corrector values.

The modularity will ensure that future algorithms can be easily added to the system and eventually utilise the on-board 1GB DDR RAM to create a circular buffer to store diagnostic data.

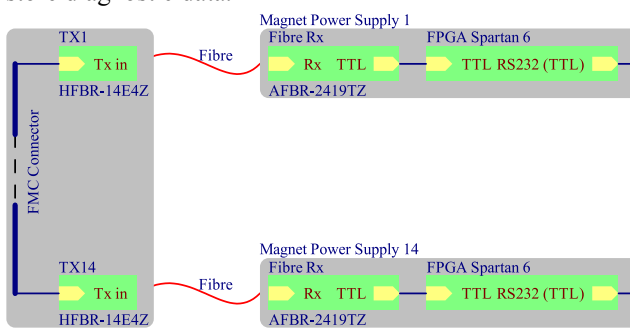

Figure 8: FPGA controller to power supply communications modules using optical fibres. The system has been tested at a baud rate of 10 MBps.

Power Supply Communications

To transmit the corrector values to the 14 power supply units a daughter board was designed to transmit the UART data via optical fibre. The transmitter uses a custom encoding scheme to pass the data to an optical receiver on the power supply at a baud rate of 10 MBps.

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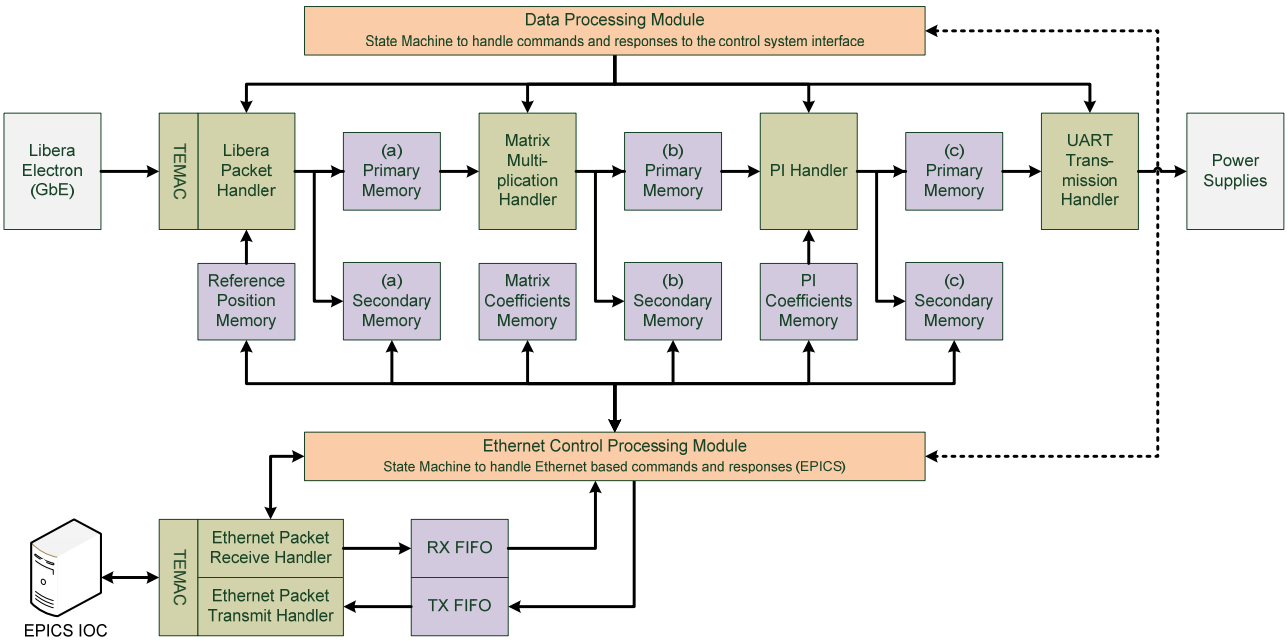

Figure 9: Feedback controller design.

POWER SUPPLY

The power supplies have been developed locally by DETECT and have supplied the AS with 15 units (1 spare) with performances listed in Table 1. These have been delivered and tested at the AS and has been shown to perform well. In some instances the actual performance exceeded the specifications by a large margin. For example the long term stability was measured at 400 mA ±70 uA and the temperature coefficient was < 100 ppm/°C. The system latency was also measured at 31 us and the bandwidth at amplitude of 400 mA was close to 4 kHz.

Table 1: Specifications for the FOFB Power Supplies

Total number of channels	84 (14 units × 6 ch)	
Output Current	± 1.0 A, bipolar	
Load Inductance range (@ 100 Hz)	0.99 mH	2.7 mH
Load Series Resistance*	1.4 Ω	2.4 Ω
Setting and readback current resolution better than	1 mA	
Current accuracy	50 mA	
Current noise, 10 kHz bandwidth	< 0.3 mA (300 ppm)	
Long term stability (8 hr)	± 0.3 mA (300 ppm)	
Temperature coefficient	< 300 ppm/°C	
Setting data rate	10kHz	
Minimum bandwidth with maximum load†	> 2.5 kHz	
Max latency (end data arrival to DAC output)	50 us	

* Including resistance of wire from the power supply rack to the magnet coils. Minimum of 0.6 Ω Maximum of 1.1 Ω.

† AC with peak amplitude of 0.4 mA (peak-peak of 0.8 mA) into an inductive load of 2.7 mH and 2.4 Ω.

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