

CHARACTERISING THE SIGNAL PROCESSING SYSTEM FOR BEAM POSITION MONITORS AT THE FRONT END TEST STAND*

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Abstract

A number of beam position monitors (BPM) are being installed at the Front End Test Stand (FETS) H^- ion source at the Rutherford Appleton Laboratory, UK, as part of the 3 MeV medium energy beam transport. The FETS ion source delivers pulses up to 2 ms long at a rate up to 50 Hz and a maximum current of 60 mA, with a 324 MHz micro-bunch structure imposed by the frequency of the FETS RF acceleration cavity. The response of an in-house designed button BPM has been simulated and then characterised on a wire-based test-rig and the results are presented. The output from a custom algorithm running on a commercial PXI-based FPGA signal processing system is evaluated using test signals from both a function generator and the BPM in the test-rig, to verify the speed and precision of the processing algorithm. The processing system can determine the beam position in eight BPMs, with a precision of better than 20 μm , within one microsecond of the signal sampling being completed.

FETS BPMS

Eight BPMs are being installed in the FETS medium energy beam transport (MEBT) after the radio-frequency quadrupole (RFQ). Six of the BPMs are in-house designed button BPMs that have been described previously, along with a description of the wire-rig [1]. The remaining two BPMs are strip-line types that are manufactured to a design from the LINAC4 group at CERN, Geneva [2]. The prototype button BPM was originally tested using a wire-rig (Fig. 1), with the output from the electrodes being acquired by a four-channel oscilloscope, the data then being read and analysed to produce a wire position in the x and y axes.

The beam (or wire) position in X and Y is given by Eqn. 1 and 2, where V_{right} , V_{left} , V_{up} and V_{down} are the voltages as measured on the right, left, up and down electrodes respectively. The constants S_x and S_y are the sensitivities for the relevant axes, d_x and d_y are the relevant position offsets.

$$Position_x = \frac{1}{S_x} * \frac{V_{right} - V_{left}}{V_{right} + V_{left}} + d_x \quad (1)$$

$$Position_y = \frac{1}{S_y} * \frac{V_{up} - V_{down}}{V_{up} + V_{down}} + d_y \quad (2)$$

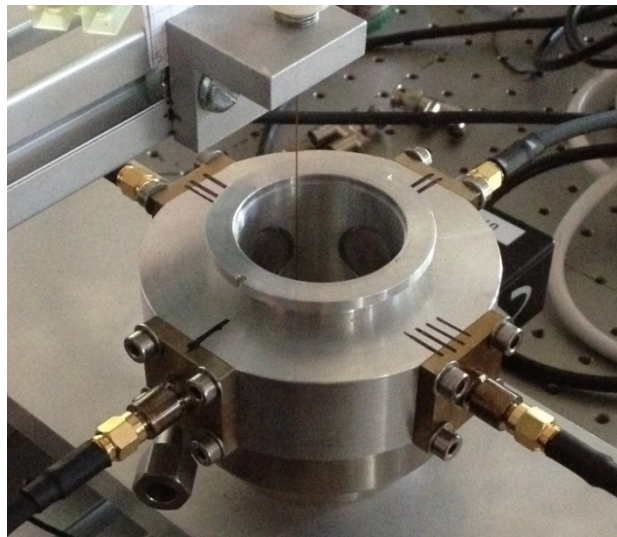


Figure 1: Prototype button BPM on the wire-rig system.

Beam Position Requirements

The ion beam rms width varies as it traverses the MEBT, varying from around 1 mm to about 20 mm. The beam position is required to be known to a precision of better than 100 μm . The beam position during the rising edge of the macro-pulse moves around, due to the stabilisation time of both the pulsed ion source extraction voltage and the space charge compensation, so several position samples of the beam must be taken during this 50 μs period [3]. The position calculation must be completed within 1 μs to avoid result pile-up in the FPGA position-calculation section. The BPM is tested on the wire-rig, and the position calculated using the FPGA, to establish the constants S_x and S_y and the accuracy of each constant.

BEAM POSITION MEASUREMENT

The signal from each BPM electrode is down-mixed, using a single stage mixer, from 324 MHz to 10.125 MHz intermediate frequency (IF), using a local oscillator (LO) frequency of 313.875 MHz. The electronics used is based on a design used by the BPM development group working on the LINAC4 H^- accelerator at CERN. The output filter has been adjusted to take into account the different IF values.

Wire-rig and Ion Beam Signal Levels

The electronics has digitally-controlled amplifiers and attenuators before the mixer, and again after the low-pass

filter. The resulting IF signal is amplified and filtered, with a maximum output level of $2 V_{p-p}$. The simulated signal level from one electrode, with a 0.35 mm diameter wire in the centre of the BPM, is around $5.5 mV_{p-p}$ (≈ -40 dBm), rising/falling by a factor 1.126 when the beam is moved six millimetres towards and away from an electrode, as shown in Fig. 2.

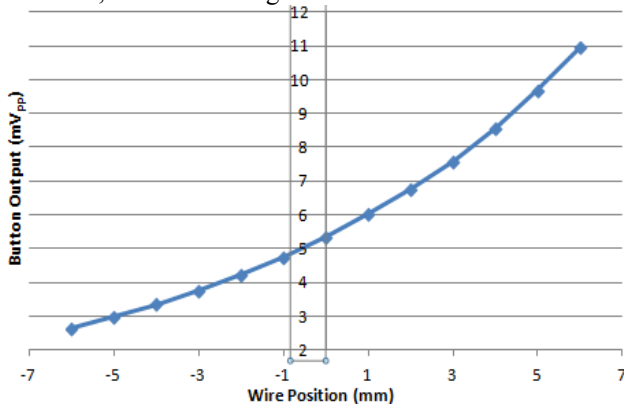


Figure 2: Simulated electrode signal level for a $\varnothing 0.35$ mm wire moving between -6 mm and +6 mm in the BPM.

The BPM electrode output from a macro-pulse of a centrally-positioned, 3 MeV beam at 60 mA has been calculated to be about $350 mV_{p-p}$ (≈ -5 dBm). The electronics has sufficient adjustment range to allow both testing using the wire-rig and operation with a real ion beam, allowing a maximum output level of $1V_{p-p}$ for the largest expected electrode signal. The displacement factor has been measured to be the same for both x and y axes, within the accuracy required.

Signal acquisition and IQ sampling

Since the beam position causes the electrode signal to only vary in amplitude and not frequency, the signal can be sampled at exactly four times the IF to obtain the signal amplitude, rather than many times per cycle. The sample rate is therefore 40.5 MS/s, which can be locked, using integer multiples and divisors, to the RF of 324 MHz and the LO of 313.875 MHz. The IQ sampling is shown Fig. 3.

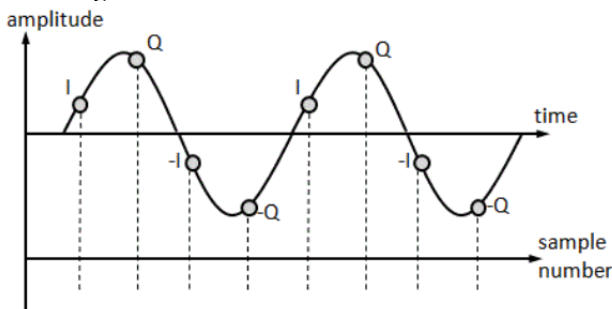


Figure 3: IQ sampling.

The amplitude and phase of the sampled signal is given by Eqn. 3 to 6. The peak amplitude for the positive and negative halves of the cycle are calculated independently allowing any possible offset to be assessed. The phase can

be used to determine the time-of-flight between successive BPMs in the MEBT.

$$V_{peak+} = \sqrt{I^2 + Q^2} \quad (3)$$

$$V_{peak-} = \sqrt{-I^2 + -Q^2} \quad (4)$$

$$\phi_+ = \tan^{-1}(Q/I) \quad (5)$$

$$\phi_- = \tan^{-1}(-Q/-I) \quad (6)$$

The BPM and electronics noise contribution is negligible to the required BPM position resolution.

DIGITIZER AND FPGA

A PXI-based FPGA card and a digitizer FPGA adaptor module (FAM), both manufactured by National Instruments (NI), are used for determining the beam position and phase using the mixed-down signals from the BPM electrodes. The specifications for the FPGA card, model PXI-7954R, and the digitizer FAM, model NI-5752, can be found in [4, 5]. The FPGA is used in a co-processing mode, which reduces the data load on the PXI chassis backplane and associated RT controller. Other beam-line instrumentation (beam current toroids and Laserwire), as well as the MEBT re-buncher cavity-control FPGA cards, will be added to the PXI chassis [6].

FPGA Programming

The PXI-7954R belongs to the Flex-RIO family of NI FPGA cards and contains a Xilinx Virtex-5 LX110 FPGA. During the BPM processing development phase, the PXI controller ran LabVIEW to enable fast debugging, but will be running LabVIEW Real-Time when the FETS beam-line starts, and will be responsible for control of the other beam-line diagnostics [6]. The position data is streamed from the FPGA card to the PXI controller using one DMA channel. The FPGA code is written in LabVIEW and uses the Xilinx compiler built in to the LabVIEW FPGA Module for code compilation and fitting. The code uses the default 40 MHz clock domain when running on the FPGA. The PXI-7954R and Digitizer FAM are shown in Fig. 4.

The processing code was initially simulated to see what size and speed of FPGA would be required to calculate the positions for eight BPMs, before a decision was taken on which FPGA card to use. The final code takes about 30% of the available FPGA resources, which allows sufficient headroom for further development.

Digitizer FAM

The NI-5752 is a 32-channel, 12-bit, simultaneously-sampled 50 MS/s digitizer module that attaches to, and is directly controlled by, a Flex-RIO FPGA card. Each of the 32 channels is connected to one channel of BPM electrode/electronics, with the channels sampled at 40.5 MS/s. Each digitizer channel signal should be in the range -1 V to +1 V. Signals a small amount outside this

range will be clamped, but large signals may destroy the device, so the mixer electronics is clamped to ± 1 V to ensure damage is avoided.



Figure 4: PXI-7954R FPGA card and NI-5752 Digitizer Adaptor Module.

Processing Method

At the start of the macro-pulse a synchronisation pulse starts the FPGA-controlled digitizer acquisition. At each rising edge of the sample clock, the sampled channel data is added to one of four FPGA accumulators, labelled I, Q, -I and -Q, on a round-robin basis. After 1024 sample clock edges (time), the accumulator result data is right-shifted by eight bits, equivalent to dividing each accumulator by 2^8 (256), and the resulting accumulator mean put into FIFOs ready for further processing.

Each output from the total of 128 means now has identical, parallel processing performed. Each mean is squared by multiplying with itself, added to its ‘partner’ squared mean (eg add BPM1 I^2 to Q^2 , $-I^2$ to $-Q^2$ etc), and the square-root of the resulting sum is calculated. The square-root results from opposite pairs of BPM electrodes are then divided to obtain a position ratio. The ratio is scaled by the relevant sensitivity factor, which has previously been loaded into a look-up-table (LUT). The resulting beam positions for both the positive and negative parts for each axis of all the BPMs is then DMA’d to the PXI host controller for distribution to BPM position client software. For phase of the BPM signal is calculated by taking the arctangent of Q/I and $-Q/-I$.

Position Calculation Time

The LabVIEW FPGA module has a set of functions, from the *high-throughput maths* palette, allowing deterministic operation on fixed-point numbers running on FPGA targets. Each function can be configured to accept a fixed-point number as input, and convert it if necessary, within the same clock cycle. Handshaking is used between functions to indicate when an operation has completed.

The multiplication and addition functions are all ‘single-cycle’ operations, meaning they take one clock cycle. One clock cycle for a 40 MHz clock is 25 ns. The number of clock cycles taken to perform square-root, division and arctangent functions is the number of bits describing the number which is being operated on.

To minimize the time taken for the bit-length dependent operations, each number is described using fixed-point

representation, the number of bits being sufficient to express the largest value that can occur. The digitizer interface reads out 256 12-bit numbers thus requiring 20 bits. After squaring and summing the $I^2 + Q^2$ value is described by 41 bits, but the output from square-root function is just 21 bits, and therefore requires 21 clock cycles, totalling 525 ns. The division of two 21-bit numbers requires 22 bits to describe its output, taking 550 ns. The beam position can therefore be calculated in 46 clock cycles, or 1.15 μ s using a 40 MHz clock.

Calculation Optimisation

There are several optimisations for the code and compilation parameters that can be made to reduce the position calculation time. The first is to increase the clock rate from 40 MHz for the functions taking the most clock cycles, namely the square-root and division operations. But increasing the clock rate makes the logic more difficult to fit into the FPGA, and a lot of the functions have been optimised for fitting using a 25 ns cycle time. Nevertheless a compilation has been completed using a 45 MHz clock, reducing the position calculation time by around 10%.

A further improvement in calculation time can be obtained by reducing the number of samples required for the mean, hence decreasing the number of bits that are necessary. The subsequent division and square-root functions will operate on a reduced number of bits, reducing the amount of clock cycles required. A reduced number of digitizer samples being used for the mean calculation means that more beam positions can be calculated during the macro-pulse. Table 1 summarises the beam sampling time, or interval between successive position determinations, and the corresponding number of clock cycles required for the calculation. The minimum sampling interval is 1.58 μ s to avoid calculation pile-up.

Table 1: Number of clock cycles required to calculate beam position for different sampling intervals

Sampling Interval (μ s)	Number of clock cycles	Processing time at 40 MHz (μ s)
25.28	46	1.15
12.64	44	1.10
6.32	42	1.05
3.16	40	1.00
1.58	38	0.95
0.79	36	0.90

A further decrease in processing time can be achieved by pipelining some of the high-throughput functions, meaning a subsequent calculation, or calculations, can be started before the previous calculation has finished.

BPM SYSTEM CHARACTERISATION

Calibration of the prototype BPM has been performed, firstly to check the function of the wire-rig apparatus,

BPM and the electronics, but primarily to measure the sensitivity constants, S_x and S_y . The results obtained when using the button electrode outputs were read directly by a four-channel, 8-bit, 2 GS/s oscilloscope showed large errors, since the quantisation noise is significant in the unamplified electrode signal of just a few mV.

The results from a single wire-rig measurement, using the down-mix electronics and the FPGA position calculation are shown in Fig. 5. The error for both x and y axes is less than 20 μm , a factor five better than the positional requirements. Further measurements indicate the linear region extends to around 4 mm from the BPM centre, maintaining a position error within 20 μm , which is in good agreement with the simulated value.

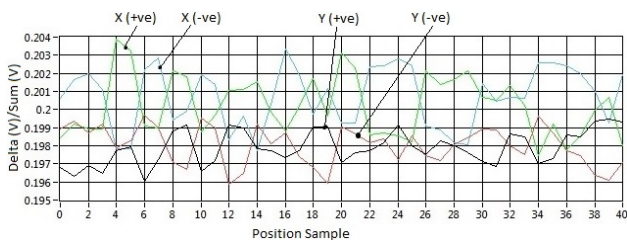


Figure 5: Measured wire position for x and y axes, for both positive and negative amplitudes.

There is a small discrepancy between the calculated, simulated and measured sensitivities. The simulated sensitivity axis is 1.03 ± 0.02 dB/mm compared with a measured sensitivity of 0.81 ± 0.14 dB/mm. The calculated sensitivity, using the formula in [7], for the FETS button BPM of 40 mm internal diameter and a button of azimuthal diameter 47° , is 1.67 dB/mm. The sensitivities are summarised in Table 2. The wire-rig and simulated sensitivities are in good agreement. The calculated sensitivity is somewhat higher than the simulated value, but the higher order terms have been neglected in the calculation.

Table 2: Summary of sensitivity values for different calculation methods

Calculation Method	Sensitivity (dB/mm)	Ratio	Difference wrt Simulation
Simulation	1.03	1.126	0%
Wire rig	0.81	1.098	-2.5%
Calculated	1.67	1.212	+7.6%

BPM INSTALLATION

The eight production button BPMs have now been manufactured, albeit with a slight misalignment between the axis of each electrode and their respective mounting holes, as shown in Fig. N. Rotating a BPM in its port by 180° reduces the axial misalignment to 0.1 mm with respect to the BPM axis. It is expected that a very small ‘tilt’ to the measured beam position will be apparent, although this can be corrected by rotating the BPM a slight amount during installation.

The wire position has been read from the LabVIEW real-time controller, to which the calculated BPM positions have been channelled from the FPGA, using network-published shared variables. The network loading passing position data to the BPM viewer client was negligible, and there was no pile-up of data in the RT controller, network or client. The beam position as measured by each BPM will be recorded, along with other beam-line diagnostic data, to monitor and improve the ion-source and beam-line performance.

CONCLUSION

The FPGA and digitizer FAM, along with the associated LabVIEW code, have proved to be part of a very effective beam position measuring system. The requirement for a readout position resolution of 100 μm was exceeded by a factor of five when testing the BPM on the wire-rig, and the total processing time of 1 μs allows for a large number of samples during a beam macro-pulse. By using faster clocks for some of the FPGA calculation functions, reducing the sampling interval and more efficient pipelining of functions it is estimated the calculation time can be reduced by around 50%.

The simulated and measured wire positions are in good agreement, and it is expected this agreement will extend to the actual beam position. Further characterisation of all the BPMs to be installed in the beam-line is currently taking place, and additional development of the wire-rig will also occur.

ACKNOWLEDGMENT

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