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HIGH-SPEED DIRECT SAMPLING FMC FOR BEAM DIAGNOSTIC AND ACCELERATOR PROTECTION APPLICATIONS

J. Zink*, M. K. Czwalinna, M. Fenner, S. Jablonski, J. Marjanovic, H. Schlarb
DESY, Hamburg, Germany

Abstract

The rapid development, in the field of digitizers is leading to *Analog-to-Digital Converters* (ADC) with ever higher sampling rates. Nowadays many high-speed digitizers for RF applications and radio communication are available, which can sample broadband signals, without the need of down converters. These ADCs fit perfectly into beam instrumentation and diagnostic applications, e.g. Bunch Arrival time Monitor (BAM), klystron life-time management or continuous wave synchronization. To cover all these high-frequency diagnostic applications, DESY has developed a direct sampling FMC digitizer board based on a high-speed ADC with an analog input bandwidth of 2.4 GHz. A high-speed data acquisition system capable of acquiring 2 channels at 500 MS/s will be presented. As first model application of the versatile digitizer board is the coarse bunch arrival time diagnostics in the free electron laser FLASH at DESY.

INTRODUCTION

Modern linear accelerators require a very high precision *Low-Level-RF* (LLRF) control system. In the *European X-Ray Free Electron Laser* (XFEL) and *Free-Electron-Laser in Hamburg* (FLASH) the LLRF-systems are realized in *Micro Telecommunication Computing Architecture* (MTCA.4). In addition to the control system the accelerators need very high accuracy diagnostic systems to measure, e.g. the beam position, the bunch arrival time , klystron failures, and other accelerator parameters. To reduce the board space and the

Figure 1: New DFMC-DS500 digitizer board.

number of components in the system, the authors designed a digitizer board based on an ADC with a maximum sampling rate of 1 GS/s. The new digitizer board (see Fig. 1) in ANSI/VITA 57.1 2010 [1] FMC form factor will be used in different diagnostic applications. It is integrated in the existing MTCA infrastructure and installed on a DESY *Advanced Mezzanine Card* [2] DAMC-FMC25 [3] carrier board. Due to the high input bandwidth of the digitizer, there is no need for a down converter stage in front of the ADC.

FMC DIGITIZER DFMC-DS500

The core component of the converter board is a dual channel 12-bit RF sampling ADC from Texas Instruments with a sampling rate of 500 MS/s per channel. In *dual edge sampling* (DES) mode the two channels are combined together and the ADC is sampling at 1 GS/s. The minimum guaranteed single channel analog bandwidth is 2.4 GHz. In DES mode the bandwidth is decreased down to 1.2 GHz. Since the manufacturer offers a whole family of compatible ADCs, different variants can be fitted onto the FMC [4].

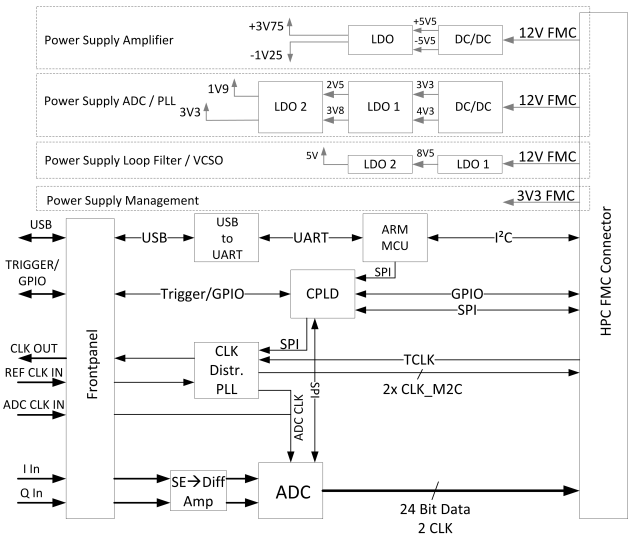

Figure 2: Block diagram of the DFMC-DS500 digitizer.

Figure 2 depicts the block diagram of the digitizer board. The inputs of the ADC are driven by fully differential amplifiers (FDA) [5, 6] with a large-signal bandwidth of 4.8 GHz. These amplifiers act as active baluns and replace the transformers which are normally converting single ended input signals to differential signals. The ADC has two 12-bit wide *low voltage differential signaling* (LVDS) data connections to the carrier card to achieve minimal latency. These lines can be driven with well defined voltage levels independent from the level of the adjust voltage (V_{ADJ}) [1].

Clock Tree

Clocking the ADC can be done in different ways. In addition to a direct clock feed via a front panel connector,

* johannes.zink@desy.de

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there is a *phase-locked loop* (PLL) located on the board which can be locked to an external reference clock or to an on-board high-precision, high-stability 10 MHz reference oscillator.

Management

An ARM *micro controller unit* (MCU) realizes the management. Main task of the MCU is power management and writing initial configurations into the ADC and the PLL after power on before a *Field Programmable Gate Array* (FPGA) located on the carrier takes over control. To translate several control signals into the V_{adj} voltage domain a small *Complex Programmable Logic Device* (CPLD) with four input-/output banks is part of the board management.

DATA ACQUISITION SYSTEM

To evaluate the DFMC-DSx00 FMC mezzanine board, a data acquisition (DAQ) system was developed for Xilinx KCU105 evaluation kit and for DAMC-FMC25 AMC board. The DAQ system consists of firmware (FPGA part) and software. The KCU105 board is plugged in an industrial PC, which provides PCIe interface to the FPGA. Similar arrangement is used for DAMC-FMC25, which provides PCIe interface to an in-crate CPU AMC board.

Firmware

The main building blocks of the firmware on KCU105 are depicted in the Fig. 3.

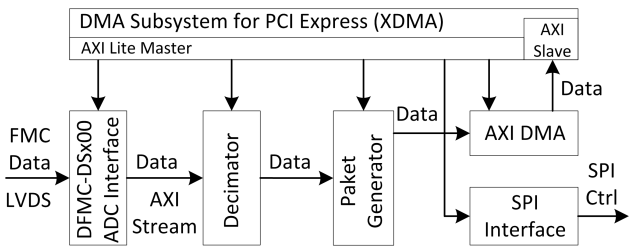

Figure 3: Schematic view of Firmware building block.

DFMC-DSx00 ADC Interface The ADC interface is responsible for capturing the data from parallel LVDS bus. This module takes advantage of IDELAY and ISERDES blocks in Xilinx Kintex UltraScale devices. A Built-In Self Test state machine determines the optimal settings of delay chains upon start-up and on user request. The output of the ADC module is 128-bit wide AXI-Stream interface, with four samples in parallel for each channel.

DFMC-DSx00 SPI Interface The SPI interface provides communication with components (CPLD, ADC, PLL) on the DFMC-DSx00 mezzanine board. The CPLD provides status information and also the board hardware and firmware version information. The SPI interface can also be forwarded to on-board ADC and on-board PLL, e.g. to retrieve the status information and to change the configuration of the said devices.

Packet Generator The packet generator module prepares and packages the data from ADC module in a format, suitable for AXI Direct Memory Access module.

AXI Direct Memory Access Xilinx AXI DMA module is used to transfer the data from ADC into on-board DDR4 memory. Attached to the AXI DMA is a small BRAM memory, where the descriptors for the DMA engine are stored. Up to 100 million samples (0.2 second at 500 MS/s) can be stored in the DDR4 memory, providing excellent resolution in frequency domain.

DMA Subsytem for PCI Express Xilinx DMA Subsytem for PCI Express is used to provide an access to configuration and status registers in all previously-described modules. It also provides high-throughput DMA access between on-board DDR4 memory and CPU memory.

Software

Ubuntu 16.04 LTS is running on the industrial PC. A driver is provided by Xilinx to communicate with FPGA registers and with Xilinx DMA Subsytem for PCI Express. On top of the driver a Python library (`dsx00lib`) and a command-line interface (`dsx-cli.py`) were developed. The command-line interface provides several useful commands for evaluating the FMC mezzanine; the most useful feature is the possibility to dump the data into a (compressed) file. Data can be later elaborated with user's software of choice.

COARSE RF BAM CHANNEL

In FLASH and XFEL accelerators an electro-optical BAM is installed and measures the bunch arrival time. This system has very high accuracy and can determine the arrival time with femtosecond precision [7]. If the BAM is power cycled or a loss of optical synchronisation or large timing jumps of electron bunches occur, the BAM system has to be setup. This procedure is time consuming and requires a specialist. To simplify the setup of the BAM system, a second coarse RF BAM system with picosecond accuracy is planned. This system will provide a coarse bunch arrival time to the optical BAM system to automatically adjust the the optical delay lines [7].

Beam Pick Up

Figure 4 shows the coarse RF BAM system. The RF BAM system uses the same combined broadband pick up signals like the optical BAM system [8]. By combining two opposite pick up signals together the signal dependence on the bunch transversal position is reduced [7, 9]. Before the combined signal is fed into the optical BAM system, a second signal for coarse RF BAM channel is decoupled. Figure 5 depicts the expected waveform and the dependency of the amplitude to the bunch charge. The signal has a high bandwidth of 40 GHz and has a theoretical resolution of 5 - 10 fs [7].

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Analog Front End

A 10 dB coupler produces the signal for the coarse BAM analog front end (AFE). The front end consists of different attenuators, amplifiers and filtering stages. The signal bandwidth and the amplitude is very high and cannot not be directly processed by the DS500 digitizer. Thus in the first stage the signal is attenuated by 5 dB and filtered. The low pass filter has a cut-off frequency of 2.5 GHz followed by a band pass filter with a center frequency of 2.383 GHz and a band width of 80 MHz. After reducing the bandwidth to 2.4 GHz the signal is amplified, high pass filtered and attenuated to prevent oscillations between the amplifiers. The digital step attenuator allows to fit the signal level to the full scale range of the ADC. After another amplifier stage there is a power limiter which protects the following ADC and driving stage against excessive overloading.

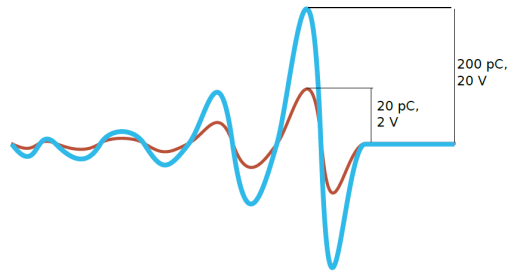

Figure 5: Dependency of the signal amplitude on the bunch charge. The amplitude increases with the bunch charge [7].

Sampling and Processing

Configuring the ADC in dual edge sampling (DES) [10] mode doubles the sampling frequency from 433 MHz to 866 MHz. A reference clock drives the PLL reference input on the DFMC-DS500. Trigger signals coming from the MTCA backplane activate the DAQ on the DAMC-FMC25 and a set of samples is taken by the FPGA. Acquired data can then be processed by the control system and can be used to automatically adjust the electro-optical BAM system for faster setup after machine restart.

RF BAM Measurement Setup

The final goal of the coarse BAM channel is to determine the bunch arrival time within the range of a few picoseconds. Pick ups at the beam line produce a complex high bandwidth waveform.

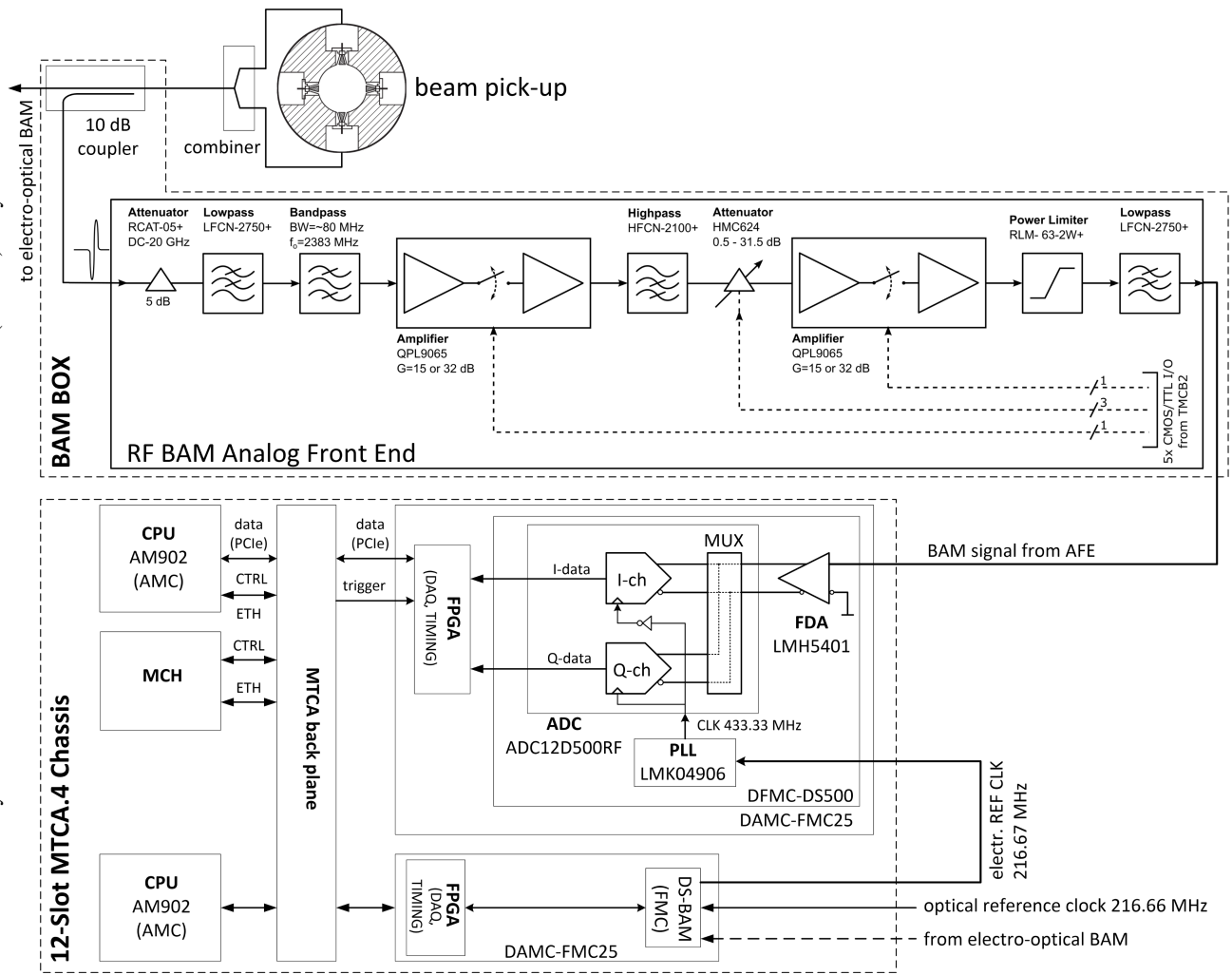

Figure 4: Overview of the coarse RF BAM channel.

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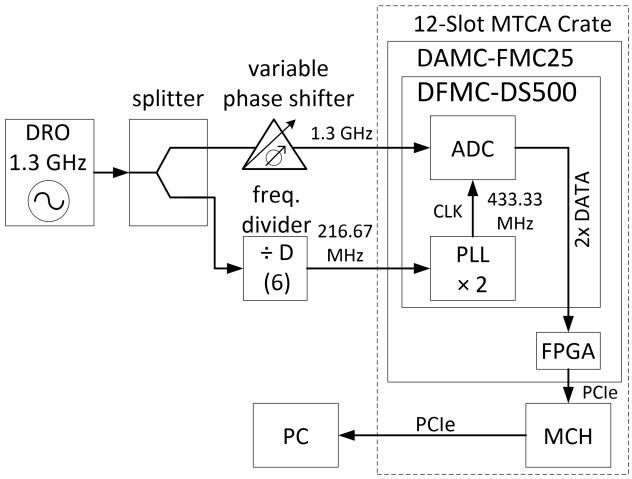

Figure 6: Measurement setup for estimating jitter.

Therefore measurements with 1.3 GHz sine wave were made to evaluate the systems performance under ideal conditions. Figure 6 shows the measurement setup. A *dielectric resonator oscillator* (DRO) was used to produce a clean, stable and accurate sine wave with a frequency of 1.3 GHz. After splitting the signal, one part is fed into a by six clock divider to produce a 216.66 MHz reference clock. The reference clock is doubled by the on board PLL, to provide 433.33 MHz ADC clock. The 1.3 GHz carrier is periodically sampled at the same point and a DC signal is produced. Using the variable phase shifter in between the splitter and ADC allows to shift the amplitude of the sampled DC signal. With this setup the overall jitter of the PLL and the ADC is converted into amplitude noise.

To roughly estimate the timing error of the system the sampled DC was adjusted to zero by shifting the phase of the input signal and 101 batches of 16352 samples were recorded. Figure 7 depicts the PDF of the timing error measured with the DFMC-DS500.

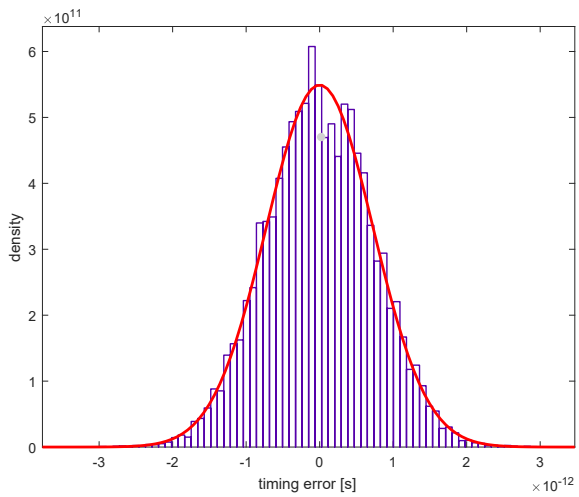

Figure 7: PDF of timing errors.

CONCLUSION AND OUTLOOK

The measurement data in Figure 7 looks promising concerning coarse RF BAM accuracy. The timing error is 7 ps (peak-to-peak) and 726 fs (RMS). It can be further reduced by averaging the sample values during operation in the accelerator. In the next step, the operation in FLASH will show whether the accuracy can actually be achieved.

The digitizer board, especially the PLL, is not running at the full performance concerning clock jitter and further improvements of the DFMC-DS500 will increase the over all accuracy of the coarse RF BAM system.

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