COMMISSIONING OF THE OPEN SOURCE SIRIUS BPM ELECTRONICS

D. O. Tavares*, G. B. M. Bruno, S. R. Marques, L. M. Russo, H. A. Silva, LNLS, Campinas, Brazil

Abstract

Sirius is a 3 GeV 4th generation circular light source designed to achieve an emittance of 0.25 nm·rad [1]. During the early stages of the machine design, the BPM electronics was selected as one of the projects to be developed by the LNLS team. This paper will report on the manufacturing and deployment processes of the referred electronics as well as the achieved reliability and performance.

INTRODUCTION

All units of the Sirius BPM Electronics have been manufactured and are currently being prepared for deployment in the machine. In total, 21 BPM racks will be deployed along the accelerator, of which 20 racks are dedicated to booster's and storage ring's electron BPMs, white photon beam BPMs and fast orbit feedback, and 1 rack is dedicated to transfer lines BPMs. A 22nd BPM rack will be kept in the Beam Diagnostics laboratory as a homologation rack for repairs and new developments . Not included in this list are the Linac BPM electronics, which were supplied by SINAP as part of a turnkey Linac contract. They will not be covered in this paper.

SIRIUS BPM ELECTRONICS

As shown in Fig. 1 the assembly of a BPM rack is composed of the following parts: (i) one 12-slot MicroTCA.4 crate; (ii) several RF Front-End (RFFE) modules, one per BPM; (iii) one 24-port Ethernet switch; (iv) one isolated AC/DC linear power supply serving the RFFE modules; (v) RF coaxial cables between RFFE modules and digitizer boards; (vi) Ethernet cables for RFFEs and crate.

The MicroTCA.4 crate is populated with modular FPGA carrier boards following PICMG AMC [2] and VITA FMC [3] standards, each of them playing the role of either a timing receiver, a 4-channel RF signals digitizer or a 4-channel digital picoammeter, depending on the I/O mezzanine modules attached to it. In the future, an additional crate slot will be used as fast orbit feedback (FOFB) processor and fast orbit correctors' power supply, for which multi-gigabit optical I/O mezzanines and an open hardware 10 kHz bandwidth linear power supply rear-transition module (RTM) will be employed.

The RFFE is an Ethernet-controlled analog front-end module providing the following core functions to the BPM system: (i) low-pass filtering of high accelerator RF frequency harmonics; (ii) 2x2 switching of diagonally opposed BPM antenna signals, with optional RF switches temperature stabilization; (iii) narrow band-pass filtering to avoid aliasing of revolution harmonics to the baseband; (iv) RF signals amplification with digitally controlled gain.
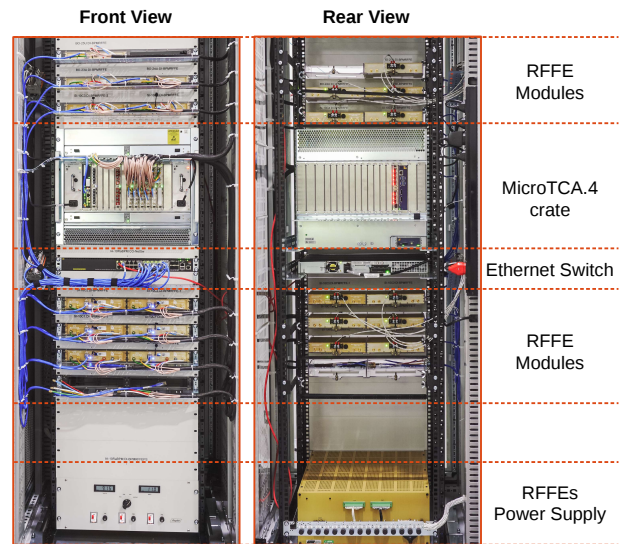
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* daniel.tavares@lnls.br

Figure 1: BPM rack layout.

Following ESRF's and Soleil's approach [4], the signals from the BPM pick-ups will be brought to the electronics by delay-matched cable assembly with (160 ps peak-to-peak error), composed of four LMR195 coaxial cables extruded within a common encapsulation, aiming at minimizing the position drifts caused by unequal thermal variations of cables' characteristics. This is a critical part of the system, since such drifts could not be calibrated by the RFFEs switching scheme. Cables lengths vary from 25 m to 70 m.

Another bundle of cables connect the 4 RFFE RF outputs and switching clock signal input to the digitizer's 4 ADC RF inputs and trigger output of one BPM, respectively. The 4 RF cables are also delay-matched with peak-to-peak error below 20 ps. They are double-shielded 2 m long RG316 coaxial cables providing more than 100 dB isolation.

The digitizer sampling clock is generated in each FMC ADC module and is synchronized with the accelerator's master oscillator by means of a timing receiver in the crate [5]. A reference clock is delivered by the timing receiver and sent to all BPM digitizers through one of the MicroTCA.4 backplane's low jitter clock line.

Each RFFE is controlled via Ethernet (TCP/IP) by the crate CPU. They are physically connected to the rack's Ethernet switch but logically isolated from the accelerator's control network by means of Virtual LANs. Only the crate CPU has access to the RFFE IP addresses of the corresponding rack. The AMC FPGA boards are in turn accessed via PCI Express. The BPM EPICS IOC of each BPM run in the crate CPU and publish the BPM PVs to the control network.

The BPM project followed an open source design philosophy aiming at facilitating collaboration with other institutes [6]. The RFFEs, RF digitizers, FPGA carrier and

timing modules are all open hardware projects licensed under CERN Open Hardware License [7]. Software and gateware designs are published at GitHub under open source licenses [8].

MANUFACTURING

The next sections describe the processes of manufacturing, testing and integrating the Sirius BPM electronics. It also summarizes the failures and difficulties found along the way.

Procurement

Two strategies were evaluated for manufacturing ready-to-commissioning boards: (i) assembling the boards through contract manufacturers (CM) and doing all testing, system setup and installation at LNLS; (ii) contracting a turnkey provider who could arrange board manufacturing, board testing and occasional repairs.

From 2016 through 2017, several companies were evaluated, local and foreign ones, for both strategies. On the turnkey side, two Brazilian companies developed test benches for the boards as part of the *Desafio Sirius* (Sirius Challenge) project, a government subvention program that financed third-party technology development in several areas of the Sirius project. Electronics suppliers which traditionally serve the accelerators community were also contacted.

A decision for a mixed approach, where LNLS contracted the board manufacturing directly from a CM while also contracting a third-party for tests, integration and system assembly was made in 2017. An important reason for this decision was the late development of some boards, for instance the 4-channel 250 MS/s ADC FMC module (FMC ADC), which had improvements being made to the project until 2017. These late developments, while not a departure from the overall architecture of any boards, meant less time for a full project transfer that would be necessary for a turnkey arrangement.

Both parts of the RF BPMs digitizer, the AMC FMC Carrier (AFC) FPGA board and the FMC ADC modules, and the SFP rear transition module (RTM-SFP) used in the timing receiver, were manufactured by the Polish CM Creotech [9], who was selected due to prior experience as developer and manufacturer of these boards. The RFFE boards were in turn manufactured by the Brazilian CM CADService [10], who supplied most of the electronic components, hired the PCB manufacturer, assembled the boards and performed standard electrical testpoint checks and visual inspection.

System Integration

All of the manufactured BPM electronics boards were individually tested by ATMOS Sistemas [11], one of the successful companies in *Desafio Sirius*. They developed test benches for automated testing and report generation (Fig. 2), and also worked as a system integrator, by assembling the electronics boards, cables and mechanical parts into the BPM racks. In summary, the contract which was established between LNLS and ATMOS had as deliverable a set of 22 fully functional BPM racks accompanied with detailed reports of each board.

Most digital signals and components, including high-speed transceivers, were tested in a pass/fail basis by the integrator. To allow for future analysis, low-frequency analog signals, clock waveforms, raw ADC data captures and RF signals test results had their measurements stored and attached to the test reports. Besides standard acceptance procedure, these reports were also meant to facilitate detailed life cycle and maintenance analysis.

After individual boards testing, the system proceeded to integration: the FMC modules were mounted to their corresponding AFCs and installed in the MicroTCA crates. A set of automated scripts programmed the FPGAs gateware, loaded the crates' CPU operating system and application software images and configured the MicroTCA crate controllers (MicroTCA Carrier Hub - MCH) with application-specific settings. The crates were then run in the bench without RF signals for evaluating basic functions such as communication between CPU, MCH and all installed boards. These tests allowed to detect any problems in the digital part of the assembled crate: CPU and MCH setup, EPICS and other software installations, PCIe links between AMCs and CPU, timing system clock acquisition, locking and distribution, and proper control of FMC modules. After this test, the populated crates were mounted in the already-built BPM rack and all internal cables were connected.

Once the BPM racks were fully assembled they underwent a burn-in procedure intended to stress the system enough to catch *infant mortality* failures and possible occurrences of performance degradation. The burn-in procedure was specified at 100 hours. If any failures were detected, the corresponding BPM electronics were replaced by another unit which had previously been "burned" and the defective parts sent for diagnostics and repair.

After the burn-in procedure, a final inspection was performed at the integrator site and the racks were packaged for delivery. After arriving and being unpacked at the LNLS site, the racks underwent the final performance tests before being sent to the deployment at Sirius's instrumentation rooms.

Failures

The extensive automated tests enabled the detection of manufacturing issues in an early production stage, especially in the RFFE modules, which were not passed though functional tests at the manufacturer. Table 1 presents a summary of the manufacturing failures segmented by boards/modules models.

The RFFE internal analog boards had the majority of the defects found during these tests, with about 20 RF channels not passing the test, from a total of 1040 channels. In contrast, the RFFE power supply and controller baseboard, which are much less sensitive than the analog boards, had a lower fail rate. The main source of failure was the presence of solder flux residues on the Ethernet jack preventing the boards from establishing Ethernet communication. These
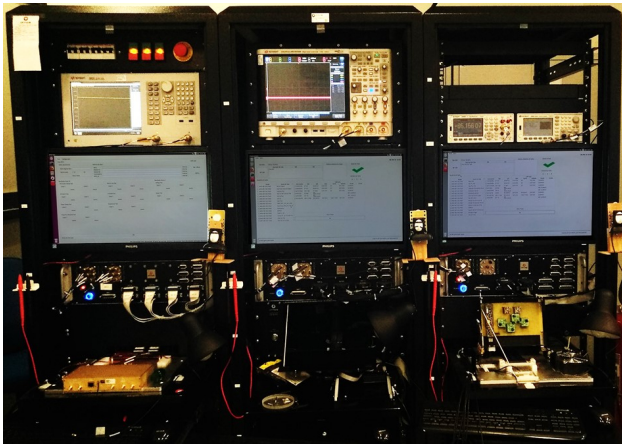
Figure 2: Manufacturing test benches at ATMOS Sistemas. Each cabinet is dedicated for individual tests of one board model, either AFC, FMC ADC or RFFE.

boards were sent back to the CM for rework and then resent to the system integrator.

Most problems found in the AFC board were related to the button switch and LEDs in the power panel, and may have been caused during FMC mounting or other board manipulation. Improvements to board design were suggested to avoid this issue in future versions. The new tests also revealed a previously unknown problem with the clock signal path coming from the AFC to the FMCs, which are harmless to the BPM electronics but could affect other applications. Moreover, one specific transceiver of four boards, which had previously passed Creotech's tests did not pass the new tests at ATMOS. Their causes are still unclear and are still under investigation.

The FMC ADC tests showed an unexpected issue in the clock circuitry, in which a small percentage of the boards (about 7%) showed an unexpected noise in the clock output when the oscillator is turned off. These boards do not exhibit any abnormal behaviour during operation, and were not removed from the production pool. The most prominent functional issues were related to the trigger output/input circuit, accounting for 1.5% of the total number of boards tested.

A recurring failure of SMA cables' connectors occurred in 12 units from a total of 236 cable assemblies. In these cases, the male SMA connector nut lost the grip after a small torque was applied. This does not always happen in the first connection, and often are detected during the burn-in procedure or after delivery, requiring the replacement of the whole cable assembly. An investigation together with the cable supplier showed that the C-spring holding the SMA coupling nut to the connector body did not have enough elasticity, applying less force than necessary to hold the nut at the specified torque. New connector assembly and cable test procedures were developed with the cable supplier to avoid further issues.

Commercial off-the-shelf equipment was not immune from failures. All MicroTCA CPUs (NAT NAT-MCH-RTM-

ComEx model) had an incorrectly soldered resistor, resulting in the operating system not being able to access or identify part of the installed SDRAM memory. The repair consisted in desoldering that resistor from all the CPU modules. The rework was performed by the integrator under the manufacturer guidance and presented no further issues. Besides that failure, two MicroTCA fan trays failed out-of-the-box and will be returned to the manufacturer.

Table 1: Failure Rate for Different BPM Equipment

Equipment	Total	Rejected	Failure %
RFFE (RF boards)	520	20	3.8%
RFFE (Control board)	260	1	0.4%
AFC	175	7	4.0%
FMC ADC	257	11	4.3%
Intra-rack Cables	1180	14	1.2%

ISSUES FOUND

The next sections describe all important issues affecting performance, reliability and maintainability found between the last prototype phase and deployment.

RFFE Microcontroller Ethernet PHY

When preparing for final production, a few spur sidelines with slowly varying frequency were spotted on the RF signals' spectra of the pilot batch RFFEs. It had the same frequency for all 4 channels but different frequencies among other RFFE units. Those spurs unequivocally explained occasional position measurement drifts of a few hundreds nanometers, since the spurs' frequency could get arbitrarily close to the RF carrier frequency and even pass through it as it wandered.

By investigating the issue it could be nailed down to the clock recovery circuitry inside the RFFE microcontroller board's Ethernet PHY, which generated sharp edges in the 125 MHz clock, thus producing harmonics close the BPM frequency, roughly 500 MHz. The hardware in use was a general purpose commercial microcontroller, mbed [12], which did not have precautions to avoid interferences in its carrier board. The spurs was generated at two frequencies, one related to the locally-generated TX clock, and one related the RX board, and dependent on the frequency of the Ethernet switch clock.

In order to isolate and filter out those spurious lines, a new microcontroller module was designed to serve as replacement to mbed, namely the RFFE-uC [13]. Among the measures which were taken to circumvent the issues were a better decoupling of PHY and microcontroller power supplies, EMI shielding around the PHY circuit to avoid any possible radiated noise, trace relayout to reduce coupling between PHY signals and other circuits, and a better common-mode choking of the Ethernet traces. The noise from the RX clock was below the RFFE noise floor after the PHY IC was properly decoupled. The noise from the TX

clock was more resilient, and even though it was reduced by more than 30 dB with the aforementioned measures, only by adding a spread-spectrum clock generator the interference could be reduced to below the RFFE noise floor.

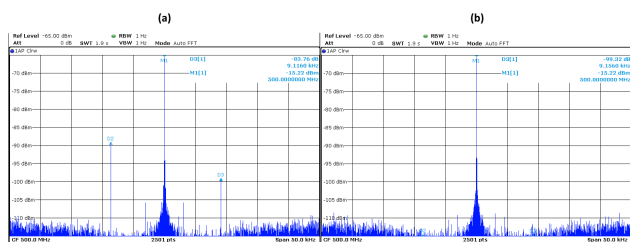Figure 3 shows the RFFE channel spectra comparison between mbed and the RFFE-uC.

Figure 3: Comparison of RFFE output spectra when employing the mbed microcontroller board an the RFFE-uC board designed at LNLS. (a) mbed; (b) RFFE-uC.

RFFE Attenuator

During burn-in tests several RF channels showed abrupt gain variations in the order of 0.05%, in intervals of hundreds of milliseconds or a few seconds. By taking a closer look to the problem it was found that those gain changes occurred in the Mini-Circuits DAT-31R5A-SP+ digital step attenuator. Since this behavior was not detected in prototyping phases, one of the raised hypothesis to explain such failure was that the attenuator IC batch was defective and needed replacement. However, by contacting the manufacturer it was found the DAT-31R5A-SP+ needed to be supplied with −3.6 V in one of its pins to operate in a spurious-free mode. By testing a supposedly defective DAT-31R5A-SP+ unit with −3.6 V supply on a Mini-circuits attenuator evaluation kit, it was verified that the unexpected gain variations completely vanished.

The DAT-31R5A-SP+ part number soldered to the final production boards was in fact a replacement of the DAT-31R5-SP+ part number, an older IC which became obsolete in the course of the project. By digging into the problem it was found the DAT-31R5-SP+'s datasheet required grounding one of the pins for which the DAT-31R5A-SP+'s required supplying with −3.6 V to operate in spurious-free mode, although this change in interface was not reported in the DAT-31R5-SP+'s replacement guide nor was mentioned in the datasheet. Although the investigation of the root causes by the manufacturer started very satisfactorily, with responsive replies and exchange of information, the final solution has not been reached since the manufacturer suddenly stopped replying to any of LNLS's contacts.

Fortunately a footprint-compatible replacement provided by another manufacturer was found, namely the IDT F1953. It can operate spurious-free without the need of a negative supply. Figure 4 shows the comparison of Mini-Circuits and IDT chips.

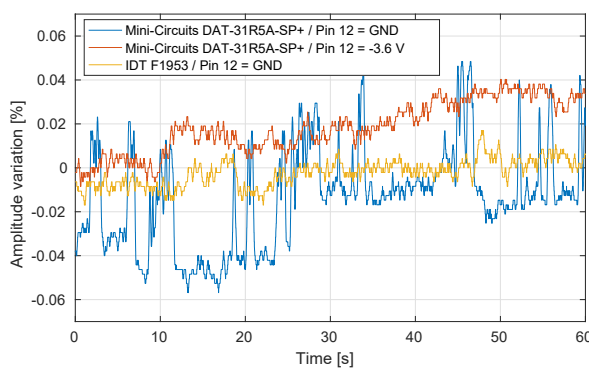Although the replacement of the Mini-circuits DAT-31R5A-SP+ by the IDT F1953 seems to solve the reported

Figure 4: Attenuator gain behavior measured with R&S FSV spectrum analyzer at zero span and 5 Hz bandwidth. Mini-Circuits B14-TB-342 and IDT F1953EVBI evaluation kits were used.

issue, its actual suitability to the design still needs to be demonstrated with a fully assembled RFFE and long term tests. At present, LNLS has not yet made a decision on whether or not to proceed with a gradual rework of all the manufactured RFFEs for making this replacement.

Interference of Reference Clock into the RF Path

Along the project's prototyping phases, the chosen frequency of the reference clock sent through the crate backplane was $f_{RF}/8 = 62.5$ MHz. However, during the validation tests it was noticed the 8th harmonic of such reference clock interfered with the RF signals being digitized by the ADCs, causing a dependence of the position measurements with signal's phase. This is explained by the fact that the sum of two sinusoidal waves, one with fixed amplitude and phase (the reference clock interference) and the other with varying relative phase (the RF signal), translates into a varying amplitude of the resultant signal and ultimately in the position measurements.

The solution was to choose a different reference clock for which no harmonics would interfere with the RF signal. The chosen reference was $f_{RF} \cdot 5/36 = 69.44$ MHz, which is a revolution frequency harmonics of both booster ($h = 828$) and storage ring ($h = 864$) machines and is close to the previously validated reference frequency, 62.5 MHz. Figure 4 shows a comparison of position measurement sensitivity to phase variation, where a phase modulation of 2π rad peak-to-peak of 0.2 Hz was applied to the RF generator and the power level was adjusted to provide −4 dBm at the ADC board inputs. Although the improvement is relatively small, in the order of 60 nm, it has roughly the same order of magnitude of the targeted long-term stability, 100 nm.

System Reliability

Besides the extensive tests performed along the manufacturing process, system integration and burn-in phases, the performance tests carried out by the LNLS team proved to be an essential step for final validation. With the increase of units to be tested and within a more realistic installation
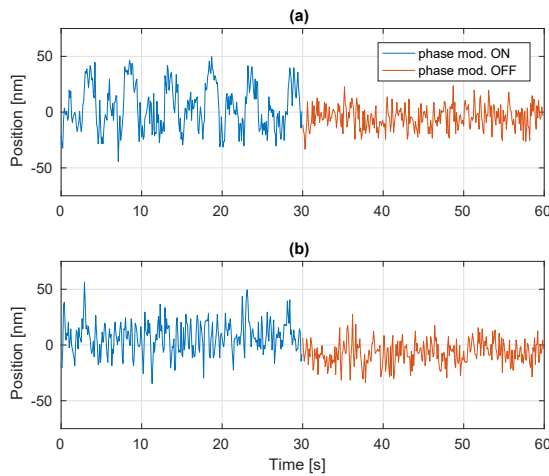
Figure 5: Position measurement variation caused by 5 Hz phase modulation in RF signal caused by reference clock interference: (a) $f_{refclk} = f_{RF}/8$; (b) $f_{refclk} = f_{RF} \cdot 5/36$.

scenario, issues which were not detected during prototyping phase started to emerge.

Occasional and unexpected failures such as FPGA boards' erratic resets and bad recovery from power outage helped the LNLS team to tune specific parts of the system. Other issues such as the replanning of VLAN and network routes inside the crate CPU and discovery of identification accessories affecting the tightening of SMA connectors along the RF signal path helped anticipating problems prior to the accelerators' commissioning.

At the time of writing, the true concern in terms of system reliability comes from the sporadic and unrecoverable loss of communication with RFFE modules, for which no cause has been identified yet. The first effort to overcome this issue was the implementation of a watchdog mechanism in the RFFE microcontroller to allow resetting the RFFE firmware when it is not able to receive heartbeat requests from its sole client, i.e., the MicroTCA crate CPU. This operation will happen transparently to the RF channels operation, since absolutely no effects will be caused in the digital attenuator settings, RF switching or power supplies of the RF channels.

FPGA Gateware Update

One of the strengths of MicroTCA.4 is its hardware management capabilities. For instance it gives remote access to the JTAG bus of each AMC card in a crate for debugging, FPGA gateware programming, etc. However, besides the advertised MicroTCA capabilities, the available solution for remotely programming the FPGAs' FLASH memory via JTAG yields 40 min update time per FPGA board in the chosen MicroTCA crate model. Since this process must be done sequentially, it results in a total of 7 h and 20 min when updating a fully populated BPM crate (11 AMC boards). This unexpectedly high programming time is explained by two factors: (i) low JTAG maximum frequency, currently at

4.1 MHz; (ii) a constant exchange of messages between the Xilinx Virtual Cable (XVC) server and its clients.

The MCH vendor, N.A.T., is developing two features to overcome the aforementioned issues: a clocked JTAG Switch Module (JSM) gateware which will increase the JTAG frequency up to 20 MHz and a scriptable way of uploading SVF files to the MCH. With this two new features in place the total update time of a full crate should decrease to roughly 1 h.

Further improvement is still possible if the update is managed by the application gateware itself, and the new firmware bitstream is sent to the FPGAs via PCIe. With this mechanism implemented, the full set of 22 racks with fully populated crates could be updated at less than 5 min. There would still be the risk of corruption if the update is interrupted. In this case the previous method using the JSM could be used as fallback solution. This mechanism will be implemented by LNLS in future gateware/software releases.

ACHIEVED PERFORMANCE

As the BPM racks were being delivered by the integrator, the LNLS team started executing the last performance tests prior to installation. A 25 m² area in the LNLS's Metrology building was made available for receiving up to 9 BPMs racks simultaneously. The building's temperature is controlled within 1 °C peak-to-peak, thus close to the planned temperature stability inside Sirius's instrumentation rooms, 20 ±0.25 °C. The setup is capable of testing 1 complete BPM rack per day. It takes 3 h for measuring beam current dependence (BCD) and resolution, 8 h for long term drift data taken, 1 hour of cables disassembling and assembling and half an hour for final checks and preparation for running the automated scripts. At the time of writing, 90 BPM electronics (8 BPM racks) have been tested, out of a total of 250 units.

All tests presented in the next sections were performed using a R&S SMA100A signal generator as RF source and timing master clock reference. The RF frequency was set to 500 MHz and the timing reference clock, provided by R&S SMA100A's auxiliary clock output, was set to 625 MHz in order to avoid artificial interferences with the RF signal. A SINAP Event Generator (EVG) was used as timing master and provided a fiber connection to the Event Receiver placed inside the BPM's MicroTCA crate. The RF signal was split by 16 (Mini-Circuits ZB16PD-72+) and further by 4 (Mini-Circuits ZFSC-4-1+) right before entering each of the BPM electronics inputs. 1 dB and 2 dB attenuators (Mini-Circuits VAT-1+ and VAT-2+) were connected to 6 units of the 1:4 splitters in order to simulate 0.5 mm off-centered beams in both planes. All unused splitter outputs were matched with 50 Ω loads.

Since the Sirius BPM Electronics employs a 2x2 RF channels switching scheme, a modified version of the *difference-over-sum* method was employed, as shown in Eqs. (1, 2). It allows better suppression of common gain drifts in the

pair of channels being swapped without meaningful loss of accuracy when compared to the standard method.

$$x = \frac{K_x}{2}\left(\frac{TO - BI}{TO + BI} - \frac{TI - BO}{TI + BO}\right) \qquad (1)$$

$$y = \frac{K_y}{2}\left(\frac{TO - BI}{TO + BI} + \frac{TI - BO}{TI + BO}\right) \qquad (2)$$

where TO, BO, TI and BI denote the amplitudes of top-outside, bottom-outside, top-inside and bottom-inside antennas in a 45°-rotated BPM. K_x and K_y are standard *difference-over-sum* BPM geometric factors, which were set to 10 mm during the performance tests for easy comparison with other reported data. Sirius's storage ring and booster button BPM geometric factors are $K_x = K_y = 12\,\text{mm}/\sqrt{2} = 8.49\,\text{mm}$ and $K_x = K_y = 18.1\,\text{mm}/\sqrt{2} = 12.76\,\text{mm}$, respectively.

When varying the generator power level for testing beam current dependence (BCD) and RMS resolution, the RFFE attenuators were set accordingly to provide −5.6 dBm signal power level in the RFFE outputs, which corresponds to roughly 8% of ADCs' full-scale.

Resolution and Beam Current Dependence

Figure 6 shows the average resolution and beam current dependence for all tested electronics at different input power levels. The horizontal axis also displays the expected signal level which will be delivered by Sirius's storage ring BPM pickups after cables. The resolution is given in two different bandwidths, from 0.1 Hz to 1 Hz and from 1 Hz to 1 kHz.
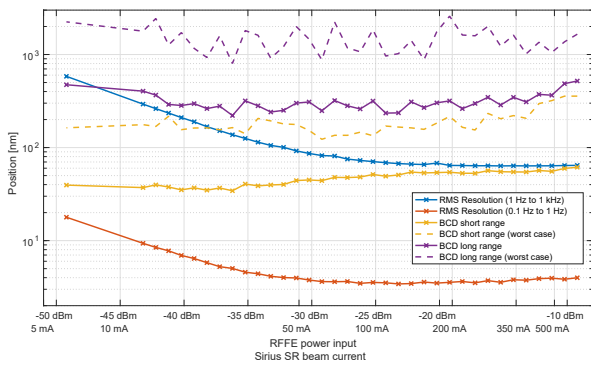

Figure 6: BCD and resolution performance.

The most stringent Sirius one sigma resolution specification is 80 nm in a 0.1 Hz to 1 kHz frequency band. These numbers are set to allow reaching position stability of 5% beam size at 1 kHz bandwidth when operating with FOFB on. Taking into account the BPM geometric factor re-scaling for storage ring button BPMs, the results show that the specified resolution can be met for beam currents from 500 mA down to 50 mA at Sirius storage ring.

BCD specifications were defined for two scenarios: (i) long range, where amplitudes are varied 30% peak-to-peak and simulates electron beam in decay mode; (ii) short range, where amplitudes are varied 2% peak-to-peak simulating

top-up operation. The targeted BCD performances are 1 μm in long range and 100 nm in short range. The results show these performances can be met on average but are exceeded in a few BPM units.

Long-term Drift

The Sirius BPM Electronics must reach a peak-to-peak drift performance of less than 100 nm in an 1 hour span and 5 μm in an one week span. Figure 7 shows the 8-hour drift performance for all tested electronics, plotted as the histogram of the peak-to-peak value of position waveforms collected at 10 Hz and decimated to a 1 min sampling period. A threshold of 200 nm was set to segment the data set in BPMs with acceptable and unacceptable performances.

During the tests, a −20 dBm signal level was used at the RFFE input, roughly equivalent to a 200 mA beam current in Sirius storage ring.
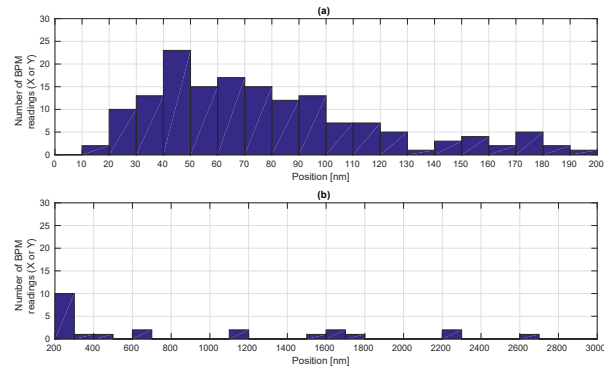

Figure 7: Peak-to-peak 8-hour drift performance histograms. (a) Position readings below 200 nm; (b) Position readings between 200 nm and 3 μm.

The causes of the drifts above 200 nm had not yet been completely identified at the time of writing. In two BPMs (i.e. four X and Y position readings) the out-of-specification performance has been traced down to deffective RFFE RF channels. For other BPMs, it has been noticed the performance is improved in the long run when the BPMs of a rack are left drifting for many days (3 or more), then slowly approaching the drift specification. It suggests the accomodation of the test setup's cables may explain some of the unwanted behavior. The issue will be further investigated.

Figure 8 shows the 8-hour drift waveforms for 20 selected BPMs where drift performance stayed below 200 nm. The traces were ordered from the highest to lowest performance BPMs.

FUTURE PLANS

All tests herein presented were performed with CW signals. The manufactured BPM electronics should start receiving real beam signals before the end of 2018, when booster commissioning is planned to occur. Several aspects which were not covered by the described tests will have to be validated, for instance the quality of BPM cables assembly,
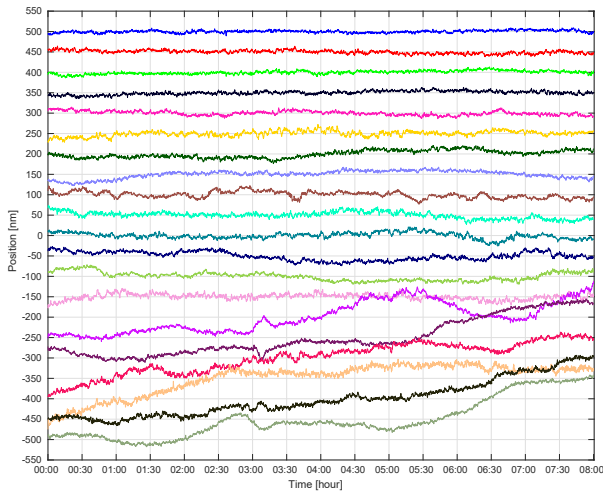
Figure 8: 8-hour drift of selected BPM readings, in ascending order of performance.

shielding and grounding, the effect of tunnel thermal stability on the long term position measurements, overall control and data acquisition software reliability and user experience.

The Sirius BPM Electronics project is rather a live project at this point in time. Bug reports and feature enhancements are posted on GitHub repositories' issue tracker and are tackled according to the priority and resources.

A few hardware projects should come on line in the first half of 2019: (i) an EPICS-controlled rack manager which will be able to provide rack's temperature monitoring and power distribution units control; (ii) fast orbit corrector Power Supply in MicroTCA RTM module [14], which will be attached to an AFC FPGA board used as FOFB controller and provide small signal analog bandwidth of 10 kHz on magnets with up to 3.5 mH inductance and 1 A maximum current.

CONCLUSION

The Sirius BPM Electronics project is in its final stage of deployment. The reported production failure rates and achieved performance so far points to a smooth commissioning with real beam signals. Many critical issues were found along the way and solved, whereas the digital step attenuator spurious gain behavior still remains open for the already manufactured boards. Nonetheless, it seems it has not spoiled short- and long-term performances in a significant way. The issue may be very likely solved by replacing the attenuator part number on new production batches.

By adopting the strategy of developing the electronics in house, LNLS had also experienced the role of developing manufacturing processes and establishing partnerships with local and foreign companies for the task. That was a long and laborious process until reaching the required final quality. In total, 6 years have elapsed since the first conceptual ideas and the final production.

Differently from other approaches, the Sirius BPM Electronics architecture was thought as a modular system. Many parts of the system are reused in several subsystems, for instance the same FPGA AMC (AFC) design is currently shared among RF and X-Ray BPM electronics, timing system and FOFB, with the same MicroTCA crate hosting all these systems. The AFC and FMC ADC comply with the AMC and FMC industry standards and can be used in other contexts, or even be leveraged by commercially available modules, such as the CAENels FMC-Pico-1M4 picoammeter [15] used for X-Ray BPMs or Faster Technology FM-S14 FMC SFP module [16] to be used in the FOFB solution. Moreover, the RFFE module is a standalone electronics, Ethernet-controlled, which can be used in conjunction with non-MicroTCA digitizers.

The same modularity concept is present in the gateware and software solutions, where well established infrastructure was adopted as the basis for the application-specific code, for instance the Wishbone bus for interconnecting HDL cores inside the FPGA and the ZeroMQ messaging library [17].

By releasing modular, standard-compliant and open source hardware, gateware and software designs, the barriers for reusing the Sirius BPM Electronics – as a whole or by picking some of its specific modules – are significantly reduced.

ACKNOWLEDGEMENTS

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