ISBN: 978-3-95450-201-1 doi:10.18429/JACoW-IBIC2018-TUPA16

SIGNAL PROCESSING FOR BEAM LOSS MONITOR SYSTEM AT JEFFERSON LAB

J. Yan, T. Allison, S. Bruhwel, W. Lu, Jefferson Lab, Newport News, VA 23606, U.S.A.

Abstract

Ion Chambers and Photomultiplier Tubes (PMT) are both used for beam loss monitoring in the Machine Protection System (MPS) at Jefferson Lab. These detectors require different signal processing, so two VME-based signal processing boards, Beam Loss Monitor (BLM) board and Ion-Chamber board, were developed. The BLM board has fast response (< 1 μs) and 5 decades of dynamic range from 10 nA to 1 mA, while the Ion-Chamber board has a slower response but 8 decades of dynamic range from 100 pA to 10 mA. Both boards feature machine protection and beam diagnostics, in addition to a fast shutdown (FSD) interface, beam sync interface, built-in-self-test, remotely controlled bias signals, and on-board memory buffer.

INTRODUCTION

The Beam Loss Monitor (BLM) system is an important part of the Jefferson Lab Machine Protection Systems (MPS) [1]. It detects bremsstrahlung radiation from low level beam loss during tune-up and beam operations and provides a machine protection trip well before the beam can damage accelerator components. Two types of radiation detectors, 931B PMT [2] and CERN Ion Chamber [3], are installed for the beam loss monitor system of the CEBAF at Jefferson Lab. An 8-channel VME based BLM board, which has replaced the original 4-channel CAMAC based board, are developed as the current acquisition electronics for PMT detectors, with negative current between -5 nA to -1 mA and a fast response time. Meanwhile, a newly designed 5-channel Ion Chamber (IC) VME board provides the current acquisition for CERN Ion Chamber, which has a slow time response and a large dynamic range.

NEW BLM BOARD DESIGN

The new 8-channel BLM signal processing board has a functional block diagram that consists of analog signal processing and digital processing. The analog processing includes linear signal tuning, operational amplifier (op-amp) integrating signal processing, Howland voltage-to-current converter circuits, and logarithmic current signal processing. The digital processing includes FSD signal logic, analog-to-digital (ADC) data acquisition, and FPGA digital control. The linear tuning is an op-amp circuit with a gain of 5490. It converts negative current from PMT to voltage, referred to as the pre-amplified voltage. The pre-amplifier voltage signal then serves as the input for both integrating and log circuits. Figure 1 shows the diagram of the analog signal processing for each channel. The integrating processing circuit is op-amp based and performs the mathematical operation of integration to cause the output voltage to respond to changes of the input voltage over time. The integrated output voltage is connected both to the ADC for data sampling and to a fast voltage comparator for FSD detection. The equation of the ideal voltage of the op-amp integrator is

$$V_{\text{int}} = -\int_0^t \frac{V_{in}}{R_{in} \cdot C} dt \,.$$

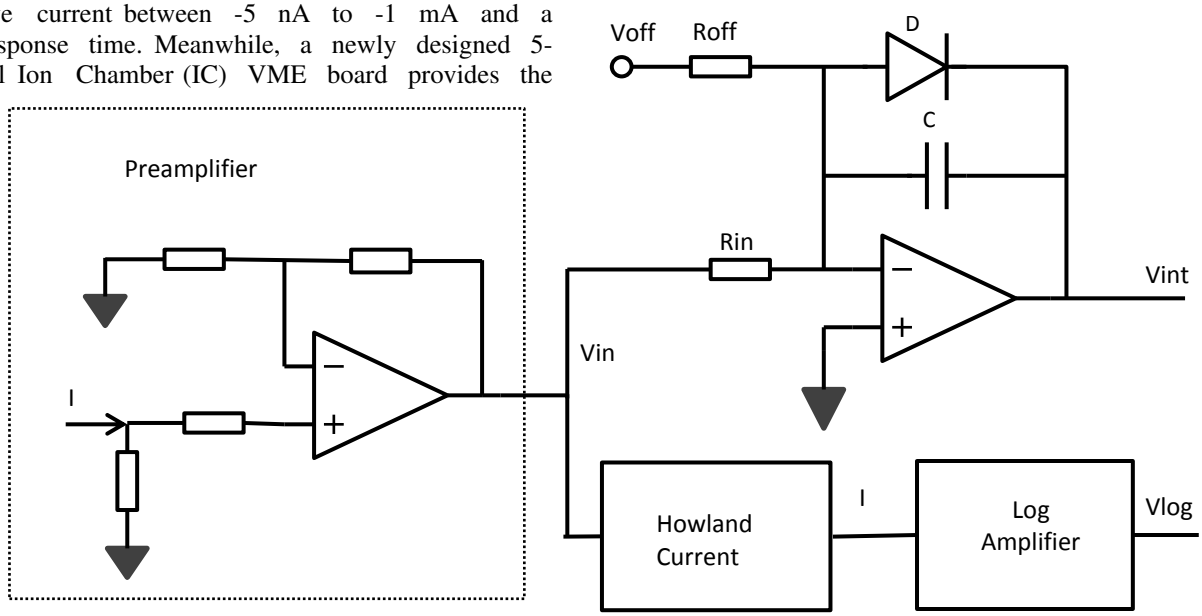

Figure 1: Diagram of the analog signal processing.

ISBN: 978-3-95450-201-1 doi:10.18429/JACoW-IBIC2018-TUPA16

The RC time constant $= R_{\text{in}} \cdot C$ is designed as 0.1 µs, and the cutoff frequency $f_c = 1/2\pi\tau$ is 1.6 MHz. A variable bias voltage V_{off} is added to the integrating circuit, which defines the threshold input voltage that initiates the integration. If $V_{\text{off}}R_{\text{off}} + V_{\text{in}}R_{\text{in}} > V_F$, the current passes through the diode and no integrating occurs; if $V_{\text{off}}R_{\text{off}} + V_{\text{in}}R_{\text{in}} < V_F$, the diode blocks the current and the circuit operates as an op-amp integrator. Here V_F is the Forward Voltage Drop of the diode D. The bias voltage V_{off} is driven by a DAC with a range of 0 to 5V. The DAC is programmed by the FPGA, so that the bias value can be controlled to avoid a ramp-up of the integrator on background noise.

The logarithmic signal processing consists of a Howland current source and a log converter circuit based on the log amplifier MAX4206. The MAX4206 is a precision trans-impedance logarithmic amplifier with 5 decades of input current across a 10 nA to 1 mA dynamic range. It computes the log ratio of the input current relative to an externally or internally generated reference current and provides a corresponding voltage output with a default 0.25V/decade scale factor. By adjusting the output scale factor and output offset voltage, the output voltage is designed to be from 0V to 5V corresponding to a 10 nA to 1 mA input current, namely 1V/decade. Since the input of the log amplifier requires a positive current source, a converter circuit has to be applied to convert the preamplifier voltage to a positive current.

The Howland current source is an op-amp circuit topology that effectively forms a linear differential voltage-to-current converter. Figure 2 shows the schematic diagram of the basic Howland Current Pump circuit, where input resistors R_1=R_3 and feedback resistors R_2=R_4. When the ratios of R_1/R_2 and R_3/R_4 are the same, the feedback from the output to both the + and - inputs of the op-amp is at equal strength [3,4]. The load current I_L, which takes the form below, mathematically analyses the circuit.

$$I_L = \frac{V_{in+} - V_{in-}}{R_1}.$$

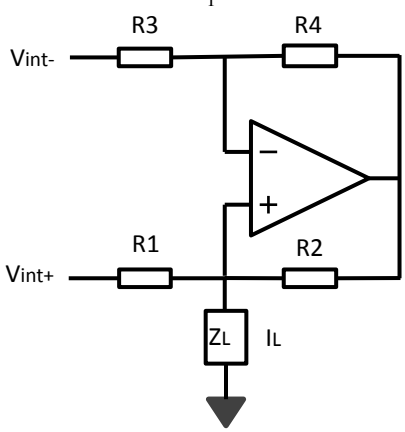

Figure 2: Schematic diagram of the Howland current source [5].

This equation shows that the output current per change of the input voltage is equal to $1/R_1$. If the input resistors and feedback resistors are matched, the output impedance of the source is high, so that the gain is identical for all output voltages and impedances, and for all inputs. However, all 4 resistors have tolerances and the resistor network will not be perfectly matched. For this application, a full precision conversion is required, so 0.1% tolerance resistors are used. The value of the resistor R_1 is selected to convert the output current precisely as the input from the PMT. The gain 5490 of the preamplifier and the gain -1/5490 of the V/I converter are chosen for the design. The current I_L is directly fed to the log amplifier and then converted to a voltage, which will be sampled by the ADC AD7656.

The AD7656 contains six 16-bit, fast, low-power, independent ADCs. Three AD7656 ADCs are applied to sample the integrated and log signals from 8-channels simultaneously. The FPGA communicates with these ADCs through a serial interface with a sample rate of 100 ksps for each independent channel. All the data are stored in a 16 Mb, 16 bit SDRAM in a ring buffer configuration and the data will provide beam loss transition play-back whenever required.

BLM TESTING AND MEASUREMENTS

The critical functions of the new BLM board are tested before the final production. They include machine protection and diagnostics, fast response for FSD, self-test, pulse measurement and continuous monitoring, and data acquisition.

A Keithley 6221 Current Source provides an input current to the BLM board and a multimeter is used to measure the integrated and log signals. The input current demonstrates 5 decades of dynamic range from -10 nA to -1 mA. Figure 3 shows how the integrated voltage (Vint) and log voltage (Vlog) change with the input current I. Here |I| is the absolute value of the input current. The log voltage has a logarithmic relation to the input current, and variation of 1V per decade of current. This curve shows that a change of current (or beam loss) is precisely monitored and it can be applied to beam loss diagnostics. The integrated voltage changes slightly, when current is low, but at a certain point (10 µA in this case) it jumps to 5.8V, which is the saturation voltage of the integrator. When the input current is less than 10 µA, the sum of the bias voltage V_{off} and the preamplified voltage V_{in} is higher than the Forward Voltage Drop V_F of the diode, and no integration occurs. When the input current exceeds 10 µA, the summation of V_{off} and V_{in} is less than V_F, so integration kicks in and the voltage reaches saturation, which will trigger the voltage comparator to generate a FSD signal. The value of the current that triggers the integrator is dependent on the bias voltage as mentioned before.

ISBN: 978-3-95450-201-1 doi:10.18429/JACoW-IBIC2018-TUPA16

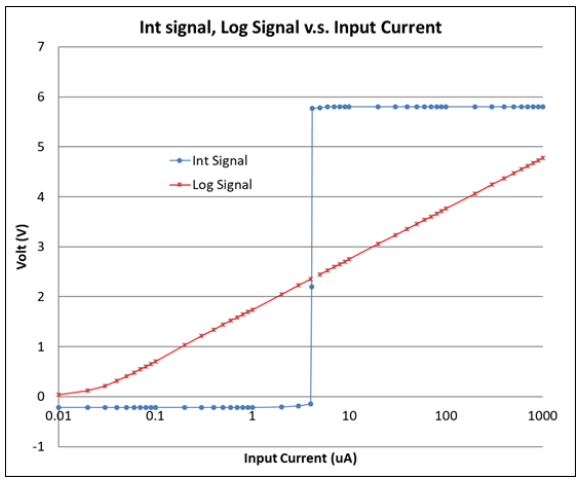

Figure 3: Integrated voltage and Log voltage dependence on the input current |I|(μA).

Each channel of the BLM board has a self-test function that feeds into a constant-on or single programmable-length current pulse, where the current can be generated by a PMT unit or an on-board signal injection. The PMT unit is connected to the BLM board via a D-9 connector and driven by a high voltage power supply. The FPGA controls the test LED inside the PMT unit. If the LED is on, the PMT will generate a negative current and output it to the analog channel of the BLM board. The test signal can be programmed as constant-on or an adjustable single pulse. The BLM board also can be tested with on-board signal injection, whereby the current is generated by a circuit on the BLM board instead of using the PMT. By using on-board testing, we measured the FSD response time of the BLM board, and studied how the integrated voltage and log voltage changed with time in pulse mode. Figure 4 shows the integrated signal, log signal, and FSD signal correspond respectively to a pulse input signal.

Figure 4: Oscilloscope measurement of pulse signal, integrated signal, log signal, and FSD signal.

In Figure 4, curve 1 (yellow) is a 1 μs pulse test signal controlled by the FPGA. Curve 2 (blue) is the log signal. Curve 3 (purple) is the integrated signal, and curve 4 (green) is the FSD signal. When the preamplifier circuit is subjected to the pulse input, the integrated signal starts to increase with time. After 360 ns, the integrated signal reaches a voltage higher than the FSD voltage comparator, and immediately triggers the FSD signal to surge. After 840 ns, the integrated signal reaches the saturation voltage. After 2.5 μs the log amplifier starts to convert the input current to a log voltage. From Figure 4 we obtain the most important timing of the BLM board, the FSD response. It is measured as 0.360 μs, less than the required 1 μs. This figure clearly shows how the integrated signal, log signal, and FSD signal correspond to a pulse input. The PMT self-test is also performed, and the measurement results are similar to those from the on-board testing.

IC BOARD DESIGN AND TEST

Compared with BLM board, the analog design of Ion Chamber board is much simpler. It doesn't require preamplifier, integrating, or Holland current circuit. The conditioned positive current from Ion Chamber inputs into a log amplifier ADL5303, which is a monolithic logarithmic detector optimized for the measurement of signal with a large dynamic range of 160 dB ranging from 100 pA to 10 mA. By adjusting the output scale factor and output offset voltage, the corresponding voltage output has 0.5V/decade scale factor. The output voltage (V_{log}) is sampled with a 16-bit ADC ADS8860 at 500K sample rate. Since the IC has slow time response, about 89 us, the signal integration for machine protection can be executed within FPGA firmware. When the V_{log} is higher than bias set (V_{Bias}), FPGA starts to integrate the number of V_{log}-V_{Bias} at 2 μs interval and obtain an integrated signal (V_{Int}). If V_{Int} exceeds the Threshold setpoint (V_{Thrd}), an integrated Ion Chamber FSD fault will be tripped. Figure 5 shows how integration and FSD trip work. The x axis is the time with unit of μs and Y axis is the signal with ADC counts. When V_{log} g is less than V_{Bias}, there is no integration and V_{Int} equals zero. After 268 μs, Vlog exceeds V_{Bias}, and V_{Int} starts integration till it is more than V_{Thrd} at time 340 μs. Figure 5 shows that the time to trip a FSD fault is about 72 μs, which meets the requirement of our Ion Chamber machine protection.

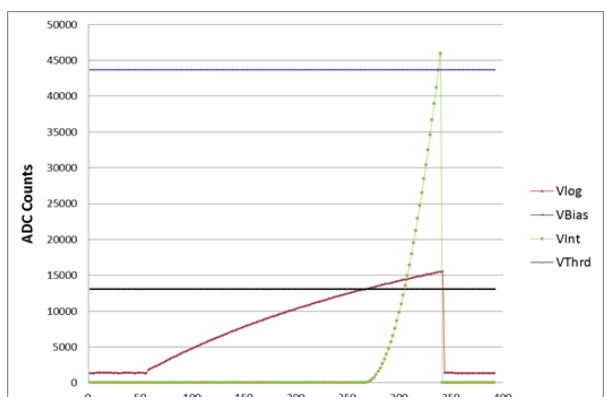

Figure 5: ADC Counts of V_{log}, and V_{Bias}, V_{Int}, and V_{Thrd} signals and FSD trip.

ISBN: 978-3-95450-201-1 doi:10.18429/JACoW-IBIC2018-TUPA16

CONCLUSIONS

The new VME based BLM and IC signal processing and data acquisition boards have been developed for the CEBAF machine protection system. The BLM board provides eight-channel analog and digital signal processing, while the IC board provides five channels, and both boards have diagnostic and machine protection functions. On the BLM board, an integrating circuit is applied to trigger the FSD fault with a response time less than 1 μs, and a Howland current source circuit is added to convert the input current for log amplifier. The integrated signal and log signal are processed simultaneously by the FPGA controlled ADCs and buffered on an on-board SDRAM memory. On the IC board, the current from Ion Chambers is directly sampled by the ADC, and all the signal integration and FSD triggering are executed within the FPGA. By monitoring the integrated and FSD signals at pulse mode, BLM board has the FSD response time of 0.36 μs, and IC board has 72 μs of FSD triggering time. Both BLM and IC boards are installed for the CEBAF operation and meet the 12GeV Upgrade requirements.

ACKNOWLEDGEMENT

Thanks to Fab Group for laying out the BCP and front panel, to Keith Cole coordinating the fabrication, and to Fab Shop for assembling the boards.

REFERENCES

[1] K. Mahoney, J. Coleman, " Overview of the Jefferson Lab Machine Protection Beam Loss Monitors", http://www.jlab.org/accel/ssg/papers_Pres/sspres/beamloss/index.html.

[2] J. Yan, K. Mahoney, "New Beam Loss Monitor for 12 GeV Upgrade", *Proceedings of ICALEPCS2009*, Kobe, Japan, page 582- 584.

[3] S. S. Gilardoni, et al., CERN-ATS-2011-131.

[4] P. Pouliquen, J. Vogelstein, R. Etienne-Cummings, "Practical Considerations for the use of a Howland Current Source for Neuro-Stimulation", *BioCAS* 2008, IEEE, page 33-36.

[5] Robert A. Pease, "A Comprehensive Study of the Howland Current Pump", *National Semiconductor Application Note 1515*, Jan. 29, 2008.