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A MicroTCA.4 TIMING RECEIVER FOR THE SIRIUS TIMING SYSTEM

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Abstract

The AMC FMC carrier (AFC) is a MicroTCA.4 AMC board which has a very flexible clock circuit that enables any clock source to be connected to any clock input, including telecom clock, FMC clocks, programmable VCXO oscillator and FPGA. This paper presents the use of the AFC board as an event receiver connected to the Sirius timing system to provide low jitter synchronized clocks and triggers for Sirius BPM electronics and other devices.

INTRODUCTION

Sirius is a 4th generation synchrotron light source based on a 5BA magnetic lattice, currently under construction in Brazil by LNLS [1]. The machine, designed to achieve a beam emittance of 0.25 nm·rad and scheduled for commissioning at the end of 2018 [2], consists of a 150 MeV Linac, a 150 MeV to 3 GeV booster and a 3 GeV storage ring with 518 meters circumference and 20 straight sections. Both booster and storage ring RF frequency is 499.658 MHz and the Linac will inject in single or multi-bunch mode at 2 Hz.

Sirius timing system [3] is a star topology optical fiber network where an event generator (EVG) broadcasts event frames to the event receivers. An event frame decoded by an event receiver can generate clock and trigger signals synchronized to the Sirius RF frequency for the beam injection process and other subsystems such as electron BPMs. The system is composed of Ethernet-configured standalone modules developed by SINAP through a collaboration with LNLS and remotely controlled by an EPICS soft IOC designed by LNLS [4].

The Sirius BPM and orbit feedback systems were developed as an open-source hardware platform [5] based on MicroTCA.4 crates, AMC and FMC modules, 1 Gigabit Ethernet and PCI Express connectivity. The digital back-end of these systems is the AMC FMC carrier (AFC) [6], a MicroTCA.4 AMC board partially based on Simple PCIe FMC carrier (SPEC) [7] design.

Thanks to the flexible clock circuits, the trigger and clock distribution options and the digital interfaces available in the AFC board, the same hardware platform was used to develop a timing receiver board to provide triggers and synchronized clocks for Sirius BPM electronics and other devices, upgrading the MicroTCA clock distribution board developed 3 years ago [3]. From now on, the timing receiver board shall be referred to as AFC timing.

HARDWARE

This section presents the AFC board focused on timing applications and the interface boards FMC 5 POF and MicroTCA RTM 8 SFP+.

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AFC

The AFC board was specified by LNLS and designed by WUT (Warsaw University of Technology) as a double-width AMC card with 2 fully populated high-pin count FMC mezzanine slots, 8 multigigabit links routed to the MicroTCA Rear Transition Module (uRTM) connector, 8 M-LVDS trigger and 2 clock lines available through the AMC backplane connector, connectivity to PCIe at Fat Pipe 1 (x4 link), redundant 1 Gb Ethernet ports, full hardware support for the White Rabbit [8] timing system and provision for standalone operation.

It has a Xilinx Artix-7 200T FFG1156 FPGA and the available clocking resources are: (*I*) a clock switch (Analog Devices ADN4604) allowing routing of MicroTCA.4 low-jitter clocks to any of the FMC slots or the AMC connector, (*II*) a 10-280 MHz I_2C programmable VCXO oscillator (Silicon Labs Si571, 571BJC000121G), (*III*) a 25 MHz VCTCXO (Mercury VM53S3-25.000) connected to a frequency synthesizer (Texas Instruments CDCM61004) configured to 125 MHz, (*IV*) a 20 MHz VCXO (IQD VCXO026156) and (*V*) 3 DACs (Analog Devices AD5662) for oscillators control.

Once inside a MicroTCA crate, an AFC timing board outputs triggers and a low-jitter synchronized clock to the other AFC boards running in the same crate through the MicroTCA crate backplane. This clock will be used as a reference clock to the BPM electronics ADCs.

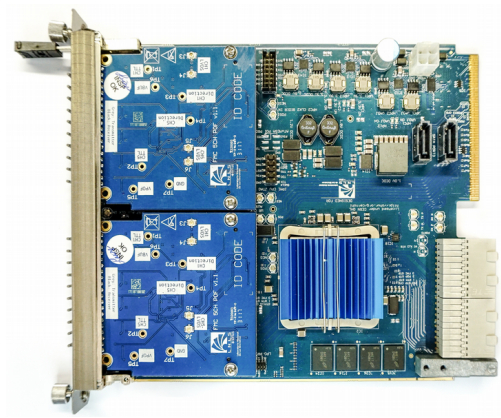

Figure 1: AFC board with two FMC 5 POF mounted.

FMC 5 POF

The FMC 5 POF board [9] has 5 plastic optical fiber (POF) transceivers mapping the same number of trigger lines from the FPGA through a FMC connector on the AFC board. As the input and output transceivers are different components with the same footprint, the board can be manufactured with up to 5 POF inputs or outputs. In Sirius timing system, it will output synchronized triggers for varied devices

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around the accelerator's facility, where most of them will be quadrupoles and sextupoles power supplies of booster and storage ring.

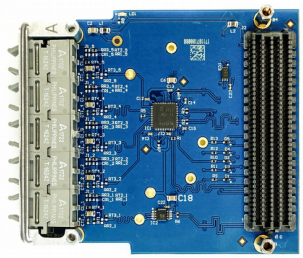

Figure 2: FMC 5 POF, a FMC board with 5 plastic optical fiber outputs.

MicroTCA RTM 8 SFP+

The MicroTCA RTM 8 SFP+ [10] is a Rear Transition Module board MicroTCA.4 standard. Its main components are 8 SFP+ connectors, which will provide optical fiber interface with the timing system, and a general purpose 10–280 MHz I_2C programmable XO oscillator (Silicon Labs Si570, 570BCC000121G) that outputs a reference clock to the FPGA GTP transceivers.

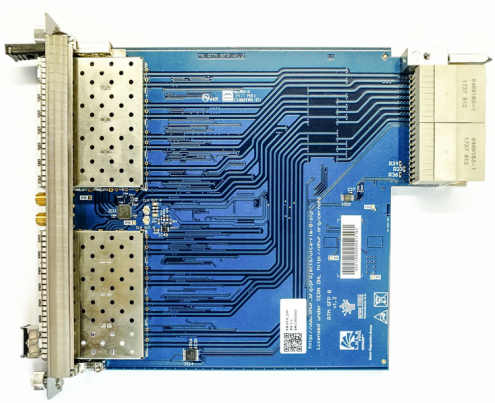

Figure 3: RTM with 8 SFP slots.

FPGA GATEWARE

The present section describes the main aspects of the FPGA gateware to implement an event receiver and a frequency and phase locked loop that outputs a low-jitter synchronized reference clock to the BPM electronics ADCs.

Event Receiver

An event frame sent from the EVG consists of an 8-bit event code and an 8-bit distributed data bus (DBUS). Each bit of the DBUS maps a synchronized clock generated by the EVG, that is continuously sending event frames at the event clock rate, which is $\frac{1}{4}RF = 124.9145$ MHz. The AFC timing can monitor one bit of the DBUS, to output a clock, or one event, to output a trigger or a pulse train.

There are 18 independently configurable monitoring channels in the AFC timing, 10 POF outputs from 2 FMC 5 POF boards and 8 AMC configurable as input or output. When outputting, each one of these 18 channels can adjust the pulse width and the delay with a resolution of one event clock period (~8 ns), as well as the pulse polarity level (low to high or high to low) and the number of pulses generated from 1 to 65535. An AMC channel operating as input can receive a general purpose trigger from another AFC board and, for example, send a corresponding event to the EVG.

Frequency and Phase Locked Loop

The AFC clocking resources were used to implement a frequency and phase locked loop (Fig. 4) to generate a low-jitter synchronized reference clock to the ADCs of the BPM electronics using the Si571 VCXO.

From the event clock recovered by the FPGA GTP transceiver, a Mixed-Mode Clock Manager (MMCM) generates the reference clock and also the DMTD clock, which is used by the frequency and phase feedback controller to measure the phase difference between the reference and the output clocks. Defining, respectively, the event, reference, DMTD and output clocks as f_{evt}, f_{ref}, f_{dmtd} and f_{out}, we have

$$f_{evt} = \frac{1}{4}RF \approx 124.915\,\text{MHz}$$

$$f_{out} = f_{ref} = \frac{5}{36}RF \approx 69.397\,\text{MHz}$$

$$f_{dmtd} = f_{ref}\frac{N}{N+1} \approx 68.918\,\text{MHz};\ N = 144$$

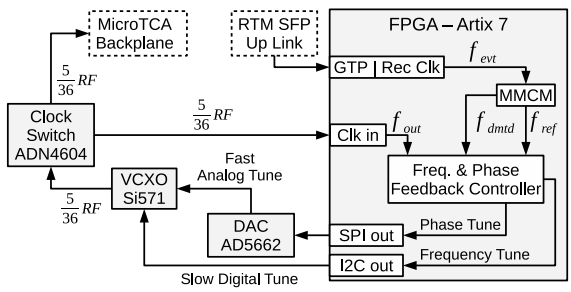

Figure 4: Synchronized reference clock block diagram.

The frequency and phase feedback controller (Fig. 5) is characterized by a frequency detector (FD) and a phase detector (PD) running in two independent feedback loops at the same time.

The FD counts the rising edges of the two input clocks during a fixed time window and calculates the difference between them to output a value proportional to $f_{ref} - f_{out}$. The length of the time window determines the sample rate, which is also the resolution of the FD, configured to be 18 Hz. A proportional and integral controller closes the loop and tunes the VCXO frequency via the I_2C, an interface that allows adjusts up to ±3500 ppm from the center frequency configuration.

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The PD is a digital version of the Dual Mixer Time Difference (DMTD) [11], shown in Figure 6, a linear method to measure the phase difference between two clock signals at same or near frequencies. It consists of two D flip-flops connected to the same clock source f_{dmtd}, which frequency is slightly lower than the one from the input clocks, undersampling f_{ref} and f_{out}. The phase difference between the clocks on the flip-flop outputs is the same as the inputs, although the output frequencies are lower and equal or near to $f_{beat} = f_{ref} - f_{dmtd}$ and hence the time interval relative to the phase difference between the output clocks is an integer number of f_{dmtd} periods. Therefore, a time counter running at f_{dmtd} was used to measure the time interval and output a value n proportional to $\phi_{ref} - \phi_{out}$, which is the phase difference between f_{ref} and f_{out} given on the interval $[0, 2\pi[$ radians. It is equivalent to measure the time interval between f_{ref} and f_{out} with a resolution of Δt_{min} given by

$$\Delta t_{min} = \frac{1}{f_{dmtd}} \frac{f_{beat}}{f_{ref}} = \frac{1}{N f_{ref}} \approx 100\,\text{ps}$$

$$f_{beat} = f_{ref} - f_{dmtd} = \frac{f_{dmtd}}{N} \approx 478.6 kHz$$

and hence, the resulting phase different is

$$\phi_{ref} - \phi_{out} = \frac{2\pi n}{N};\ n \in [0, N]$$

A moving average filter followed by a proportional controller closes the phase feedback loop driving the control voltage input of the VCXO using the DAC AD5662 controlled by an SPI interface. This configuration allows a frequency adjust range of ±192 ppm and an update rate of 478.6 kHz, as the update rate of the DAC's output is higher than the f_{beat}.

When both feedback loops are running, a large difference between f_{ref} and f_{out} turns the PD output negligible and the VCXO is driven by the frequency feedback loop, thereby moving f_{ref} toward f_{out}. Thus, the FD output decreases gradually until the frequency feedback loop becomes inactive. At the same time, the PD output becomes stable and the phase feedback loop output increases, turning the phase difference $\phi_{ref} - \phi_{out}$ constant. The frequency feedback loop maximizes the capture range, the maximum value of $| f_{ref} - f_{out} |$ for which the loop locks. The PI controller gains and the sample rate were adjusted to minimize the locking time.

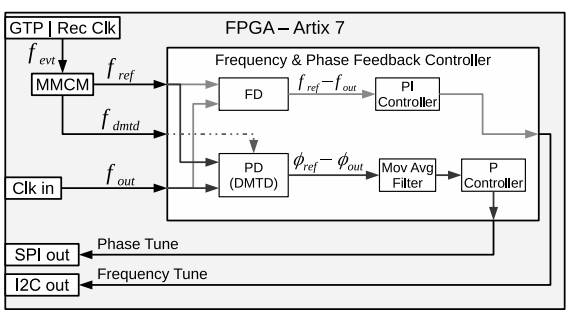

Figure 5: Frequency and phase feedback controller.

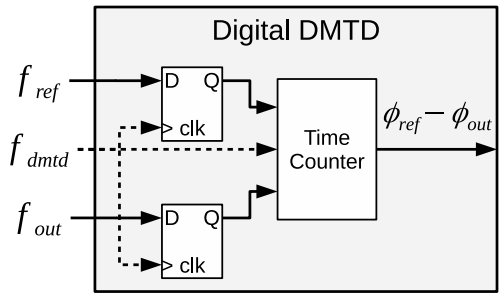

Figure 6: Digital Dual Mixer Time Difference.

PHASE NOISE PERFORMANCE

The Figure 7 shows the phase noise of the reference clock (trace 3) and the VCXO, while free-running (trace 2) and controlled (trace 1), characterized using a Rohde & Schwarz FSUP signal source analyzer, as well as the respective integrated RMS jitter (1 Hz - 5 MHz). Taking the traces 2 and 3 is possible to see that the free-running VCXO is better than the reference clock at high frequencies and the traces are crossing at about 200 Hz. The integrated RMS jitter was about 78 ps and 25 ps, respectively. Hence, the cutoff frequency of the phase feedback loop should be around 200 Hz, which was nearly achieved adjusting the moving average filter parameters and the proportional gain, as shown by the trace 1, resulting in an integrated RMS jitter of about 4 ps.

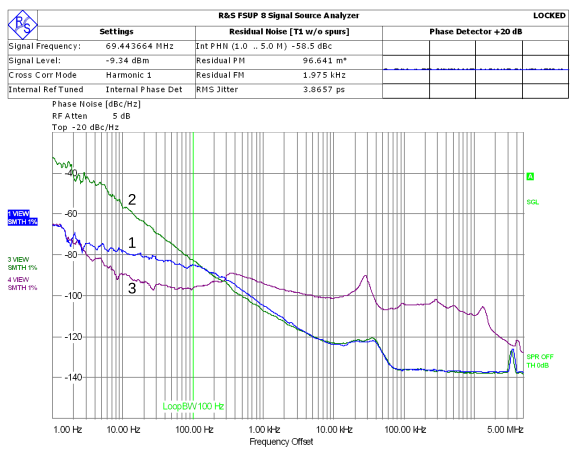

Figure 7: Phase noise characterization of VCXO controlled (1), VCXO free-running (2) and reference clock (3).

SOFTWARE INTERFACE

The AFC timing will be interfaced with the control system by means of the HALCS framework [12, 13]. It provides a modular approach for abstracting gateware modules as software services that can be exported to a control node and controlled through an RPC API (Application Programming Interface based on Remote Procedure Call). Because of that approach, all of the already supported gateware modules can be leveraged without extra effort, as the framework will automatically identify known modules and export its functionality.

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On top of that, an EPICS IOC with an asyn-based driver was developed to interface with HALCS, mapping the exported RPC API to EPICS PVs and providing access to all of the AFC timing receiver gateware functionalities.

CONCLUSION

Thanks to an open hardware project, the AFC board was developed to be the hardware platform of the Sirius BPM and orbit feedback systems. Now, it is also integrating the Sirius timing system, where more than 20 AFC timing boards will generate synchronized clocks and triggers for the BPM system and hundreds of synchronized triggers for power supplies around the accelerator.

However, the project is not concluded yet. There are some desirable features to implement as, for example, a phase compensation method to automaticlly align the output triggers, avoiding manual calibrations during the Sirius commissioning and operation.

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