ESS BILBAO INTERLOCK SYSTEM APPROACH*

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Abstract

This paper describes the approach used at ESS-Bilbao initiative for the implementation of the Interlock System. The system is divided into two parts depending on the required speed for the system response: Slow Interlocks (>100 msec.) and Fast Interlocks (<100 msec.). Besides, both interlocks parts are arranged in two layers: Local Layer and Master Layer. The Slow Interlocks subsystem is based on PLCs. This solution is being tested in the ESS Bilbao ECR ion source with positive results and the first version design is now complete for the LEBT system. For the Fast Interlocks local layer part, a solution based on NI cRIO has been designed and tested. In these tests a maximum response time of 3.5 usec. was measured for analog acquisition, threshold comparison and signal generation. For digital signals the maximum time response of a equivalent process was 500 nsec. These responses are considered valid for the standard need of the project. Finally, to extract information from the interlocks system and its monitoring, the Modbus/EPICS interface is used for Slow Interlocks, while EPICS output is produced by NI cRIO. Hence, it is planned to develop a light pyQT solution to perform this task.

INTRODUCTION

The ESS-Bilbao (ESSB) project is developing a light ion linear accelerator and neutron source [1]. The accelerator will have the following components: a high current Ion Source (IS), a Low Energy Beam Transport (LEBT), a Radio Frequency Quadrupole (RFQ), Medium Energy Beam Transport (MEBT) and a DTL (Drift Tube Linac). The IS will produce a proton beam with a maximum current of 60 mA. The LEBT will focus and monitor the particles into the RFQ, which increases the energy from 75KeV to 3MeV. The MEBT is in charge of coupling the beam into the DTL to reach a final energy of 50MeV. The protons will be fed into a Beryllium neutron production target[2].

The integrated control system at ESSB is divided into four main subsystems with different functionalities (Fig. 1) each one having its own almost independent network [3]:

1. Control Network (CN): Locally provides the controls for different devices. At a higher layer provides operating, monitoring, alarm and other services.

2. Interlock System (IN): Provides the local protection of the equipment and stops the beam in those situations with risk of damage for the machine.

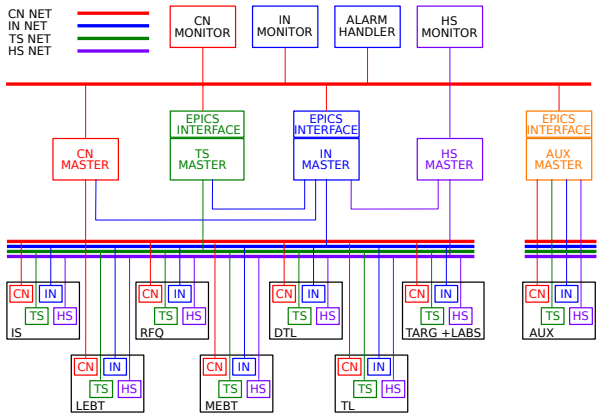

Figure 1: General control scheme.

3. Timing System (TS): Generates the necessary triggers for different devices operation and synchronizes events along the machine.

4. Human Safety (HS): Ensures the safety of personnel in case of machine malfunction.

In terms of hardware, CN is based mainly in PXI chassis for local control loops. These local controls are integrated into an EPICS network. The TS of the accelerator will be designed to be connected to a general timing system infrastructure based on White Rabbit. On the other hand, HS is built with safety PLCs together with local safety sensors (light barriers, emergency buttons,...) reaching the SIL 3/PLe safety performance.

In the case of IN, which is the main scope of this work, the treatment will be different depending on the type of signals considered: fast or slow. Slow signals are the ones which have a time response greater than 100 msecs whitout causing machine damage, while fast ones are required to have a response time smaller than 100 msecs. Slow signals processing is done by means of PLCs. On the other hand, the processing of fast signals will be done by FPGA based technology. For local equipment protection systems it will be performed by means of cRIO chassis. At higher lever, the specific hardware to process and transmit the signals to stop the beam is under study. Regarding the fast IN, it will be explored the possibility of having a redundant system through the TS by means of the WR Etherbone protocol.

Except the case of HS, the remaining systems are integrated into and EPICS network to provide operation, monitoring and high-level control functionalities. This way, different software services are implemented. For instance, CSS BEAST alarm handler [4] and archiving system based on a NoSQL database using HyperArchiver [5]. Non-

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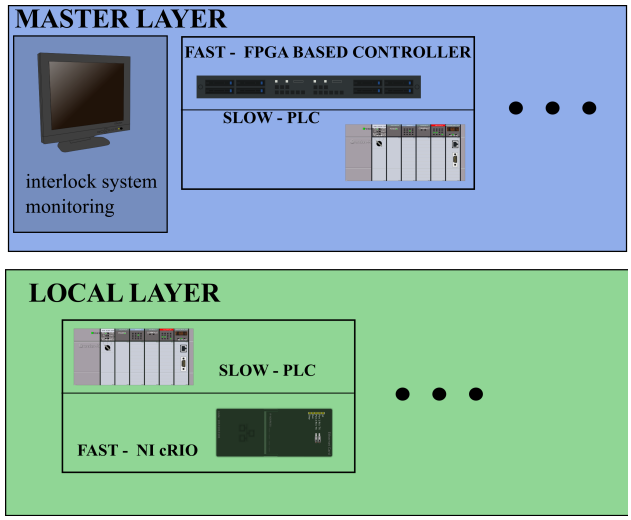

Figure 2: Architecture of the interlocks systems.

standard EPICS solutions integrating NI hardware into EPICS networks, will be used, as it was already discussed in [6].

This paper contains the description of the approach followed at ESSB to implement the interlock system in charge of protecting the machine. In the first section, the high level architecture of the whole system is described. Then the slow interlock part of the system is treated. Regarding the fast interlocks, the high level description of the system is outlined. Also, the results from a test bench to test the system requirements are presented. Then, as an example, the protection systems installed at ESSB Ion Source and LEBT are presented. In the last place, the integration of the described system into the whole integrated control system is explained.

ARCHITECTURE OF THE INTERLOCKS SYSTEMS

As stated previously, the interlocks system at ESSB will be divided into two subsystems depending on how fast is the required response. The first subsystem (Slow interlocks) handles all the signals involving a response time slower than 100 msecs. For faster response time, the Fast Interlocks subsystems are in charge of managing response . Moreover, there is an additional orthogonal division: Local Layer and Master Layer.

The Local Layer is in charge of the local protection of the equipment. Whenever any fault condition or hazard occurs that may result in some damage for the machine, the interlock system will take over the situation to avoid the risk. If necessary, the information will be transmitted to the Master Layer.

The main task of the Master Layer is to shutdown the beam and risky elements whenever there is a situation of risk for the machine. If the Local Layer detects any situation such that the machine can no longer be operated without causing damage to it, it will transmit this information to the Master Layer, which integrates information from all the local systems in order to shutdown the beam and other elements. Both layers will be composed by multiple instances of the same hardware devices.

As explained later, the integration of the Interlocks system with the rest of the services will be done at Master Layer.

SLOW INTERLOCKS

Slow interlock system takes care of those signals related to machine protection with a processing that requires a response time slower than 100 msecs.

The slow interlock system relies on Local PLCs and Master PLCs, corresponding to the local and master levels in the network defined in Fig. 1. These devices must ensure a proper reaction to avoid any harm whenever a hazard for any part of the machine occurs.

The Master PLCs will act at the master level and will be in charge of providing the supervision of different accelerator structures. These devices will also forward all the required interlocks information to the control room. They will be also in charge of rearming the interlock systems after an emergency. The rearming sequence has to be acknowledged by a human in order to avoid automatic restarts.

The Local PLCs will manage the local signals coming from the different controlled devices and prevent their damage by malfunctioning. They will also communicate and transmit information to the Master PLCs. There is implemented an architecture in which the Local PLC is able to protect the machine even when the Master PLC is out of order.

The connection between Master and Local PLCs will be done mainly by means of Modbus TCP/IP connections, but electrical boolean connections should also be implemented.

FAST INTERLOCKS

As stated before, the technology to be employed for the fast interlock systems will be FPGA based. It is worth mentioning that it is under study the use of White Rabbit by means of Etherbone[7] to redound the system.

Regarding the Master Level for fast interlocks different possibilities are under study by the time being. However for the Local level the NI cRIO is proposed.

The expected response constraints are imposed by the detection of the beam deviation and its quickly shutdown and by the interlocks required by certain elements such as the modulators for the Klystrons. This types of situations makes necessary to have a fast shutdown mechanism which is estimated to a maximum of 10 µs.

One of the main purposes of this work was to determine whether these constraints could be met with the NI cRIO..

Therefore, to test the capabilities of this device an experimental setup was arranged (Fig. 3). A pulse signal was generated by means of a signal generator. This signal is acquired by the NI 9223 analog input module or by the NI

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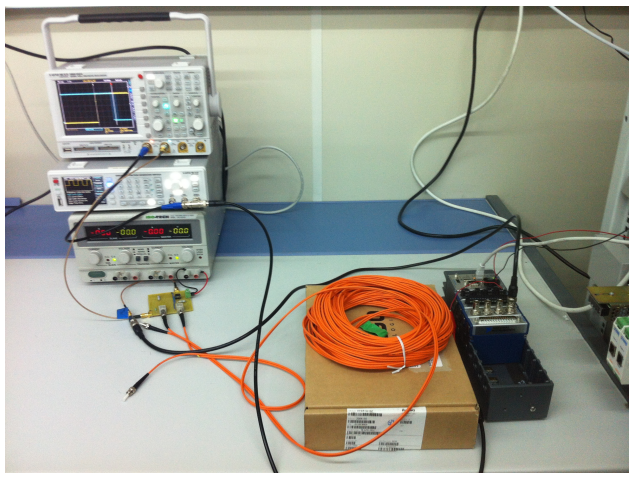

Figure 3: Test bench setup for fast interlock signals requirements evaluation.

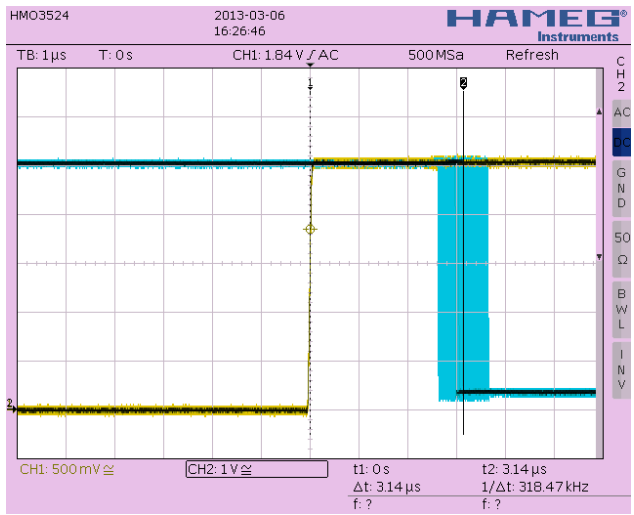

Figure 4: Measurement of transmission speed of fast interlock analog signals.

9402 Input Output digital module. Then it is processed by the FPGA of the cRIO 9112. If the analog signal overcome a threshold or the digital signal is true, another digital signal is generated through the NI 9112. This final signal is sent through a 30 meters optic fiber by using an in-house designed electrical to optical converter. The delay between the original generated pulse and the received signal at the end of the fiber after converting it back to electric signal was measured. The average delay obtained for the transmission of the analog signal was 3.14 µs. Figure 4 shows the difference between both signals. Figure 5 shows the results obtained for the transmission of digital signals. In this case the result is even better and the transmission average delay obtained is 412 nsecs. Both tests fulfill the requirements for playing the role of local interlock fast controller.

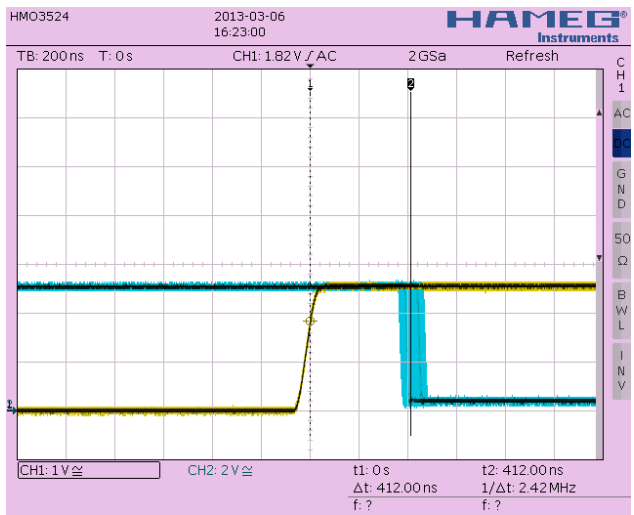

Figure 5: Measurement of transmission speed of fast interlock digital signals .

IN Application: Ion Source and LEBT Interlock System

In this section, the IN systems developed for the Ion Source and LEBT for the ESSB facility are explained.

Slow Interlocks This scheme for slow interlocks is already installed at ESSB in the ISHP project (Ion Source Hydrogen Positive) and in the LEBT. The local interlocks for the ion source is made up of two Scheneider PLCs. One of them is sitting on the ground area (Ground PLC) and the other sitting at the HV platform Platform PLC.

Ground PLC is in charge of centralising all the possible alarms, monitoring the startup process and managing the local interlock systems behavior. It also receives electrical signal from different sensors and devices (grounding arm, repeller power supply, etc.). It is communicated with the Platform PLC, which is in charge of protecting the different devices on the platform (RF generator, Klystron, power supplies,...).

In the case of the LEBT, the main elements from the perspective of the Slow Interlocks System are the solenoids. They need to be protected from any damage, which is generally caused by high temperature. The solenoids are cooled by means of water cooling loops. Therefore, different sensors are placed in these loops to assure their proper performance. The local protection is based on a Scheneider PLC, which is protecting and receiving signals from some equipment like power supplies, chillers, temperature sensors, pressure sensors, flow sensors,...

Another PLC at Master Level will be connected to the Local PLC at the LEBT and the Ground PLC at the Ion Source. The function of this PLC is to gather the information of the both systems to ensure communication between them and with the monitoring system. Therefore, this PLC will also forward the required information to the CN (EPICS based) system for monitoring the information by using Modbus TCP/IP protocol.

Fast Interlocks The fast interlocks main action for these system consists of shutting down the beam when is required by stopping the RF generator.

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For this case the system is almost the same as the one used in the testbench explained before. At the first steps of the LEBT only an ACCT will be used as diagnostic. The signal of the ACCT is acquired and treated by an FPGA hosted in a PXI chassis which determines whether it is a fault [8]. Then this signal is processed by means of the system stated in the previous section which generates the signal to stop the RF generator.

INTEGRATION OF THE INTERLOCKS SYSTEM

The ESSB facility is using EPICS as its main control framework middleware and the interlock systems as a whole must be integrated within this framework. Therefore, different EPICS based services (monitoring, alarms, archiving) will be integrated with the interlock system. In first place, EPICS based GUIs can be used for the monitoring of the interlock systems. That means that the Master Layer's slow and fast controllers should be integrated into the EPICS network. The slow controller is a PLC and could be easily integrated through Modbus TCP/IP protocol, however the EPICS integration of the fast interlock controller depends on the hardware itself. The alarm service can also be easily up an running when the previously mentioned integration is done.

CONCLUSIONS AND FUTURE WORK

In this work the approach for the interlock system being designed at ESSB has been presented. The system will be divided into two main layers: Master and Local. The Master one is in charge of integrating the information from the local interlock systems and shutdown the beam in the case of a fault. This layer has also an interface with EPICs. In this way it is also used to provide the interlock system with services for monitoring, alarms and archiving. The Local Layer will be in charge of the local protection of the equipment. Slow controller will be all PLC based. An study to use NI cRIO as a local fast interlock controller has been performed. The measured delay was around 3.5 µs for processing analog signals and 500 nsecs for processing digital signals. The results show that it is suitable to be used as a local fast interlocks controller. The fast controller at master level is under study at this moment.

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