DEVELOPMENT OF A MACHINE PROTECTION SYSTEM FOR FERMILAB'S ASTA FACILITY*

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Abstract

Fermilab's Advance Superconducting Test Accelerator (ASTA) under development will be capable of delivering an electron beam with up to 3000 bunches per macro-pulse, 5Hz repetition rate and 1.5 GeV beam energy in the final phase. The completed machine will be capable of sustaining an average beam power of 72 KW at the bunch charge of 3.2nC. A robust Machine Protection System (MPS) capable of interrupting the beam within a macro-pulse and that interfaces well with new and existing controls system infrastructure is being developed to mitigate and analyze faults related to this relatively high damage potential. This paper will describe the component layers of the MPS system including main actuators such as the FPGA-based Laser Pulse Controller, the Beam Loss Monitoring system design and the controls and related work done to date.

INTRODUCTION

The ASTA facility will be capable of testing 3 or more ILC-type SRF cryomodules under full ILC beam intensity and bunch structure. In addition, test beamlines and downstream beamlines will provide a venue for advanced accelerator R&D (AARD). Figure 1 shows a plan view of the facility that is divided into low energy and high energy phases.

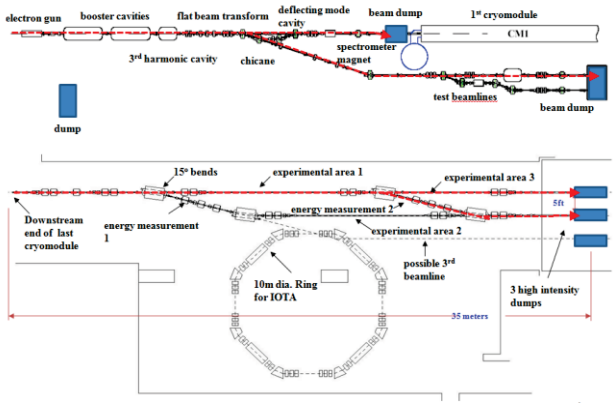

Figure 1: Machine layout.

The electron beam is produced by a 1.3 GHz RF photo-injector and then accelerated to ~50 MeV by two 1.3 GHz SRF cryomodules, each containing a single 9-cell cavity, before being injected into the 1st 8-cavity cryomodule. Initial beam commissioning of the cryomodule string will take place with a single Tesla type III+ cryomodule [1] driven by a 5 MW klystron; considered stage 1 [1]. The next stage of commissioning will take place with two Tesla type III+ cryomodules and one ILC type IV cryomodule. This cryomodule string will be driven by a 10 MW multi-beam klystron, with its associated HV power supply, modulator, and waveguide distribution system. The high energy beamlines downstream of the cryomodules will provide transport to an AARD experimental area and to the high energy beam dump.

MPS DESIGN CONCEPT

The Machine protection System (MPS) is being developed in stages that are commensurate with the commissioning goals for ASTA. The primary objectives from the MPS point of view is to mitigate beam induced damage to the machine components and to provide a comprehensive over-view of the entire accelerator based on the input status of all the relevant subsystems [2].

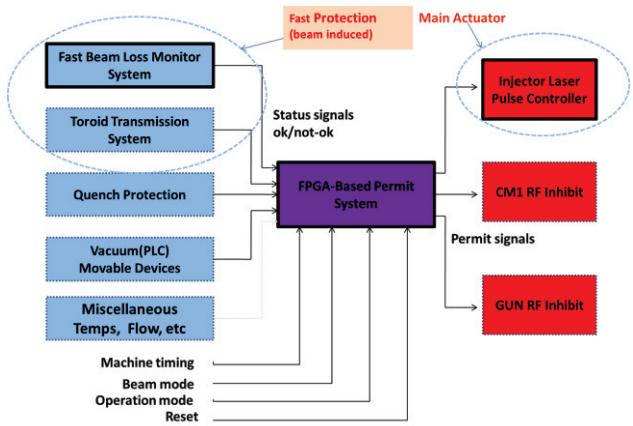

Figure 2: MPS Overview.

Figure 2 illustrates the overall MPS design which is divided into 3 layers; a sensor layer to collect sub-system status, a process layer that utilizes the status to generate the permits and an actuator layer to receive the permits and inhibit the beam. The initial stage of this development involves the design of the Laser Pulse Controller.

LASER PULSE CONTROL

The backbone of the ASTA facility is a radio-frequency (RF) photo-injector. The electron source is a 1-1/2 cell cylindrical-symmetric RF gun with a Cs2Te photocathode. The cathode is illuminated by an ultraviolet (UV, λ=263 nm) laser pulse produced via frequency quadrupling of an amplified infrared (IR, λ=1054 nm) pulse [3]. The photocathode drive laser enables the generation of a train of bunches repeated at 3 MHz within a 1-ms-duration. The 5-MeV electron bunches, exiting the RF gun are then accelerated with two superconducting radio-frequency (SRF) TESLA-type cavities (CAV1 and

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CAV2) to approximately 50 MeV. Thus one of the main actuators for the MPS is the injector Laser Pulse Controller (LPC). This device is designed to control the number and the spacing of bunches in a macro-pulse by picking single laser pulses out of a train; achieved by manipulating the Pockels cell (voltage-controlled wave plates). The LPC basically provides a gate, the length of which determines how many 3MHz laser pulses are accepted. The gate widths (minimum through maximum), delay (relative to RF), and timing for first bunch trigger along with several other parameters are configured via the control system. The maximum allowed duration for the gate is 1ms. Figure 3 illustrates this scheme diagrammatically.

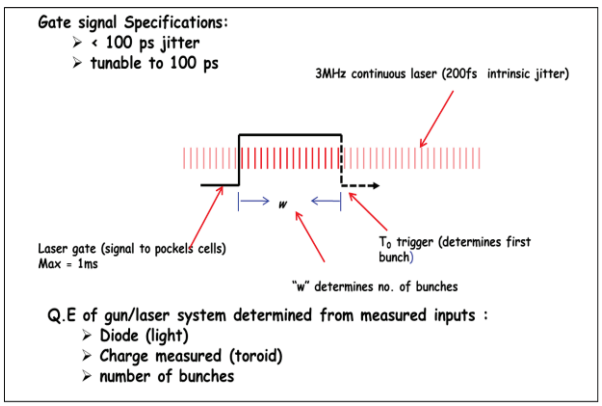

Figure 3: LPC Timing.

This system is also the main actuator for beam inhibits issued by the MPS. It is built on a VME platform with a fully programmable general purpose FPGA board. It has inputs for the requested beam modes (intensity limits) defined by the logic layer of the MPS, the MPS permit signal, the 3 MHz machine timing, and for a macro-pulse trigger. It has control outputs for the Pockels cell driver, a mechanical shutter and a first bunch timing signal. From the protection system point of view the pulse controller is used to:

- Block the Pockels cell based pulse kickers as long as the MPS input is in an alarm state.
- Enforce the limit on the number of bunches as given by the currently selected beam mode.
- Close the laser shutter on request of the MPS. This may happen when there is no valid operational mode or when some combination of loss monitors exceed thresholds which trigger a dump condition. Note that this minimum setting is the default number of bunches allowed and is designed to meet shielding requirements as well as to force operation below the threshold for machine damage potentials.

FAST PROTECTION

The MPS includes a fast protection system that is based on 40 Beam Loss Monitors (BLMs). It is being designed to interrupt the beam within a macro-pulse and relies heavily on the ability to detect and react to losses within a few nano-seconds; the loss monitors are made from plastic scintillator material and are coupled to photomultiplier tubes. First injector beam test, Figure 4, with these loss monitors indicate that the monitor possess the necessary sensitivity required to detect low charged losses as well as dark current.

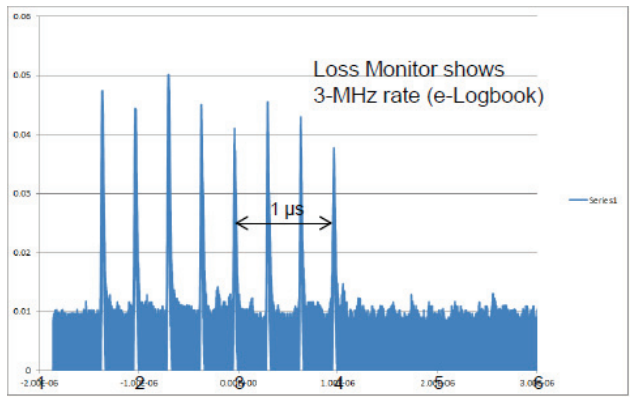

Figure 4: First Beam results.

These BLMs will serve the dual purpose as an accelerator diagnostic and as the primary detectors for fast machine protection. The monitors must therefore deliver a measurement of beam and dark current losses to the control system as well as generate a fast alarm signal when the beam losses exceed user-defined thresholds. The time resolution of the loss measurement must provide the ability to distinguish single bunches within each macro pulse. This requires a sampling frequency of at least 3 MHz with a repetition rate of 5 Hz. The BLMs are being integrated into a beam loss monitoring system capable of generating a fast trip signal based on a programmable fast comparator setting as well as an alarm condition that is derived by comparing the outputs of the PMT signals with various programmable thresholds within the BLM electronics. This alarm output is a critical component for machine protection. The desire is to provide a machine protection trip well before the beam can damage accelerator components. If one of the programmed thresholds is exceeded or if an error condition such as a high voltage failure or failed monitor is detected the system should report this to the MPS logic which in turn reduces the intensity or inhibits the beam via the LPC. The main requirements for the BLM system are:

- Provide both machine protection and diagnostic functions.
- Instantaneous read-back of beam loss
- Digital output for integrating and logarithmic signal (16 bit)
- Built in self-test and on-board signal injection for testing of monitors between pulses.
- FPGA controlled
- Local data buffer
- VME interface to ACNET control system
- Continuous and pulsed monitoring
- Wide dynamic range

Figure 5 is a simplified diagram of the signal processing path and the controls interface of the loss monitor

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electronics. A 125MHz digitizer board provides digitized signals and contains 512 MB of on-board RAM used for data logging.

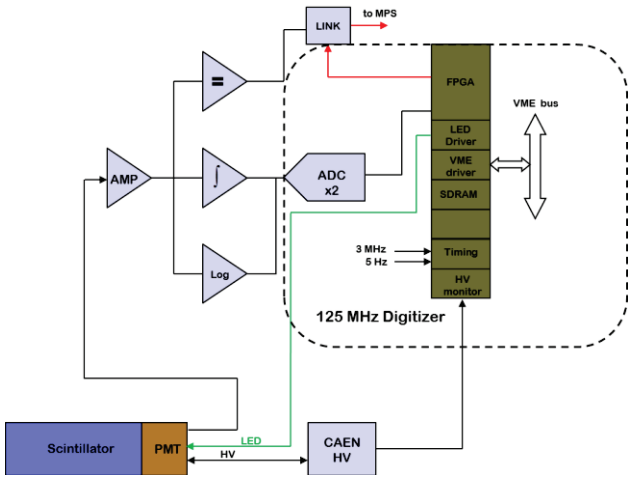

Figure 5: Loss monitor board electronics.

CONTROLS INTEGRATION

Controls integration is a key component of the MPS design concept as it not only ensures system reliability, but also allows for post-mortem analysis of detected trips. A PowerPC 5500 series board was chosen as the slot 0 controllers for the various MPS hardware components including both the LPC and BLM systems. These boards run at 1GHz, have over 1GB of expandable Ram and provide the reading and setting interface to the ACNET control system. Figure 6 illustrates the General Purpose FPGA board (V1495) that serves as the backbone for both the LPC and the main MPS system. This board handles all of the real-time computing required at the hardware level.

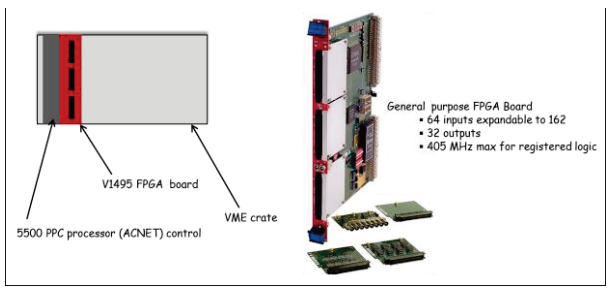

Figure 6: V1495 FPGA board.

A daughter card has been designed for the V1495 board that provides 128-MB of SDRAM. This memory extension is crucial as post-mortem fault analysis will require extensive buffers to log sensor readings around a detected fault. The daughter card includes an additional FPGA that is used as an interface and a SDRAM controller. The data path between the daughter card and the main MPS FPGA board is 32 bits wide. If running at 62.5 MHz, the peak through-put is 250 MB/s. Figure 7 shows a block diagram of this card and interface to the main MPS board.

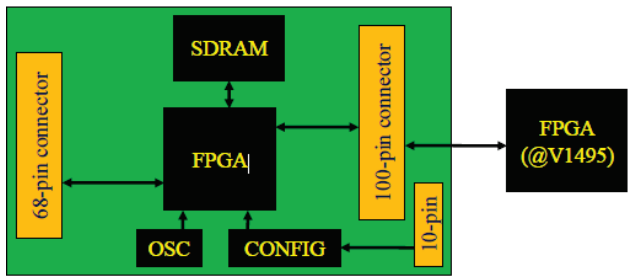

Figure 7: Daughter card.

CONCLUSION

Significant progress has been made in developing the MPS system with the design of both the LPC and BLM systems. These systems were crucial in enabling and displaying the first photo-electrons produced at ASTA. Additional effort is underway towards collecting subsystem status and developing a reliable MPS for ASTA. System integration into the complex and commission challenges lay ahead.

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